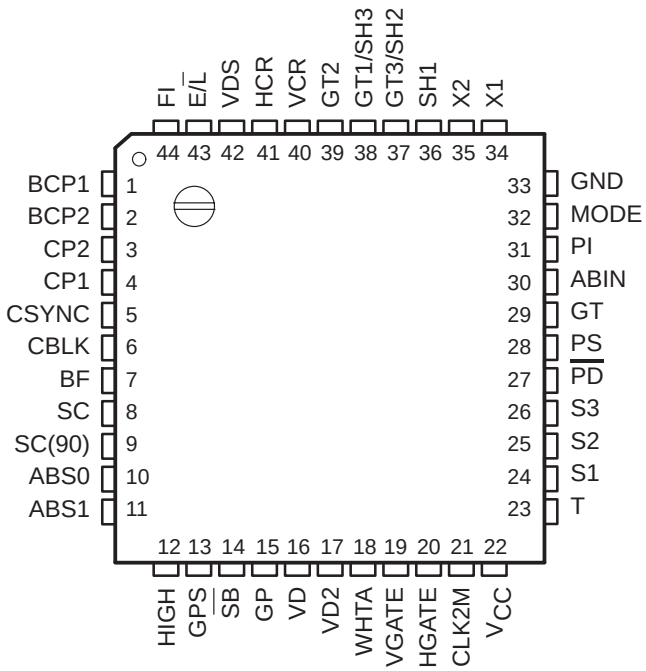
- **NTSC-Timing Operation**
- **Solid-State Reliability**
- **Color and Monochrome Operation**
- **Four Selectable-Antiblooming Modes**
- **Variable-Integration-Time Option**
- **Surface-Mount Package**
- **Clamp-Pulse Select Option**
- **Horizontal and Vertical Resets for External Synchronization**

FS PACKAGE
(TOP VIEW)



description

The SN28835 is a monolithic integrated circuit designed to supply timing signals for the Texas Instruments (TI™) 8-mm TC242/TC244 color and TC243/TC245 monochrome CCD image sensors. The SN28835 supplies both CCD-drive signals and NTSC-television synchronization signals at standard video rates. It requires a single 5-V supply voltage and a 14.318-MHz crystal-oscillator input. The SN28835 provides the user with several options including multiple antiblooming modes, variable-integration time, external synchronization, and delayed horizontal transfer.

The SN28835 is designed to drive the CCD image sensor through intermediary level-shifting devices such as the TI TMS3473B parallel driver and the SN28846 serial driver. It also supplies sample-and-hold signals for the TI TL1593 3-channel sample-and-hold circuit and multiplex signals for the TI TL1051 video preprocessor. The SN28835 NTSC synchronization-signal outputs include composite sync, composite blank, clamp, subcarrier, subcarrier delayed by 90 degrees, and burst flag.

The SN28835 is supplied in a 44-pin plastic flat package and is characterized for operation from –20°C to 45°C.

This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, precautions should be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

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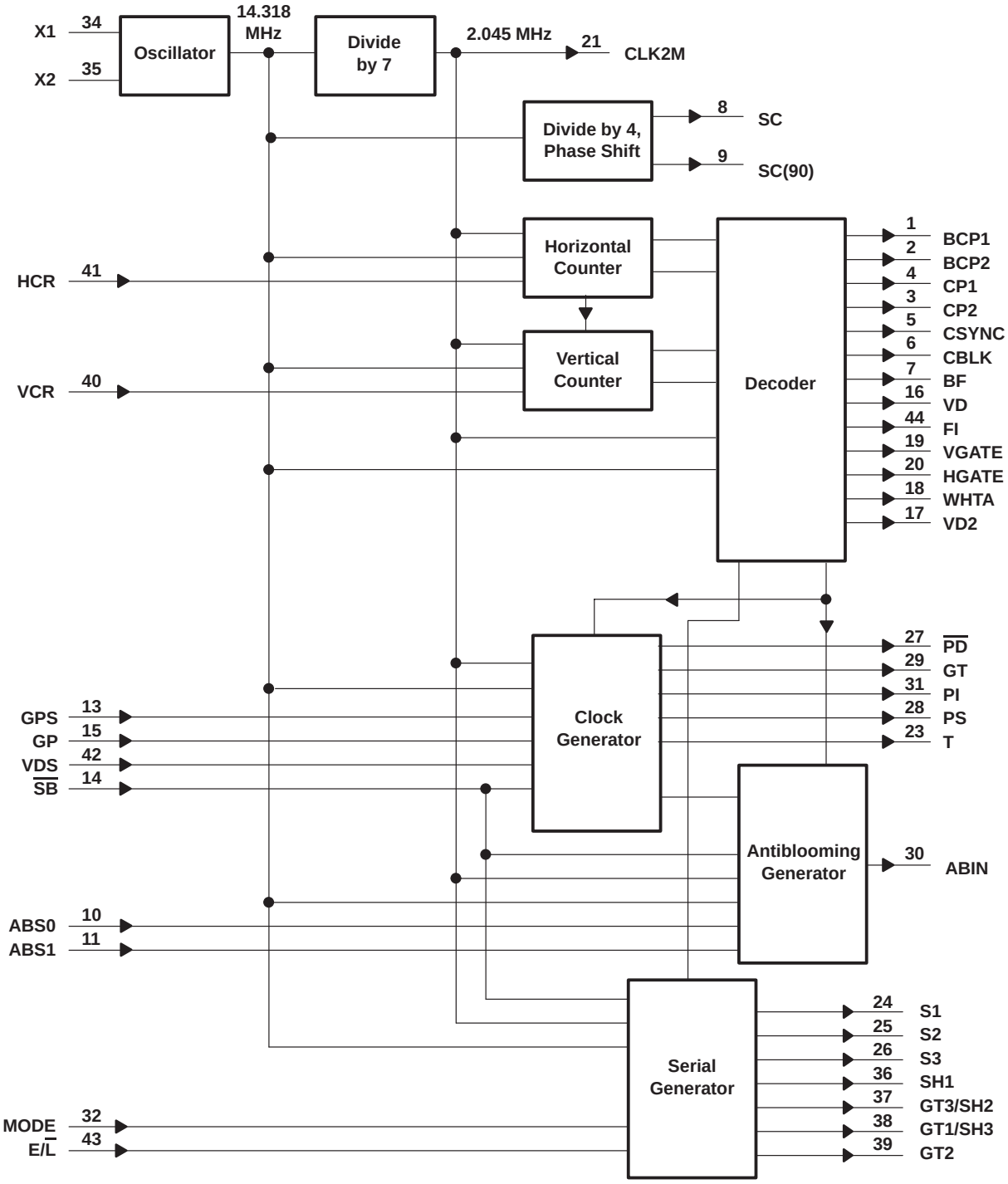
functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ABIN	30	O	Antiblooming in
ABS0	10	I	The levels on these two terminals determine which of the four antiblooming modes is selected: ABS1 / ABS0 / Operation L / L / No ABG pulses L / H / 2-MHz burst of ABG pulses H / L / 1-MHz burst of ABG pulses H / H / 1-MHz continuous ABG pulses
ABS1	11	I	
BCP1	1	O	Optical black clamp
BCP2	2	O	Optical black clamp
BF	7	O	Burst flag
CBLK	6	O	Composite blank
CLK2M	21	O	2-MHz clock
CP1	4	O	Clamp
CP2	3	O	Clamp
CSYNC	5	O	Composite sync
E/$\overline{L}$	43	I	Delay select for S1, S2, S3. When E/$\overline{L}$ is high, the three serial-transfer pulses occur early relative to the sample-and-hold pulses SH1, SH2, and SH3. When E/$\overline{L}$ is low, the three serial-transfer pulses occur late relative to the sample-and-hold pulses.
FI	44	O	Field index
GND	33		Ground
GP	15	I	Exposure control: GP gates the PS and PI outputs (see the description of GPS)
GPS	13	I	When GPS is high, the timer operates in the normal-integration-time mode (t_{int} = 16.67 ms) and VD is connected internally to GP. To operate the imager in the variable-integration-time mode, GPS must be held low and a user-defined logic circuit must be inserted between VD and GP to vary the integration time (see Figure 1).
GT	29	O	TMS3473B parallel-driver MIDSEL input switch
GT1/SH3	38	O	GT1/SH3 is a logic signal for both Y gate 1 of the TL1051 video preprocessor and sample-and-hold channel 3 of the TL1593 3-channel sample-and-hold circuit.
GT2	39	O	Y gate 2 for the TL1051 video preprocessor
GT3/SH2	37	O	GT3/SH2 is a logic signal for both Y gate 3 and sample-and-hold channel 2 of the TL1051 video preprocessor.
HCR	41	I	Horizontal-counter reset
HGATE	20	O	Decoded H count signal. HGATE is a test point and is not used in normal operation.
HIGH	12	I	Not used (tie high)
MODE	32	I	TC243/TC245 CCD select. When MODE is low, the TC244/245 CCD imager is selected; when MODE is high, the TC242/243 is selected (see the appropriate data sheets for imager differences).
$\overline{PD}$	27	O	Power down. A low-logic level on $\overline{PD}$ causes the device to enter a low power-consumption mode.
PI	31	O	Parallel-image-area gate clock
PS	28	O	Parallel-storage-area gate clock
$\overline{SB}$	14	I	Standby-mode select. When $\overline{SB}$ is high, normal operation is selected; when $\overline{SB}$ is low, the power-down mode is selected.
SC	8	O	Subcarrier
SC(90)	9	O	Subcarrier phase shifted by 90 degrees
SH1	36	O	Sample and hold 1

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
S1	24	O	Serial clock 1
S2	25	O	Serial clock 2
S3	26	O	Serial clock 3
T	23	O	Transfer-gate clock
V_{CC}	22		DC power
VCR	40	I	Vertical-counter reset
VD	16	O	Vertical drive
VDS	42	I	Vertical-dump speed. When VDS is high, the vertical-dump frequency is 3.58 MHz; when VDS is low, the vertical-dump frequency is 2 MHz.
VD2	17	O	Real-display-area signal. VD2 is a test point and is not used in normal operation.
VGATE	19	O	Decoded V count signal. VGATE is a test point and is not used in normal operation.
WHTA	18	O	WHTA is a test point and is not used in normal operation.
X1	34		Crystal oscillator (see Figure 2)
X2	35		

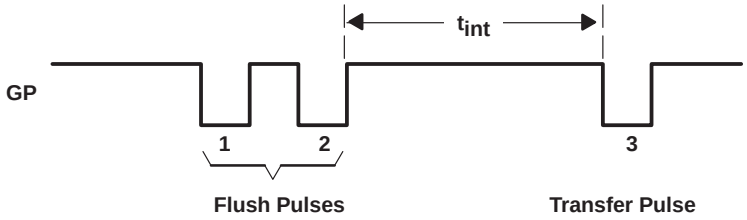


Figure 1. GP Flush and Transfer Pulses

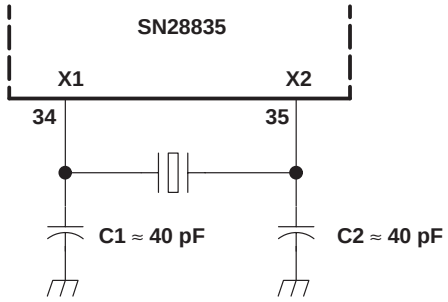
variable-integration-time mode

In addition to the normal TV mode of operation, the SN28835 timing generator offers an optional variable-integration mode for use with the TC244 and TC245 CCD area-array image sensors. The variable-integration mode is selected by applying a low-logic level to GPS. This low-logic level disables the vertical-drive (VD) signal from controlling, internal to the timer, the image-area and storage-area parallel transfer signal (GP).

Prior to the start of a new integration period, the charge that has accumulated in the image area must be transferred out. To flush this previous signal or dark-current charge from the image area, GP is pulsed low two times. Each low pulse generates 256 image-area and storage-area gate and transfer signals that shift the unwanted charge into the clearing drain. This clearing function should be performed during the high time of the VD signal (see Figure 3 through Figure 12).

The new integration period continues as long as GP remains high. GPS must be held at a low-logic level to prevent VD from controlling GP internally. The integration ceases and the readout occurs when VD and GP are pulsed low simultaneously; this is accomplished by taking GPS to a high-logic level. The readout timing is dependent on the vertical-drive pulse; this means that the total-integration time is a multiple of 1/60 of a second plus the time interval between the last GP low pulse and the next VD low pulse. The image readout occurs within the normal 1/60-second readout interval. If the integration time is less than 1/60 of a second, normal output operation occurs; if the integration time is greater than 1/60 of a second, a frame buffer may be required to capture the image.

Integration times greater than 1/60 of a second result in image degradation at temperatures greater than 25°C due to dark-current generation. The degradation is seen as a decrease in dynamic range (contrast) and an increase in noise. It is recommended that the image sensor be cooled for long-exposure operation. The dark-current generation is reduced by a factor of two for each 7°C temperature decrease. The sensor operates at –30°C. Cooling can be accomplished by using a thermoelectric or Peltier cooler attached to the image sensor. Condensation on the header must be prevented by isolating the cooled sensor from moist air. Vacuum isolation is preferred; however, the continual flushing of dry nitrogen across the header can also prevent condensation.



NOTE: The SN28835 is designed for use with a crystal oscillator. The X1 and X2 terminals should not connect directly to external driver outputs.

Figure 2. Connection of an External Crystal Oscillator to the SN28835

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.3 V to 7 V
Input voltage range, V_I . . . . . –0.3 V to V_{CC} + 0.3 V
Output voltage range, V_O . . . . . –0.3 V to V_{CC} + 0.3 V
Continuous total power dissipation at (or below) T_A = 25°C . . . . . 300 mW
Operating free-air temperature range, T_A . . . . . –20°C to 45°C
Storage temperature range, T_{STG} . . . . . –55°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level input voltage, V_{IH}	V_{CC} x 0.7			V
Low-level input voltage, V_{IL}			0.8	V
Operating frequency		14.318		MHz
Power-up time		300		µs
Operating free-air temperature, T_A	–20		45	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)‡

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	GT3/SH2 and GT1/SH3	V_{CC} = 4.5 V,	I_{OH} = –4 mA	3.5			V
	All other outputs	V_{CC} = 4.5 V,	I_{OH} = –2 mA	3.5			
V_{OL}	GT3/SH2 and GT1/SH3	V_{CC} = 4.5 V,	I_{OL} = 4 mA			0.5	V
	All other outputs	V_{CC} = 4.5 V,	I_{OL} = 2 mA			0.5	
I_{IH}§		V_{IH} = 5 V				1	µA
I_{IL}		V_{IL} = 0		–30	–200	–500	µA
$I_{CC(AV)}$	Average supply current				10	30	mA
$I_{CC(S)}$	Standby supply current				1		mA

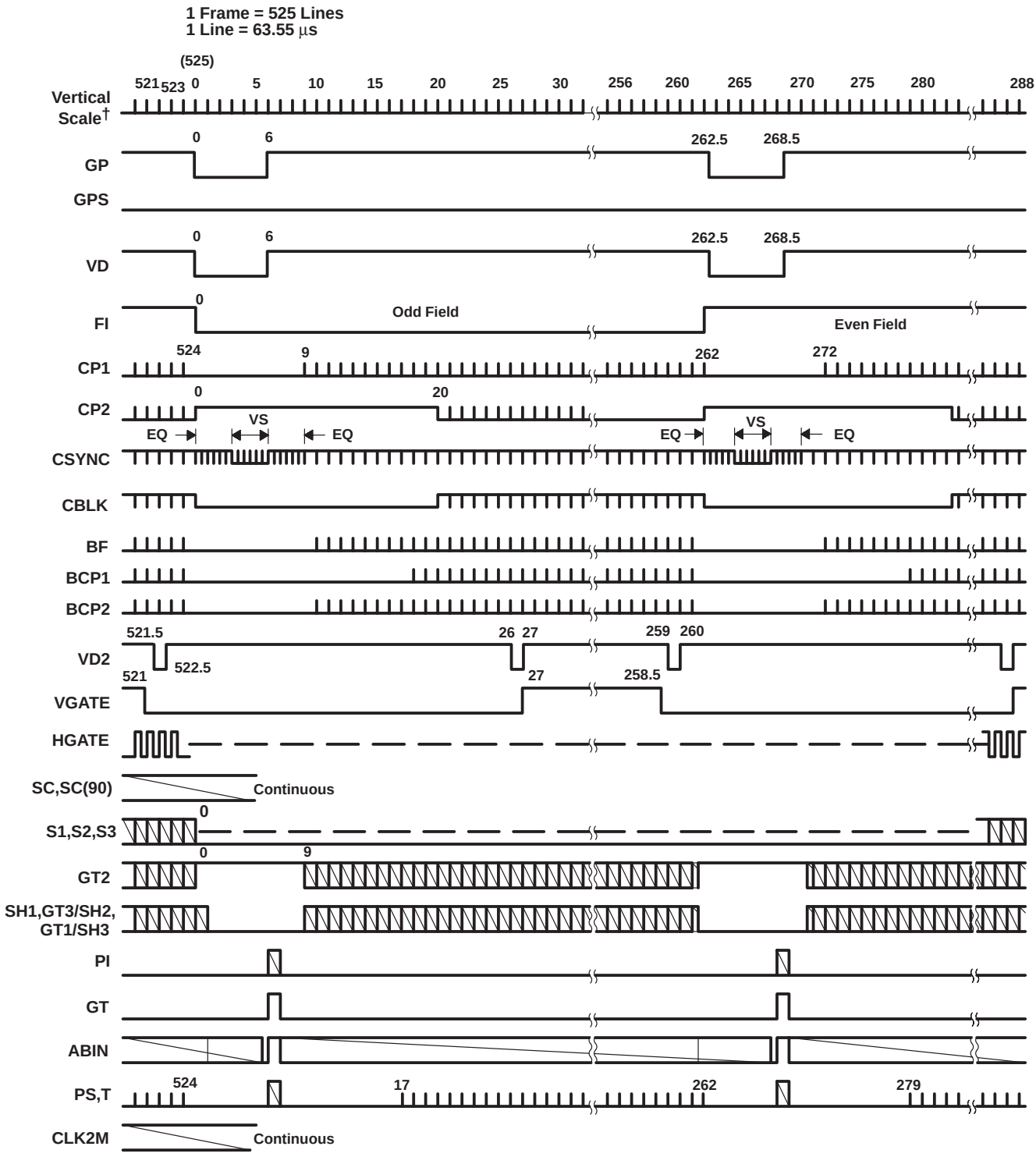
‡ The $\overline{SB}$ input is a Schmitt-trigger input with 0.1-V to 1-V hysteresis.

§ All inputs except X1 have pullup-current sources.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Frequency	SC, SC(90)	C_L = 50 pF		3.579545		MHz
		S1, S2, S3, SH1, GT2, GT1/SH3, GT3/SH2			4.772727		
t_w	Pulse duration	SC, SC(90)			140		ns
		S1, S2, S3, SH1, GT2, GT1/SH3, GT3/SH2			70		
t_r	Rise time	GT1SH3 and GT3SH2	C_L = 50 pF		10		ns
		All other outputs			50		
t_f	Fall time	GT1SH3 and GT3SH2			10		ns
		All other outputs			50		

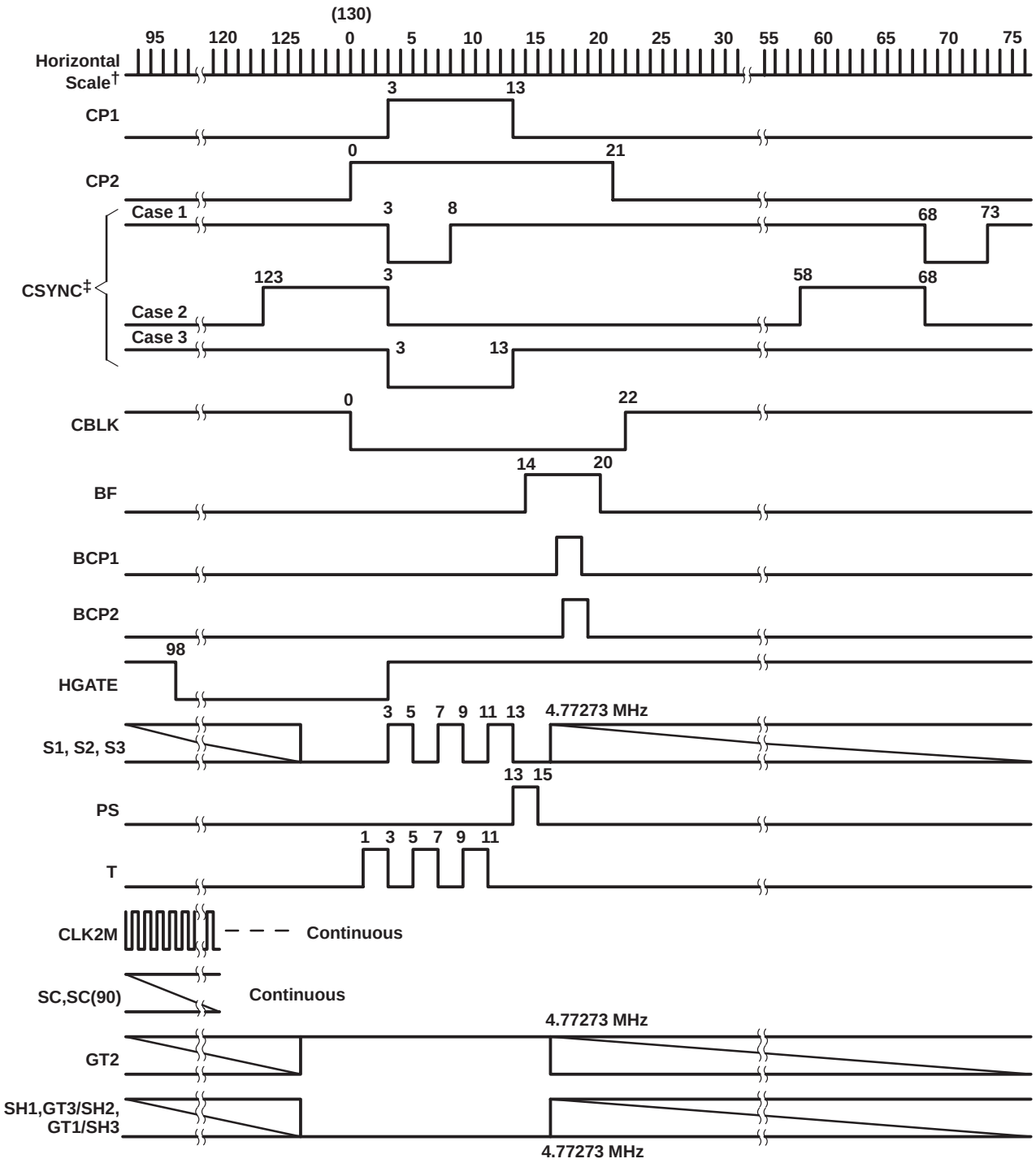
PARAMETER MEASUREMENT INFORMATION



† 525 intervals equal 33.3 ms equals 1 TV frame

Figure 3. Vertical Timing, Normal-Integration Mode

PARAMETER MEASUREMENT INFORMATION



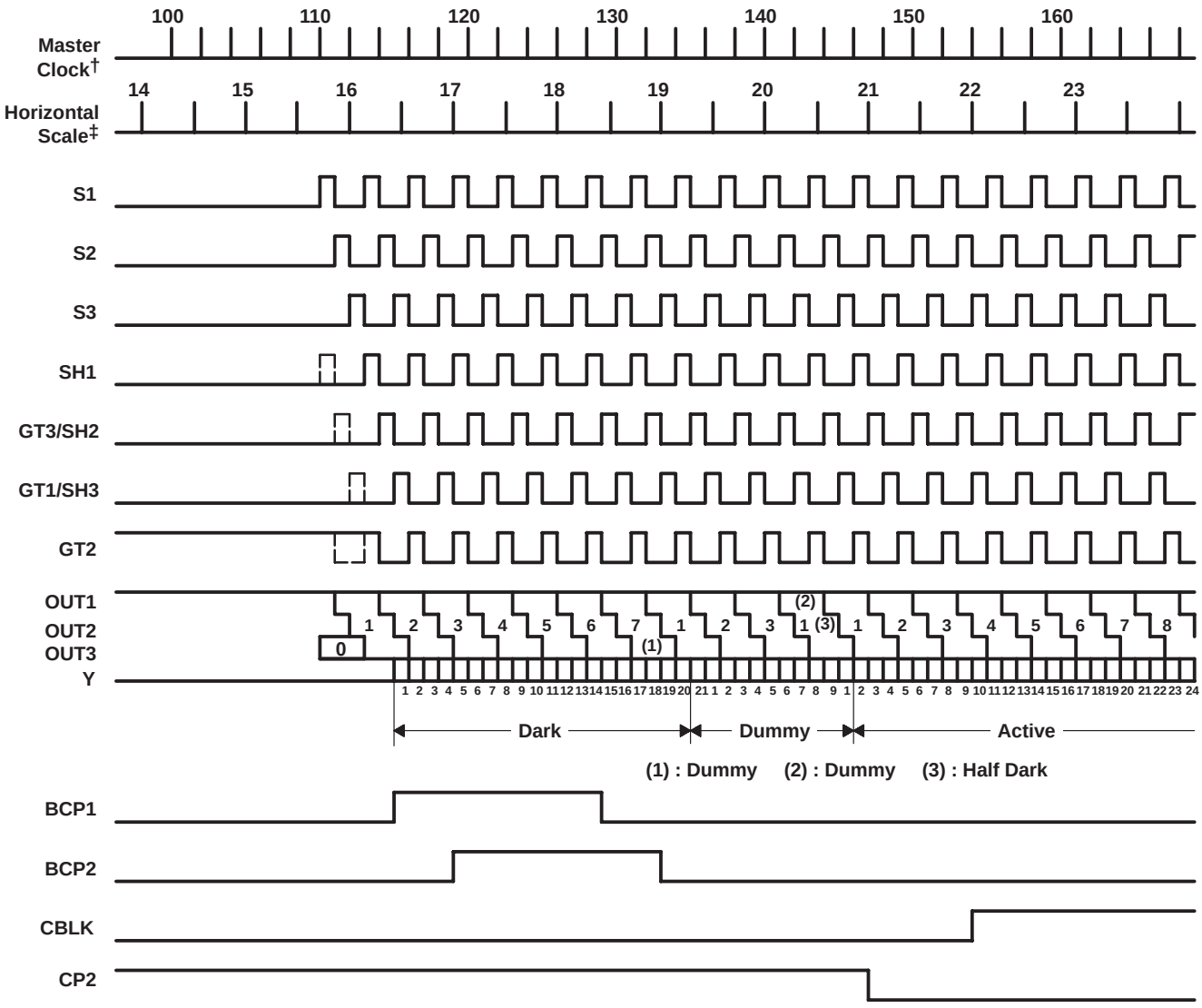
† 130 intervals equal 63.55 µs equals one horizontal-scan line

‡ CSYNC varies depending on which horizontal-scan line of a 262.5-line TV field is being examined:

- Case 1 depicts the equalizing pulses that occur during horizontal-scan lines 1, 2, 3, 7, 8, and 9.
- Case 2 depicts the vertical serration pulses that occur during horizontal-scan lines 4, 5, and 6.
- Case 3 applies to all remaining horizontal-scan lines.

Figure 4. Horizontal Timing

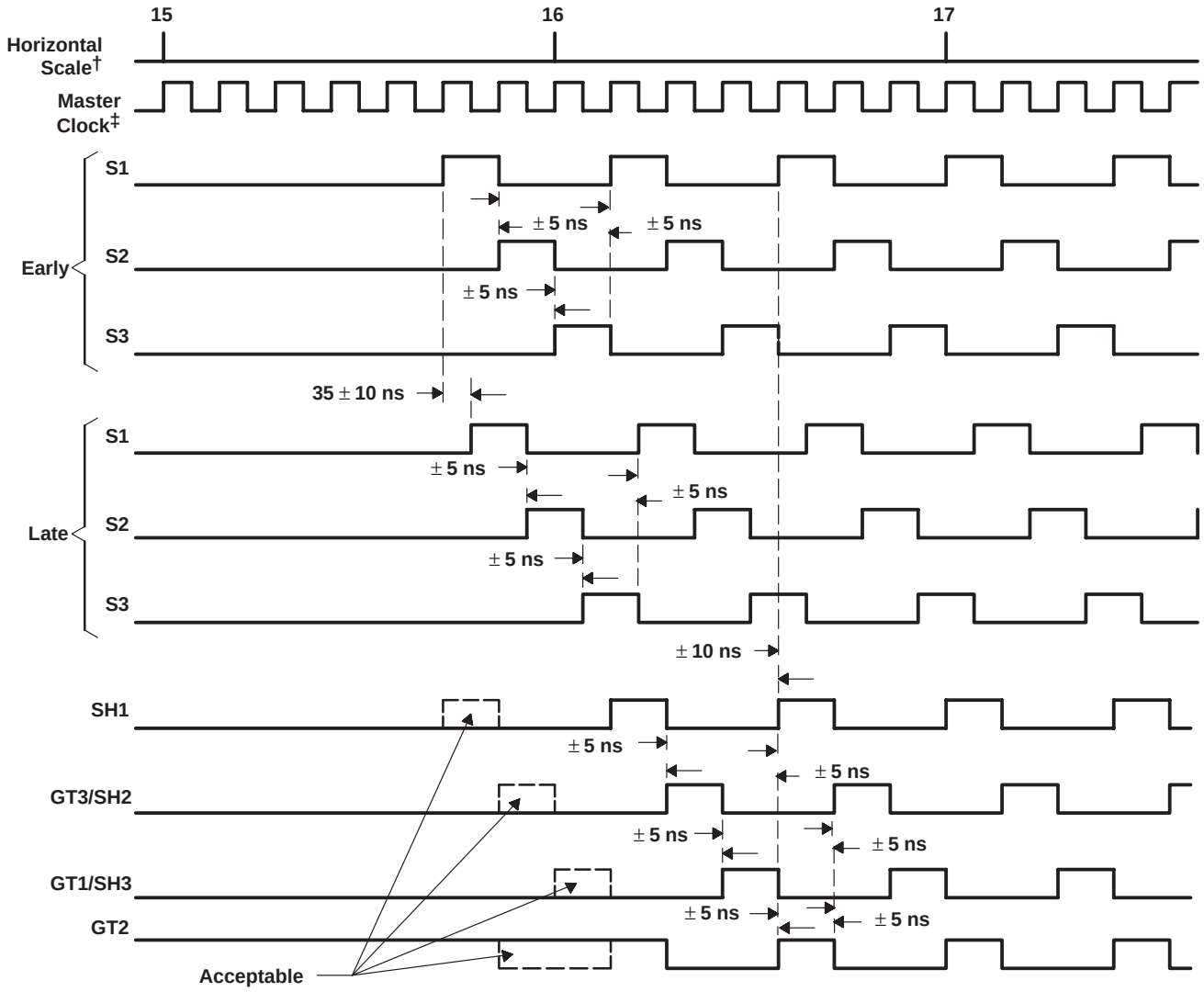
PARAMETER MEASUREMENT INFORMATION



† 910 master-clock periods equal 63.55 µs equals one horizontal-scan line
‡ 130 intervals equal 63.55 µs equals one horizontal-scan line

Figure 5. Serial and Sample-and-Hold Timing at Start of Horizontal Transfer

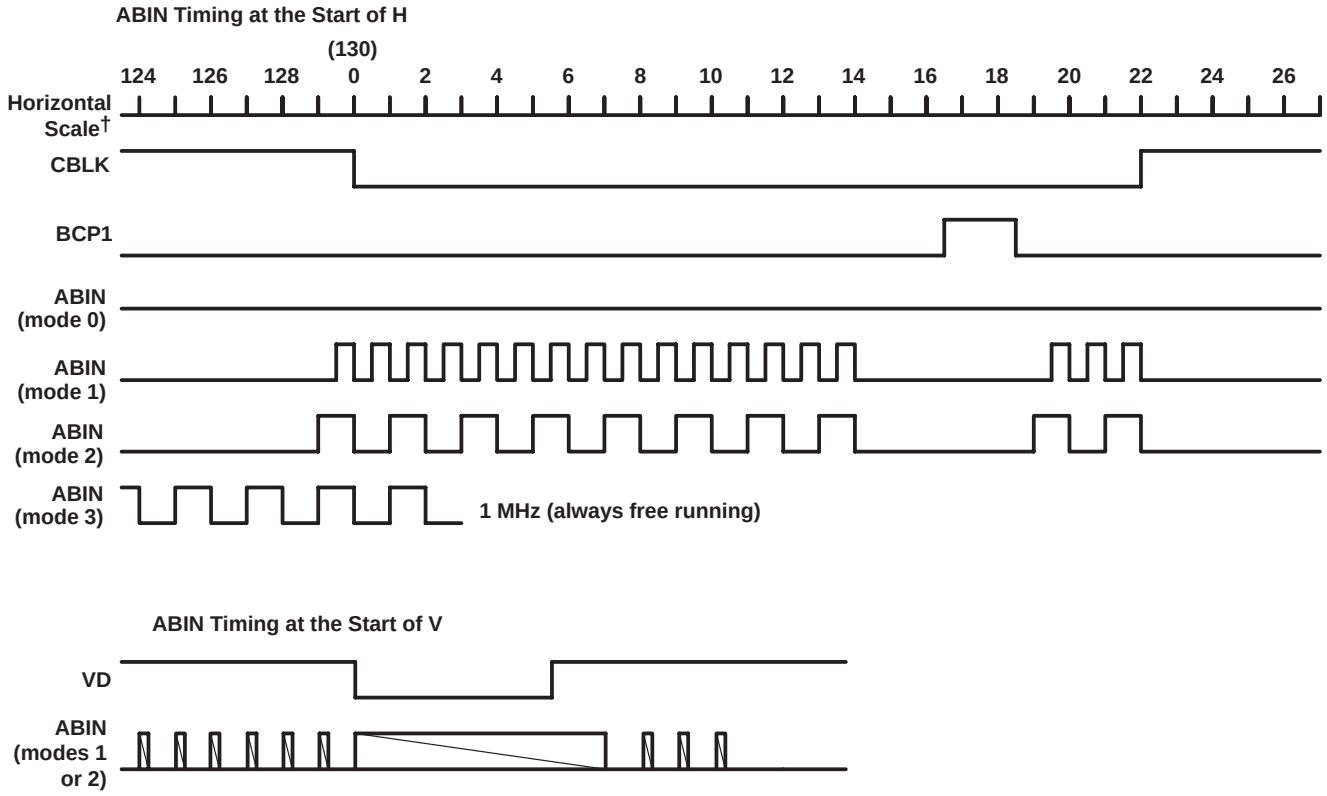
PARAMETER MEASUREMENT INFORMATION



† 130 intervals equal 63.55 μs equals one horizontal-scan line
‡ 910 master-clock periods equal 63.55 μs equals one horizontal-scan line

Figure 6. Timing for S and SH Signals Using Both Early and Late Options

PARAMETER MEASUREMENT INFORMATION



† 130 intervals equal 63.55 μs equals one horizontal-scan line
NOTE: GPS is high (VD is connected to GP internally)

ANTIBLOOMING-MODE SELECTION			
MODE‡	ABS1	ABS0	ABIN
0	L	L	Low
1	L	H	2-MHz burst
2	H	L	1-MHz burst
3	H	H	1-MHz free running

‡ In mode 2, the duty cycle is 43%; in all other modes, the duty cycle is 50%.

Figure 7. Antiblooming Timing at Start of Horizontal Transfer

PARAMETER MEASUREMENT INFORMATION

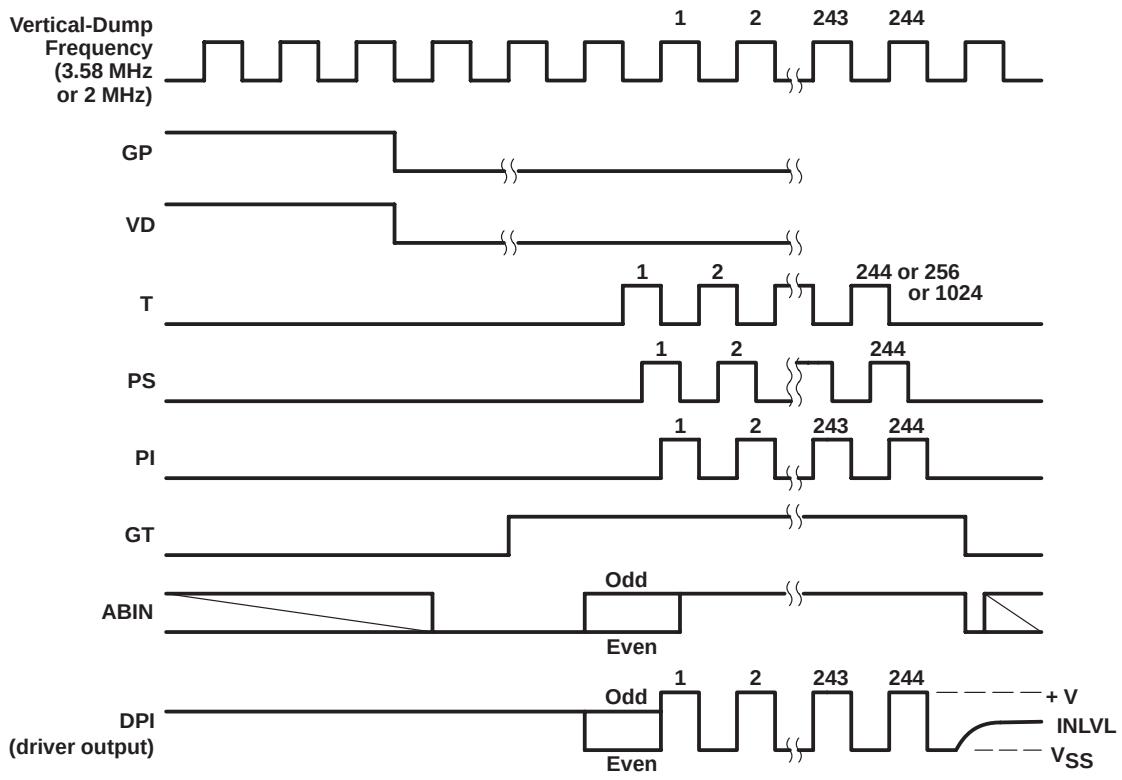


Figure 8. PI, PS, T, and ABIN Timing

NOTES: A. When the vertical-dump frequency is 2 MHz (chosen by a low level on VDS), the duty cycle of T, PS, and PI is 4/7 high and 3/7 low; the duty cycle is 50% for a vertical-dump frequency of 3.58 MHz.
B. When GPS is high, VD is connected internally to GP.
C. Neither SC nor SC(90) is used for the 3.58-MHz clock.
D. GP goes low when VD is low. PI, PS, T, and GT begin clocking after VD goes high.
E. The 90° phase shift between T, PS, and PI pulses is equal to one 14-MHz crystal-oscillator clock period.

PARAMETER MEASUREMENT INFORMATION

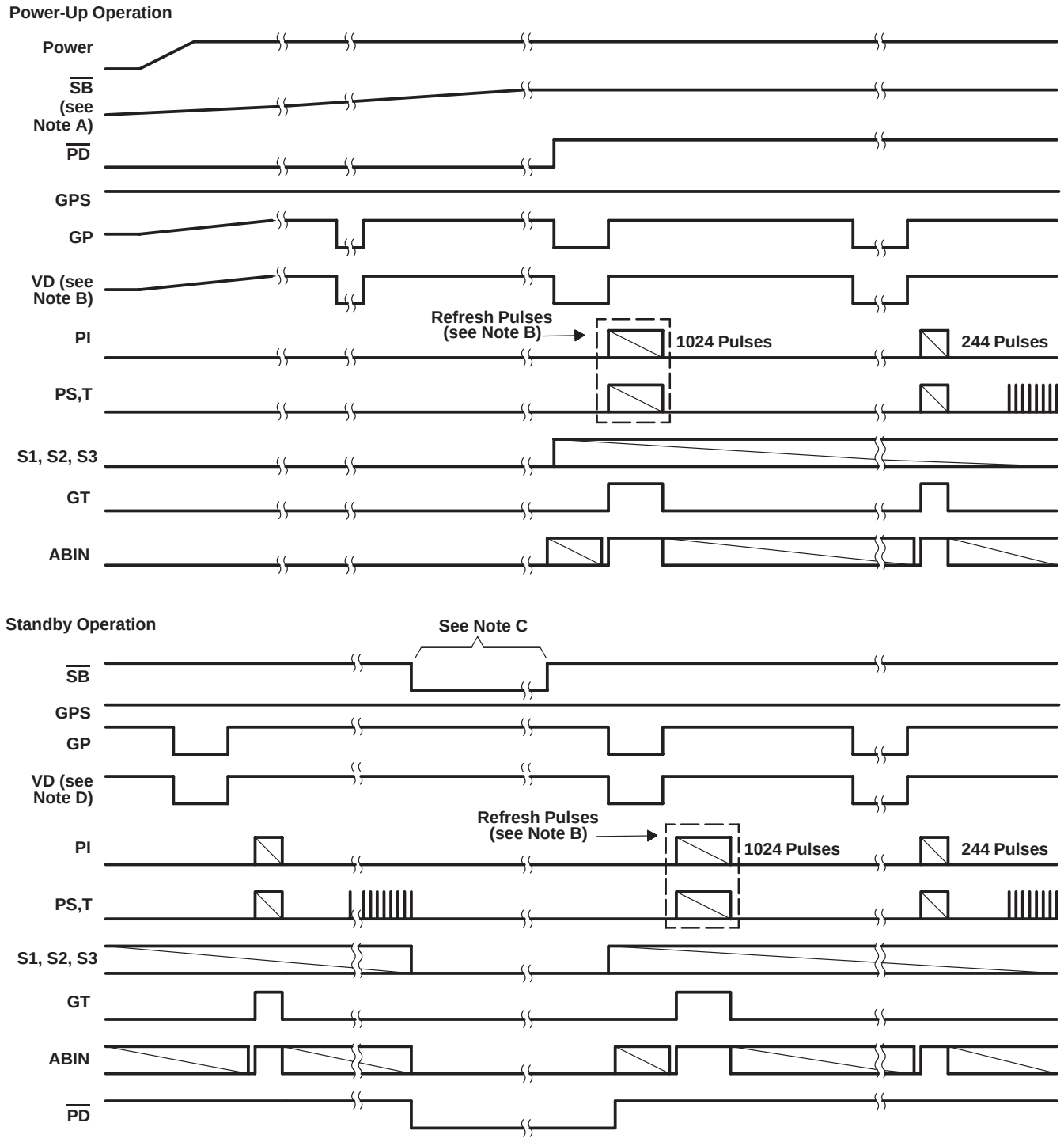


Figure 9. Power-Up and Standby Timing

NOTES: A. A 0.1-µF capacitor is connected between $\overline{SB}$ and GND.
B. In both powerup and standby operation, 1024 refresh pulses are generated on PI, PS, and T even if VD is not connected internally to GP.
C. When $\overline{SB}$ is low, ABIN, GT, $\overline{PD}$, PI, PS, S1, S2, S3, and T are all low.
D. VD is connected internally to GP (GPS is high).

PARAMETER MEASUREMENT INFORMATION

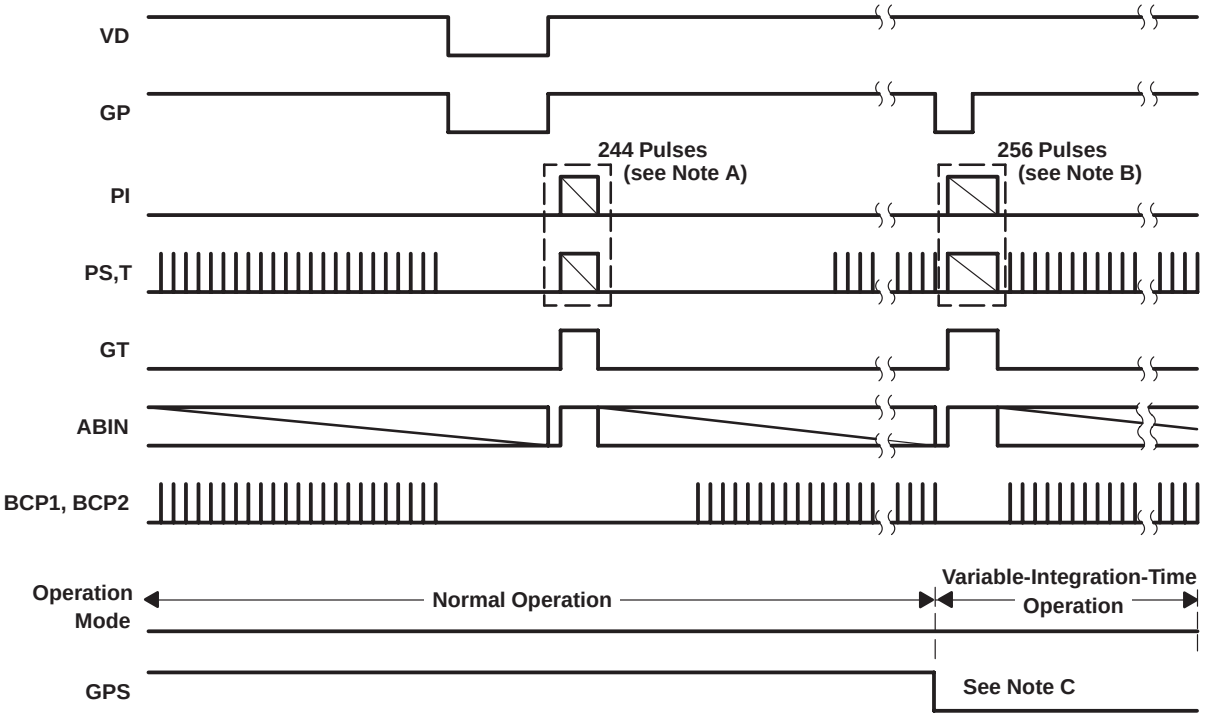


Figure 10. Timing – Normal Operation Versus Variable-Integration-Time Operation

NOTES: A. When VD is low and GP level changes from high to low, 244 pulses are generated on PI, PS, and T.
B. When GP goes low, 256 pulses are generated on PI, PS, and T.
C. Depending on the shutter design, GPS can either be held low or clocked during variable-integration-mode operation. If GPS is clocked, VD follows GP during the intervals in which GPS is high.

PARAMETER MEASUREMENT INFORMATION

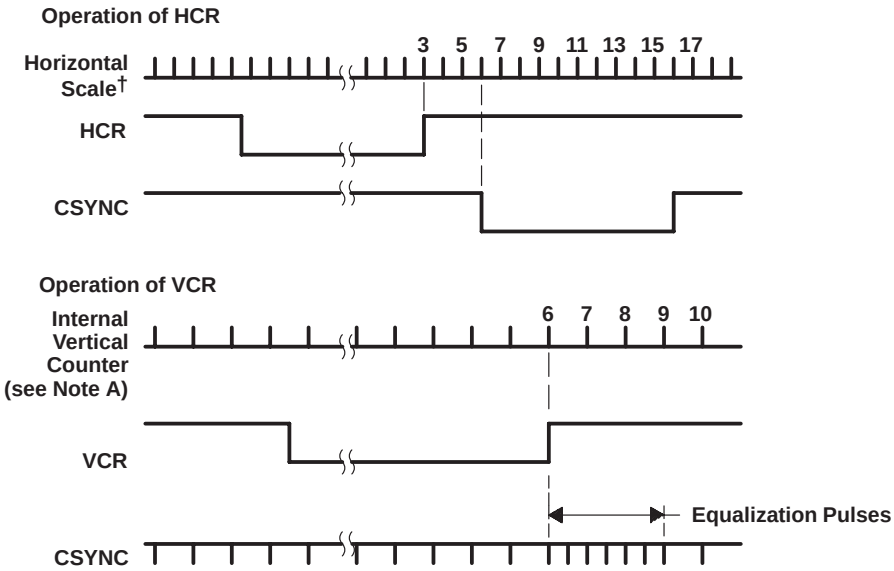


Figure 11. Horizontal and Vertical Reset Timing

† 130 intervals equals 63.55 µs equals one horizontal-scan line

NOTE A: The internal vertical counter is preset to the value 6 (indicating the end of vertical sync) when VCR transitions from low to high. Immediately following the low-to-high transition on VCR, horizontal scanning commences on line 7 of the frame.

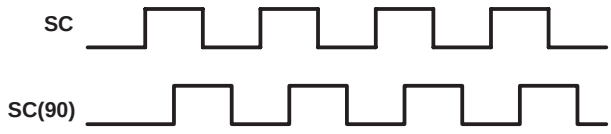
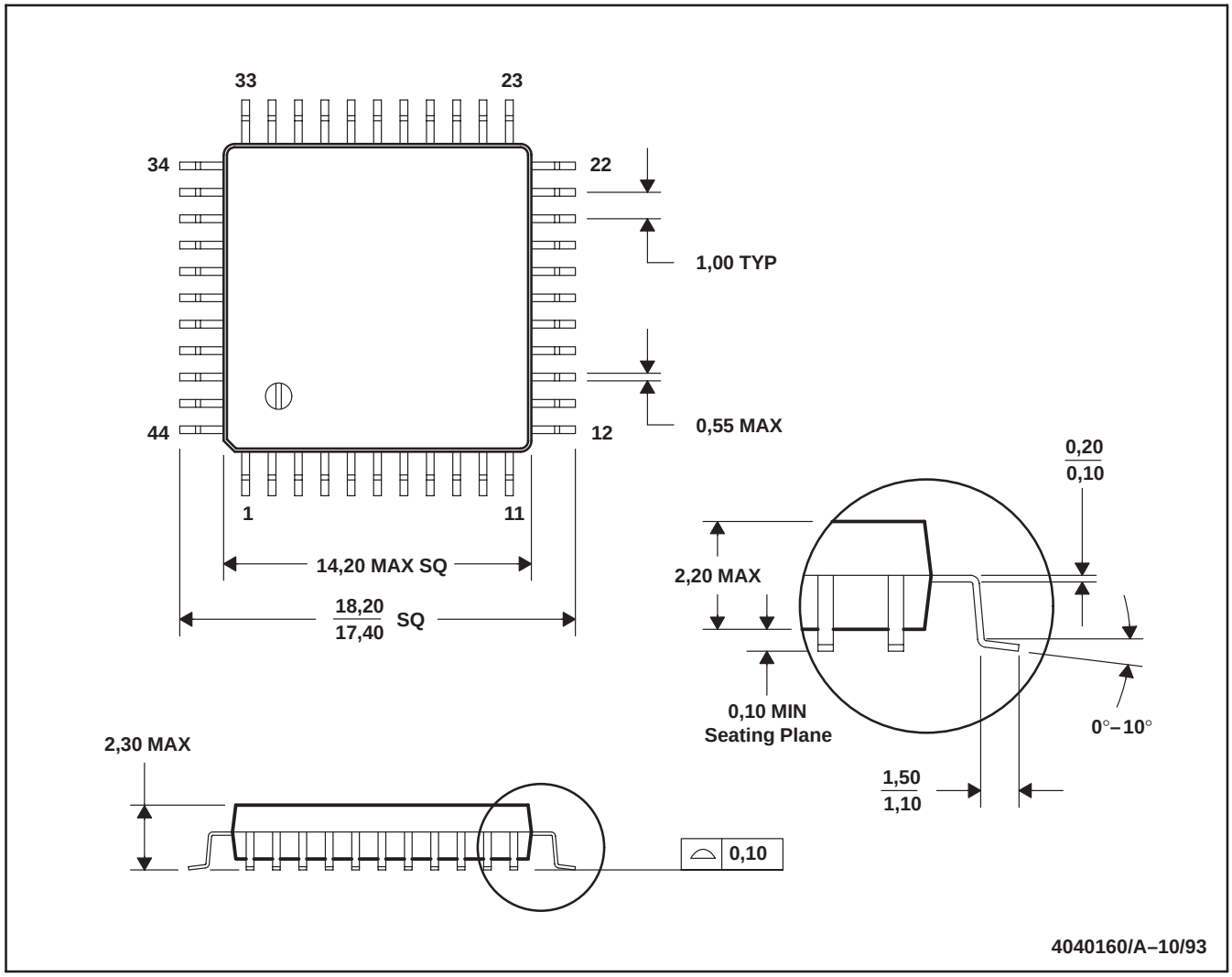


Figure 12. SC and SC(90) Timing

MECHANICAL DATA

FS/S-PQFP-G44 **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

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