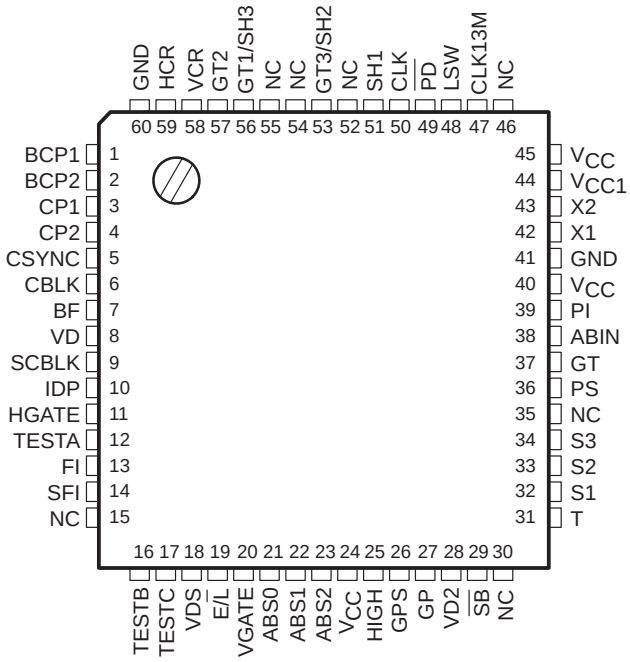
- **PAL-Timing Operation**
- **Solid-State Reliability**
- **Color and Monochrome Operation**
- **Five Selectable-Antiblooming Modes**
- **Variable-Integration-Time Option**
- **Surface-Mount Package**
- **Clamp-Pulse Select Option**
- **Horizontal and Vertical Resets for External Synchronization**

FS PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN28837 is a monolithic integrated circuit designed to supply timing signals for the Texas Instruments (TI™) 8-mm-diagonal TC276 (PAL color) and TC277 (PAL monochrome) CCD image sensors. The SN28837 supplies both CCD-drive signals and PAL-television synchronization signals at standard video rates. It requires a single 5-V supply voltage and a 13.37-MHz crystal-oscillator input. The SN28837 provides the user with several options including multiple antiblooming modes, variable-integration time, external synchronization, clamp-pulse selection, and delayed horizontal transfer.

The SN28837 is designed to drive the CCD image sensor through intermediary level-shifting devices such as the TI TMS3473B parallel driver and the SN28846 serial driver. It also supplies sample-and-hold signals for the TI TL1593 3-channel sample-and-hold circuit and multiplex signals for the TI TL1051 video preprocessor. In color applications, the SN28837 interfaces with the SN28838 color-subcarrier generator to generate the PAL color subcarrier.

The SN28837 is supplied in a 60-pin plastic flat package and is characterized for operation from –20°C to 45°C.

This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, precautions should be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

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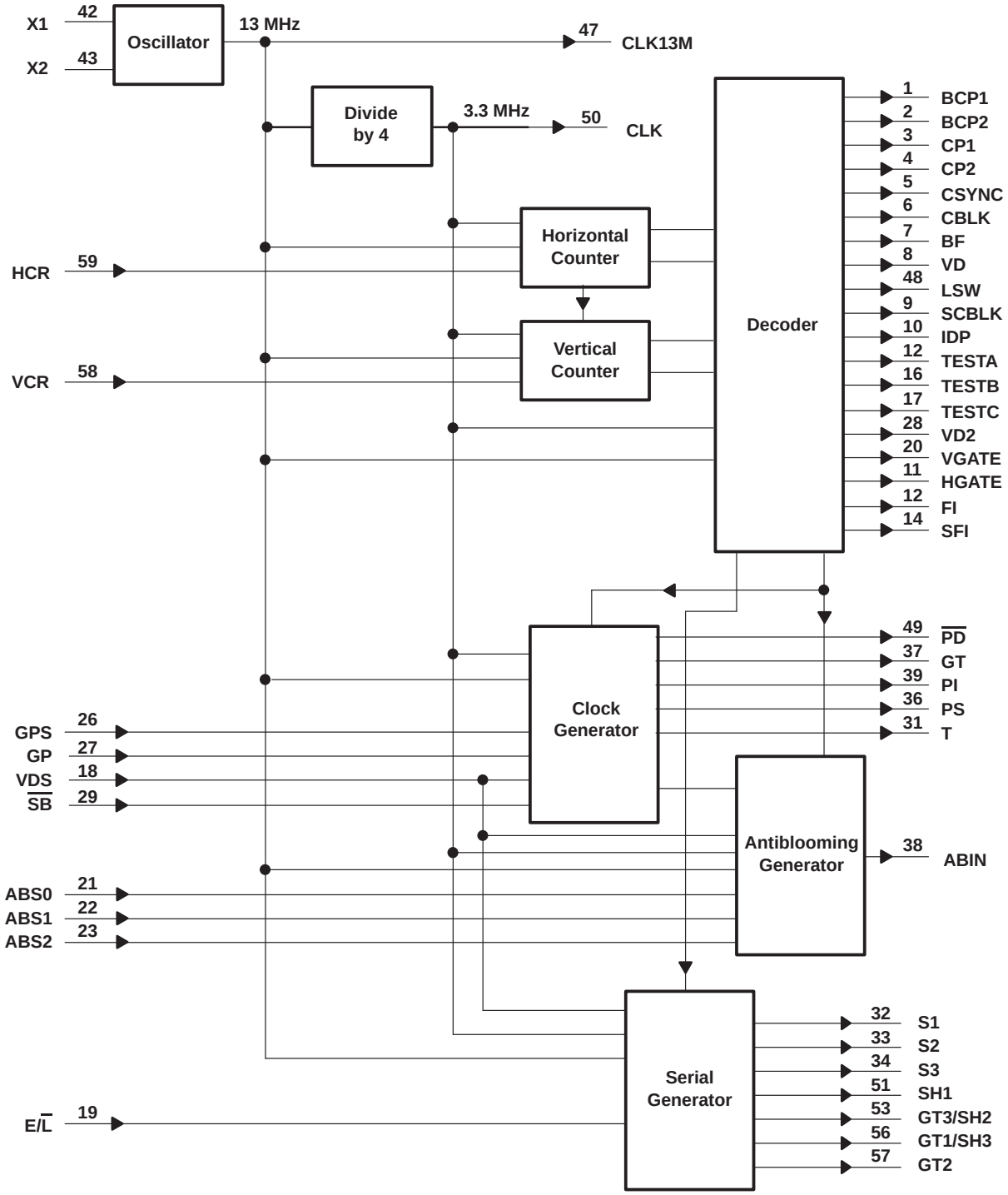
functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ABIN	38	O	Antiblooming in
ABS0	21	I	The levels on these three terminals determine which of the five antiblooming modes is selected: Mode 0: ABS2 NC, ABS1 L, ABS0 L — No ABG pulses Mode 1: ABS2 NC, ABS1 H, ABS0 L — 2-MHz burst of ABG pulses Mode 2: ABS2 NC, ABS1 L, ABS0 H — 1-MHz burst of ABG pulses Mode 3: ABS2 H, ABS1 H, ABS0 H — 1-MHz continuous ABG pulses Mode 4: ABS2 L, ABS1 H, ABS0 H — 2-MHz continuous ABG pulses Mode 1 is used for normal operation.
ABS1	22	I	
ABS2	23	I	
BCP1	1	O	Optical black clamp
BCP2	2	O	Optical black clamp
BF	7	O	Burst flag
CBLK	6	O	Composite blank
CLK	50	O	3.34-MHz clock (factory-test point)
CLK13M	47	O	13-MHz clock (connect to SN28838 color-subcarrier generator for color operation)
CP1	3	O	Clamp 1 (signal processing)
CP2	4	O	Clamp 2 (signal processing)
CSYNC	5	O	Composite sync
E/$\overline{L}$	19	I	Delay select for S1, S2, S3. When E/$\overline{L}$ is high, the three serial-transfer pulses occur early relative to the sample-and-hold pulses SH1, SH2, and SH3. When E/$\overline{L}$ is low, the three serial-transfer pulses occur late relative to the sample-and-hold pulses.
FI	13	O	Field index
GND	41, 60		Ground
GP	27	I	Exposure control: GP gates the PS and PI outputs (see the description of GPS)
GPS	26	I	When GPS is high, the timer operates in the normal-integration-time mode (t_{int} = 20 ms) and VD is connected internally to GP. To operate the imager in the variable-integration-time mode, GPS must be held low and a user-defined logic circuit must be inserted between VD and GP to vary the integration time (see Figure 1).
GT	37	O	TMS3473B parallel-driver MIDSEL input switch
GT1/SH3	56	O	GT1/SH3 is a logic signal for both Y gate 1 of the TL1051 video preprocessor and sample-and-hold channel 3 of the TL1593 3-channel sample-and-hold circuit.
GT2	57	O	Y gate 2 for the TL1051 video preprocessor
GT3/SH2	53	O	GT3/SH2 is a logic signal for both Y gate 3 of the TL1051 video preprocessor and sample-and-hold channel 2 of the TL1593 3-channel sample-and-hold circuit.
HCR	59	I	Horizontal-counter reset
HGATE	11	O	Decoded H count signal. HGATE is a test point and is not used in normal operation.
HIGH	25	I	Not used (tie high)
IDP	10	O	ID pulse (for SECAM operation)
LSW	48	O	Line switch (connect to SN28838 for color operation)
NC	15, 30, 35, 46, 52, 54, 55		No connect
$\overline{PD}$	49	O	Power down. A low-logic level on $\overline{PD}$ causes the device to enter a low power-consumption mode.
PI	39	O	Parallel-image-area gate clock
PS	36	O	Parallel-storage-area gate clock
$\overline{SB}$	29	I	Standby-mode select. When $\overline{SB}$ is high, normal operation is selected; when $\overline{SB}$ is low, the power-down mode is selected.
SCBLK	9	O	Subcarrier blank (for SECAM applications)

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
SFI	14	O	Second field index
SH1	51	O	Sample and hold 1
S1	32	O	Serial clock 1
S2	33	O	Serial clock 2
S3	34	O	Serial clock 3
T	31	O	Transfer-gate clock
TESTA	12	O	Test A (factory-test point)
TESTB	16	O	Test B (factory-test point)
TESTC	17	O	Test C (factory-test point)
V_{CC}	24, 40, 45		DC power
VCC1	44		Oscillator power
VCR	58	I	Vertical-counter reset
VD	8	O	Vertical drive
VDS	18	I	Vertical-dump speed. When VDS is high, the vertical-dump frequency is 3.3 MHz; when VDS is low, the vertical-dump frequency is 2 MHz.
VD2	28	O	Real-display-area signal. VD2 is a test point and is not used in normal operation.
VGATE	20	O	Decoded V count signal. VGATE is a test point and is not used in normal operation.
X1	42		Crystal oscillator (see Figure 2)
X2	43		

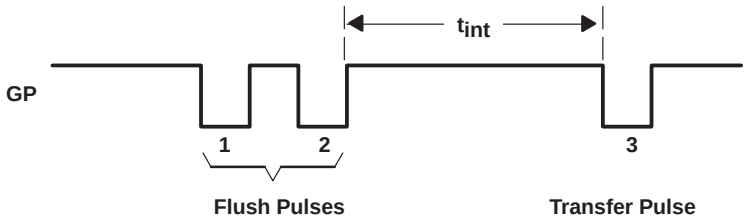


Figure 1. GP Flush and Transfer Pulses

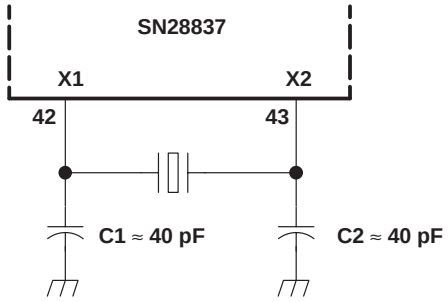
variable-integration-time mode

In addition to the normal TV mode of operation, the SN28837 timing generator offers an optional variable-integration mode for use with the TC276 and TC277 CCD area-array image sensors. The variable-integration mode is selected by applying a low-logic level to GPS. This low-logic level disables the vertical-drive (VD) signal from controlling, internal to the timer, the image-area and storage-area parallel transfer signal (GP).

Prior to the start of a new integration period, the charge that has accumulated in the image area must be transferred out. To flush this previous signal or dark-current charge from the image area, GP is pulsed low two times. Each low pulse generates 302 pulses image-area and storage-area gate and transfer signals that shift the unwanted charge into the clearing drain. This clearing function should be performed during the high time of the VD signal (see Figure 3 through Figure 13).

The new integration period continues as long as GP remains high. GPS must be held at a low-logic level to prevent VD from controlling GP internally. The integration ceases and the readout occurs when VD and GP are pulsed low simultaneously; this is accomplished by taking GPS to a high-logic level. The readout timing is dependent on the vertical-drive pulse; this means that the total-integration time is a multiple of 1/50 of a second plus the time interval between the last GP low pulse and the next VD low pulse. The image readout occurs within the normal 1/50-second readout interval. If the integration time is less than 1/50 of a second, normal output operation occurs; if the integration time is greater than 1/50 of a second, a frame buffer may be required to capture the image.

Integration times greater than 1/50 of a second result in image degradation at temperatures greater than 25°C due to dark-current generation. The degradation is seen as a decrease in dynamic range (contrast) and an increase in noise. It is recommended that the image sensor be cooled for long-exposure operation. The dark-current generation is reduced by a factor of two for each 7°C temperature decrease. The sensor operates at –30°C. Cooling can be accomplished by using a thermoelectric or Peltier cooler attached to the image sensor. Condensation on the header must be prevented by isolating the cooled sensor from moist air. Vacuum isolation is preferred; however, the continual flushing of dry nitrogen across the header can also prevent condensation.



NOTE: The SN28837 is designed for use with a crystal oscillator. The X1 and X2 terminals should not connect directly to external driver outputs.

Figure 2. Connection of an External Crystal Oscillator to the SN28837

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) . . . . . –0.3 V to 7 V
Input voltage range, V_I . . . . . –0.3 V to V_{DD} + 0.3 V
Output voltage range, V_O . . . . . –0.3 V to V_{DD} + 0.3 V
Continuous total power dissipation at (or below) T_A = 25°C . . . . . 300 mW
Operating free-air temperature range, T_A . . . . . –20°C to 45°C
Storage temperature range, T_{STG} . . . . . –55°C to 125°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5	5	5.5	V
High-level input voltage, V_{IH}	V_{DD} x 0.7			V
Low-level input voltage, V_{IL}			0.8	V
Operating frequency		13.375		MHz
Power-up time		300		µs
Operating free-air temperature, T_A	–20		45	°C

electrical characteristics over recommended operating ranges of supply voltage and free-air temperature (unless otherwise noted)‡

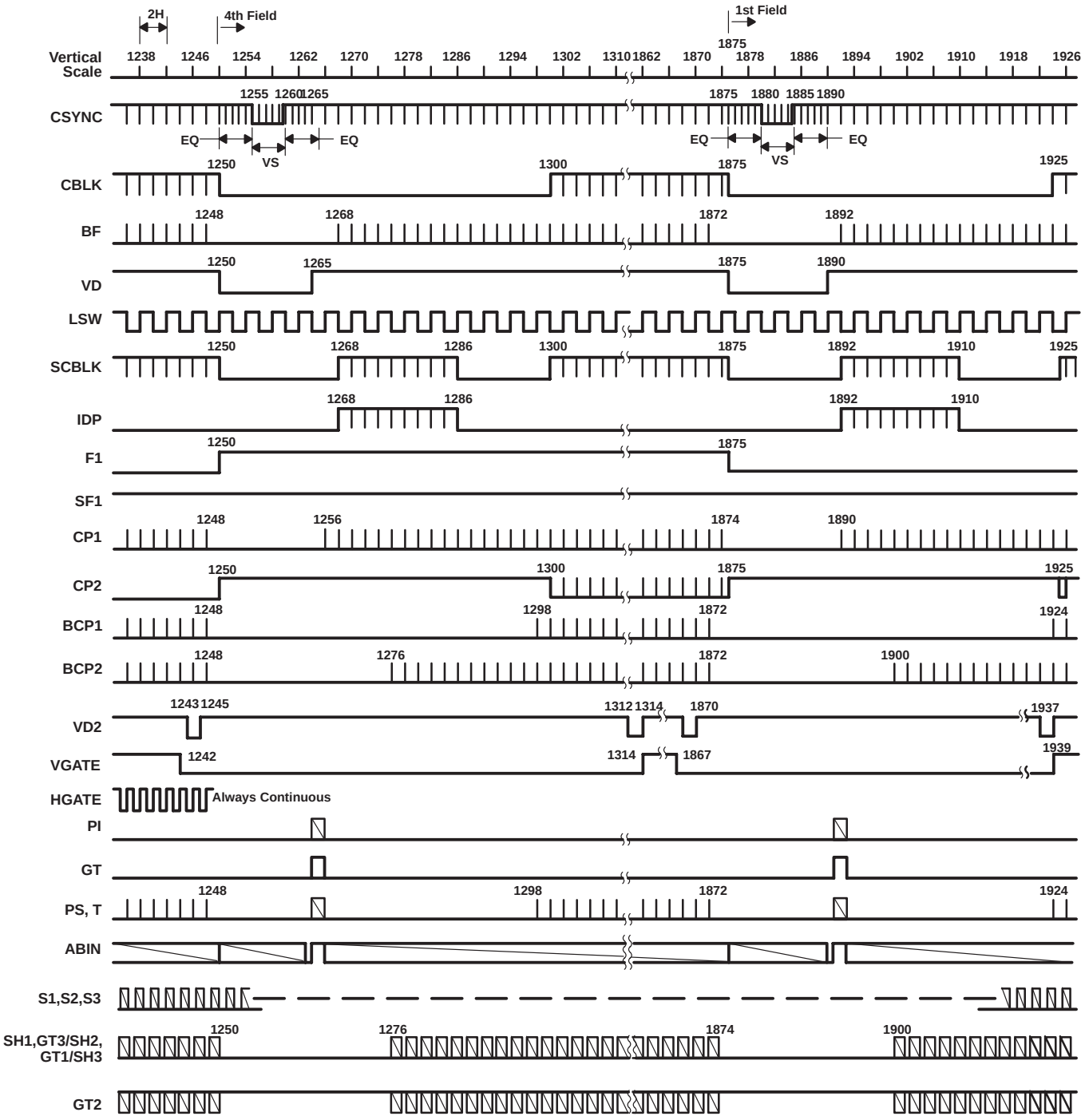
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	GT3/SH2 and GT1/SH3	V_{DD} = 4.5 V,	I_{OH} = –4 mA	3.5			V
	All other outputs	V_{DD} = 4.5 V,	I_{OH} = –2 mA	3.5			
V_{OL}	GT3/SH2 and GT1/SH3	V_{DD} = 4.5 V,	I_{OL} = 4 mA			0.5	V
	All other outputs	V_{DD} = 4.5 V,	I_{OL} = 2 mA			0.5	
I_{IH}§		V_{IH} = 5 V				1	µA
I_{IL}		V_{IL} = 0		–30	–200	–500	µA
$I_{DD(AV)}$	Average supply current				10	30	mA
$I_{DD(S)}$	Standby supply current				1		mA

‡ The HCR, $\overline{SB}$, and VCR inputs are Schmitt-trigger inputs with 0.1-V to 1-V hysteresis.

§ All inputs except X1 have pullup-current sources.

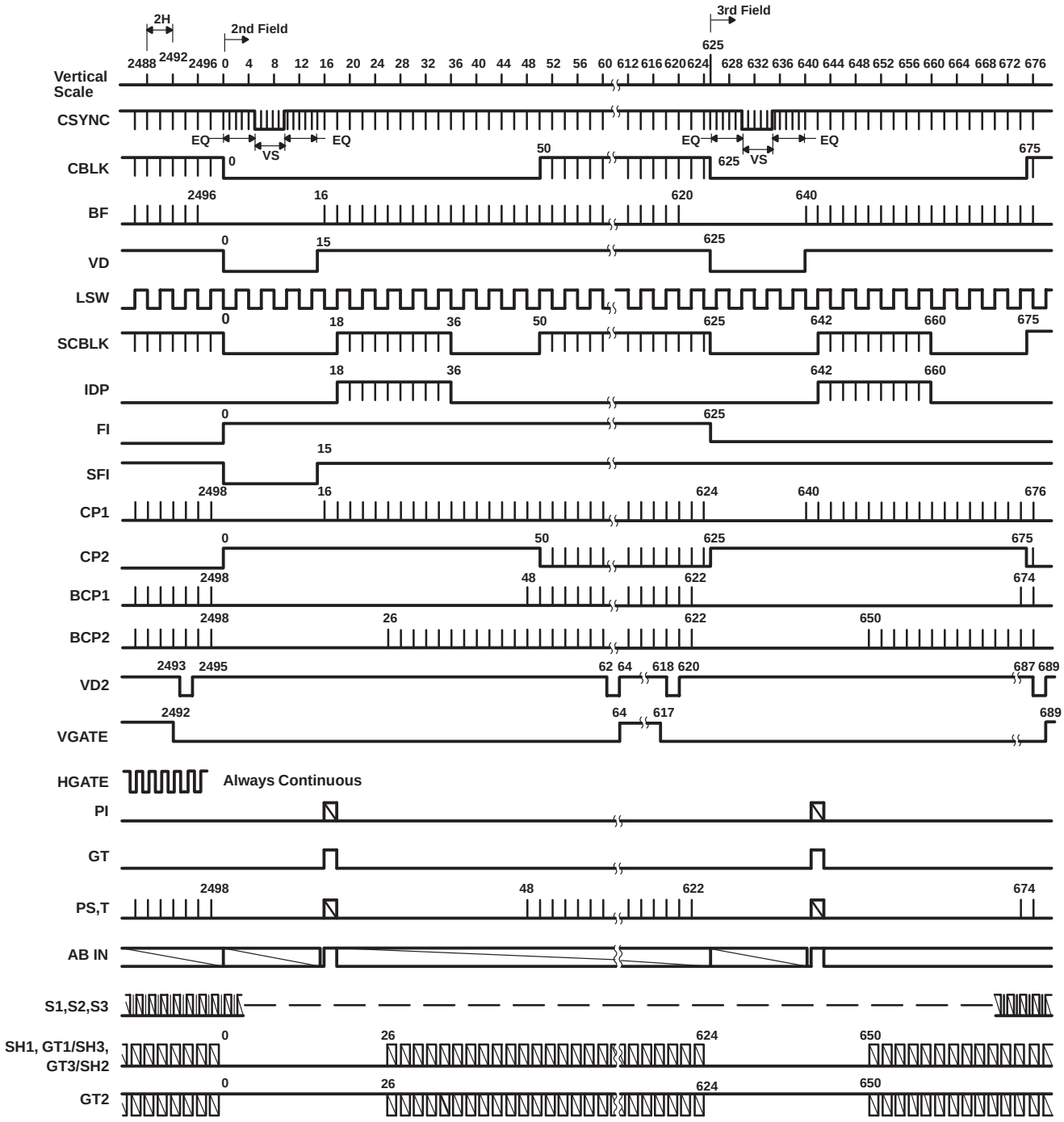
switching characteristics over recommended operating free-air temperature range, V_{DD} = 5 V

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Frequency	S1, S2, S3, SH1, GT2, GT1/SH3, GT3/SH2	C_L = 50 pF		4.458333		MHz
t_w	Pulse duration	S1, S2, S3, SH1, GT2, GT1/SH3, GT3/SH2			75		ns
t_r	Rise time	GT1/SH3 and GT3/SH2	C_L = 50 pF		10		ns
		All other outputs			50		
t_f	Fall time	GT1/SH3 and GT3/SH2			10		ns
		All other outputs			50		



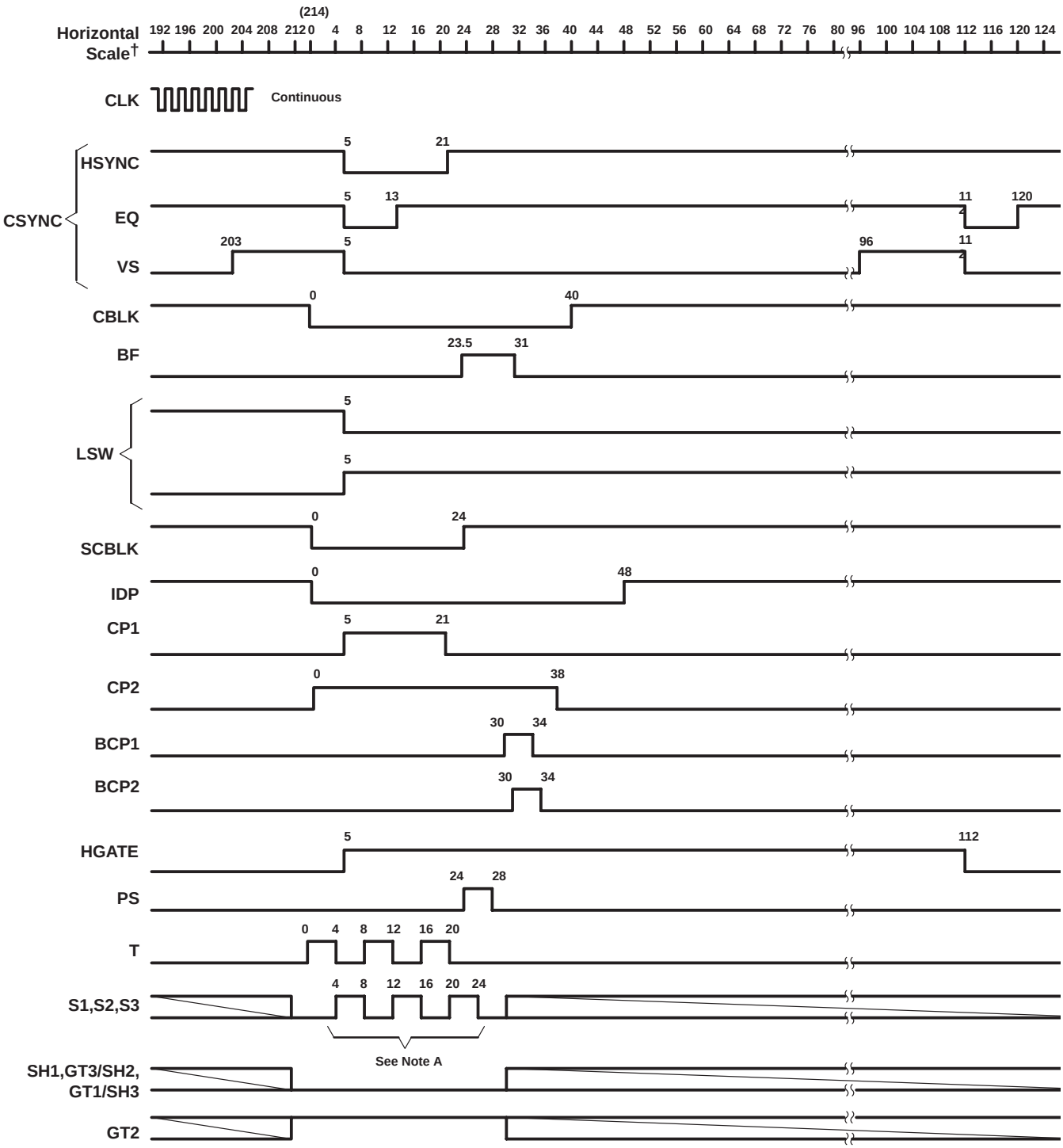
NOTES: A. GPS is low and VD is fed back to GP.
B. When GPS is high, VGATE is always low.
C. 1 field = 312 1/2 horizontal lines = 625 vertical counts. 1 frame = 625 horizontal lines = 1250 vertical counts. Period of each count of vertical counter = 32 μs.

Figure 3. Vertical Timing (First and Fourth Fields)



NOTES: A. GPS is low and VD is fed back to GP.
B. When GPS is high, VGATE is always low.
C. 1 field = 312 1/2 horizontal lines = 625 vertical counts. 1 frame = 625 horizontal lines = 1250 vertical counts. Period of each count of vertical counter = 32 μs.

Figure 4. Vertical Timing (Second and Third Fields)

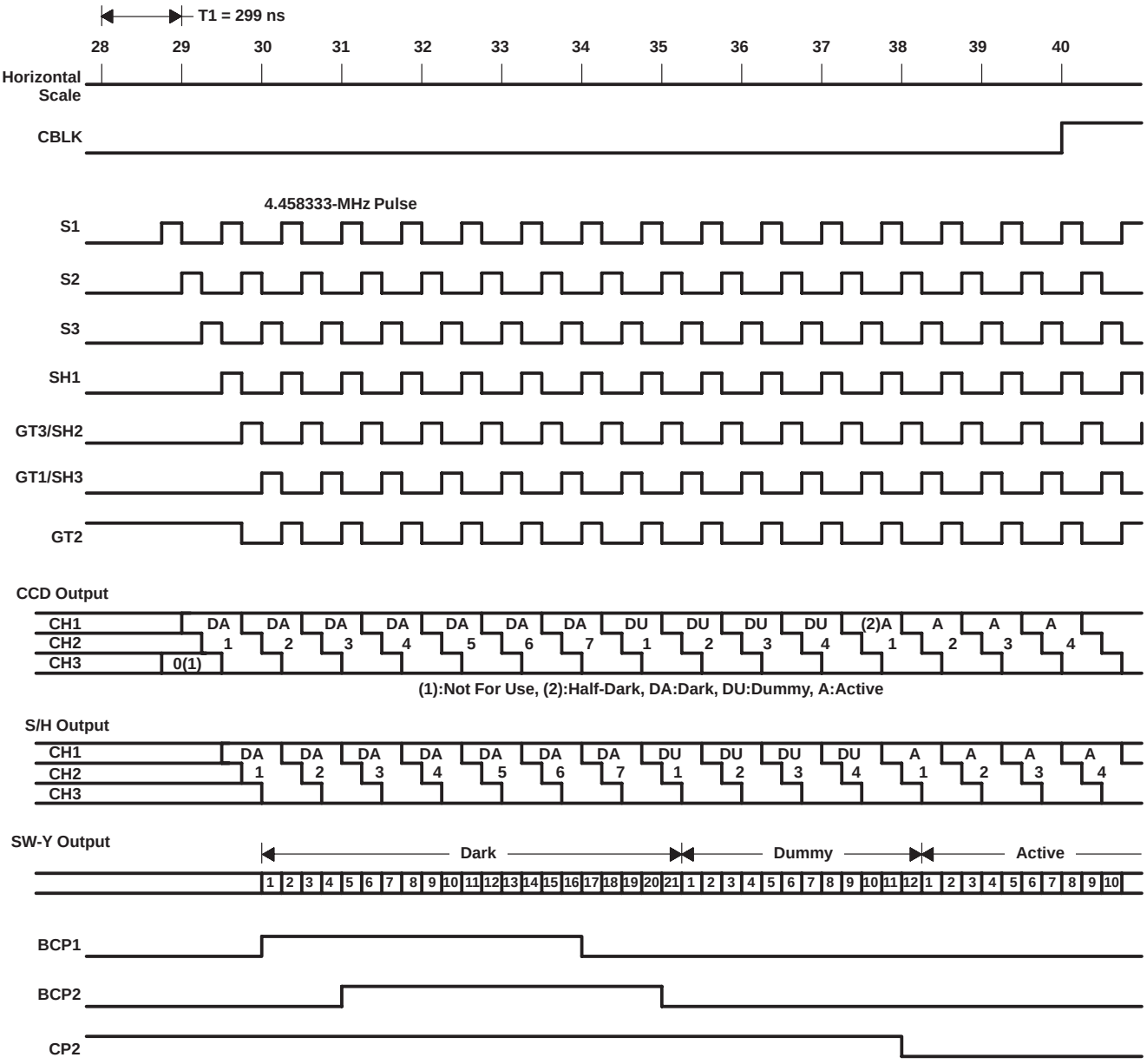


† For the horizontal scale (T1 clock), one interval = 299 ns ≥ 4 master-clock periods.

NOTES: A. Although S1, S2, and S3 appear to be coincident, S1 leads S2 by t5 ns, and S2 leads S3 by 75 ns between 4 and 24 on the horizontal scale.

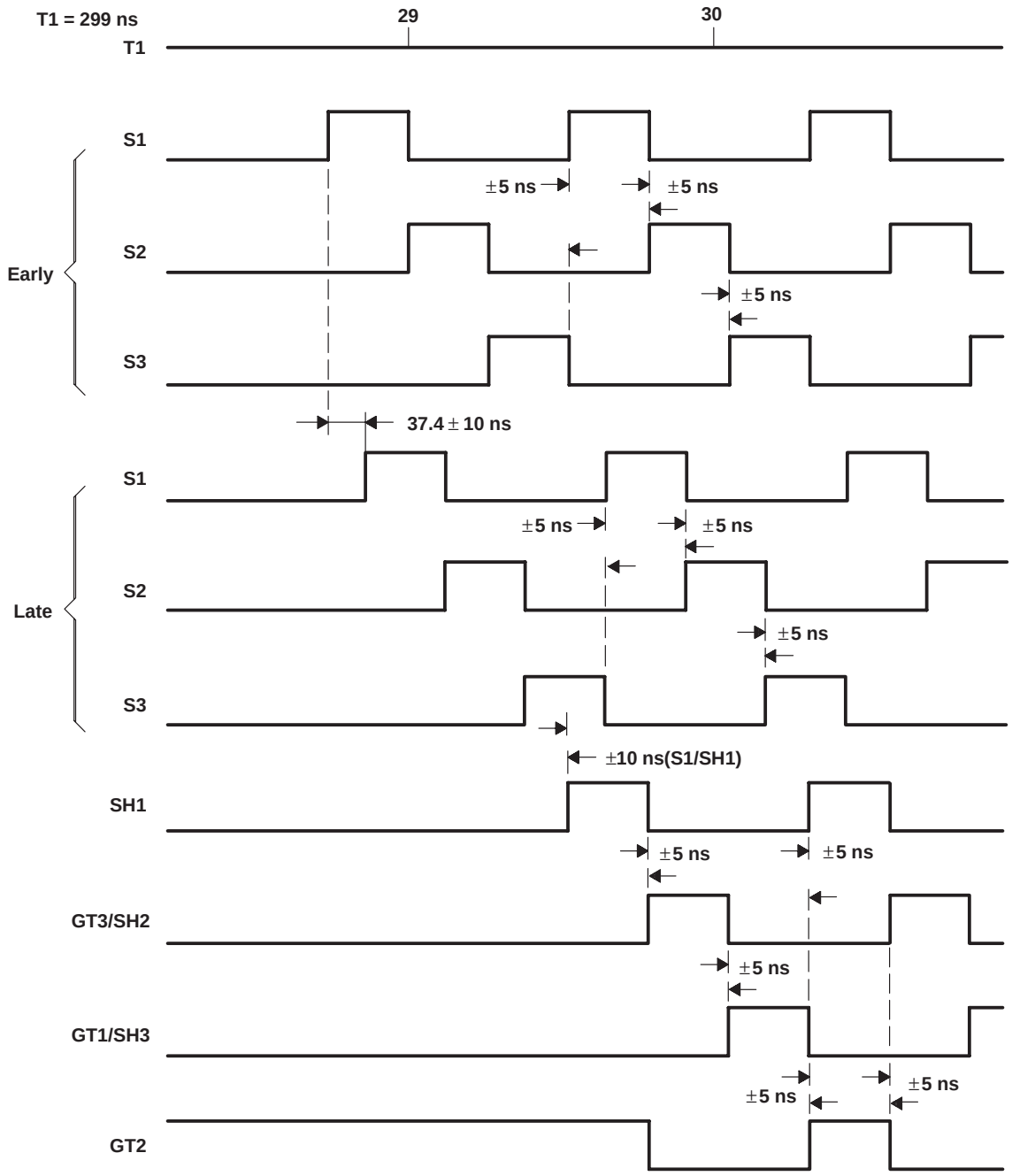
B. 1 TV line = 64 μs = 214 horizontal clocks

Figure 5. Horizontal Timing



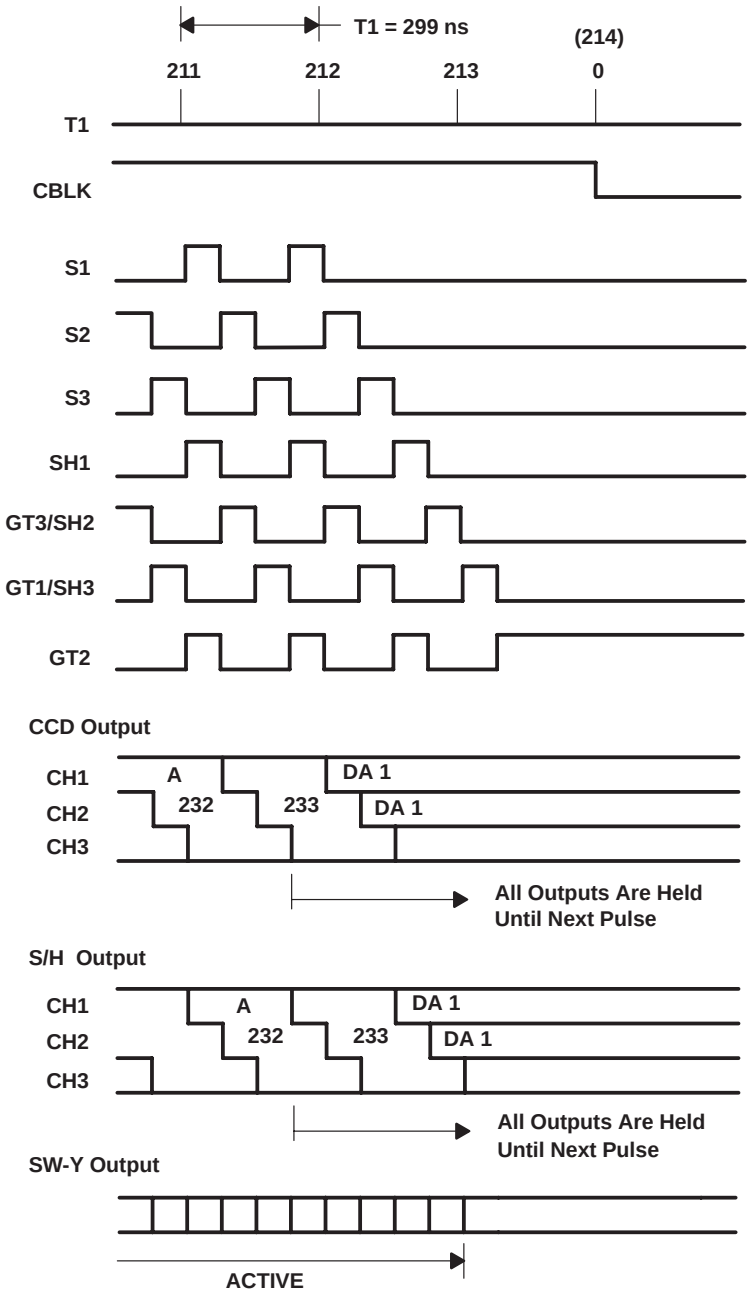
NOTE A: This chart shows early mode only. Late mode is shown in Figure 7.

Figure 6. S, SH, GT Timing (Start of H)



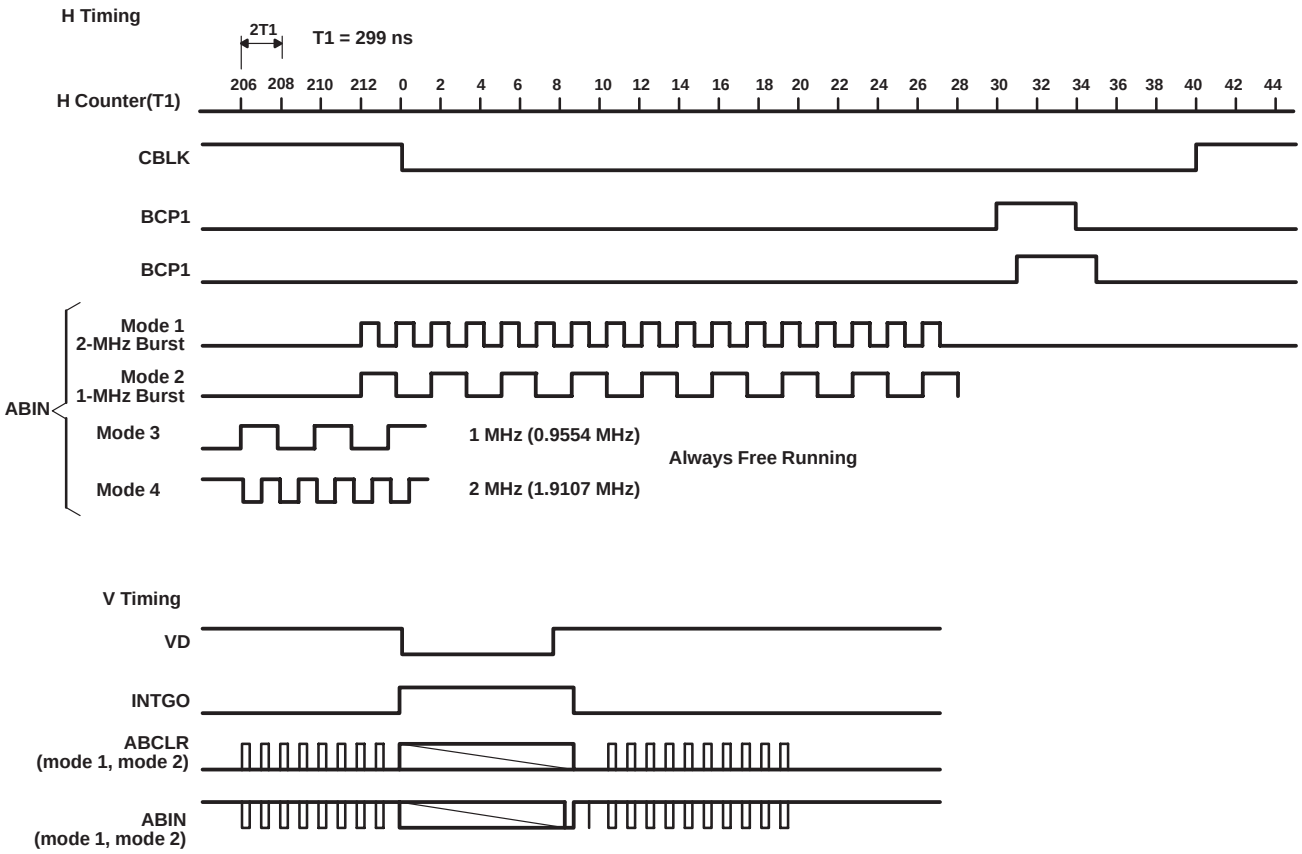
NOTE A: S1, S2, S3, SH1, GT3/SH2, GT1/SH3, GT2 are:
Cycle time = 224.3 ns
Pulse width = 74.8 ns
Duty cycle = 1/3

Figure 7. S, SH, GT Waveforms



NOTE A: This chart shows early mode only. Late mode is shown in Figure 7.

Figure 8. S, SH, GT Timing (End of H)

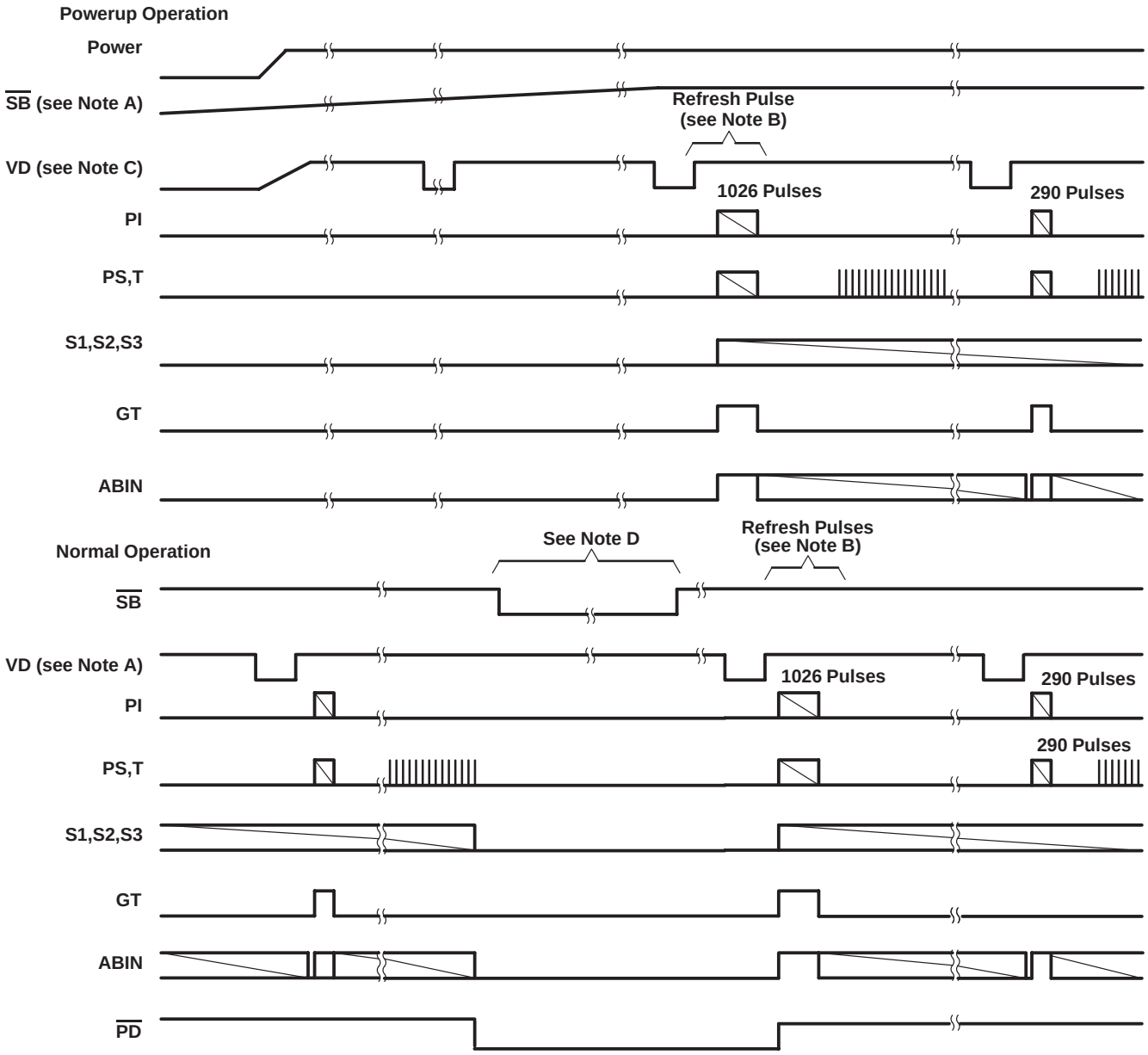


ANTIBLOOMING MODE SELECTION				
MODE	**ABS0**	**ABS1**	**ABS2**	**ABIN OUTPUT**
0	X	0	0	No ABG
1	X	1	0	2 MHz burst
2	X	0	1	1 MHz burst
3	1	1	1	1 MHz const
4	0	1	1	2 MHz const

X = Don't care

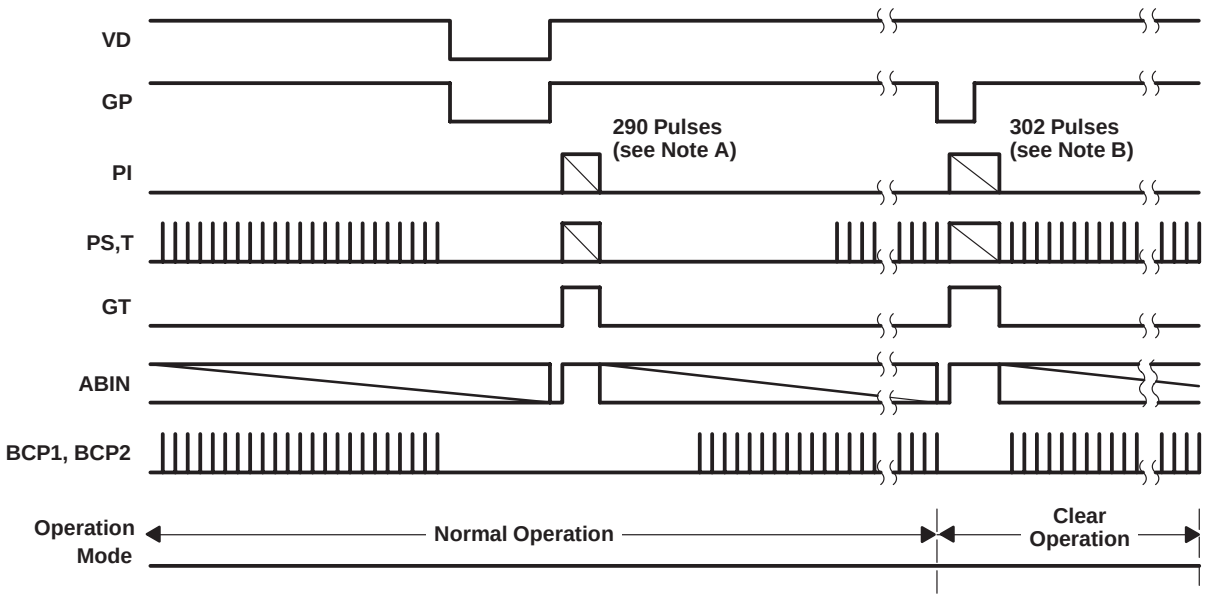
NOTES: A. For mode 1 and mode 4, duty cycle is 4/7 high and 3/7 low.
B. Only the timing from odd field to even field is shown. The timing from even field to odd field is the same as that for odd field to even field minus the H-to-V timing.
C. GPS is always high.

Figure 9. ABIN Timing



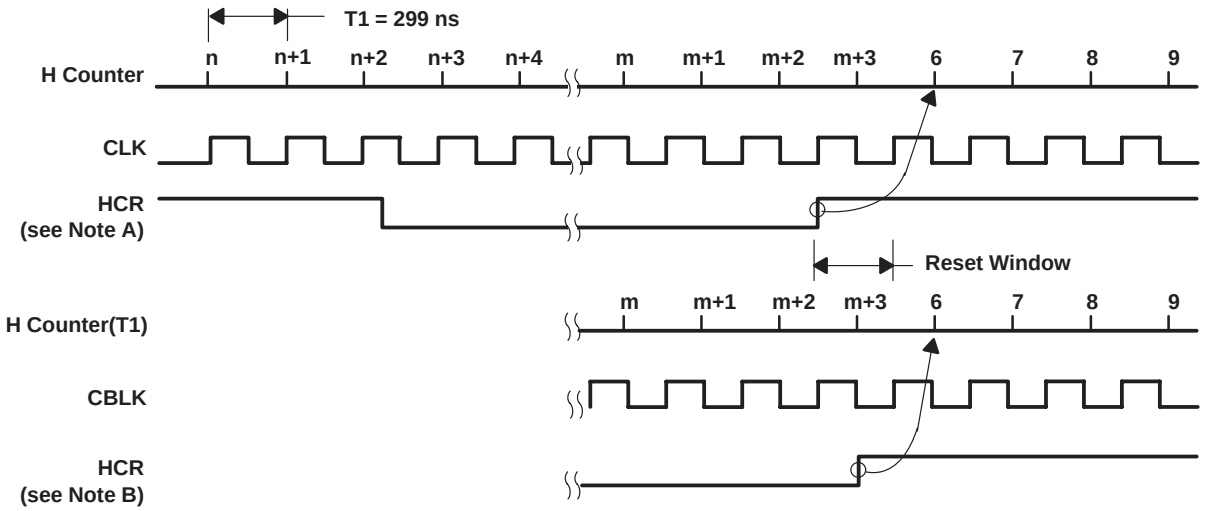
NOTES: A. A capacitor is connected to $\overline{SB}$ (between $\overline{SB}$ and GND).
B. Refresh pulses (1026 pulses) of PI, PS and T are generated even if VD is not fed back to GP.
C. VD is always fed back to GP and GPS is low.
D. PI, PS, S1, S2, S3, ABIN, and GT go low when $\overline{SB}$ is low.

Figure 10. Operation Chart of SB



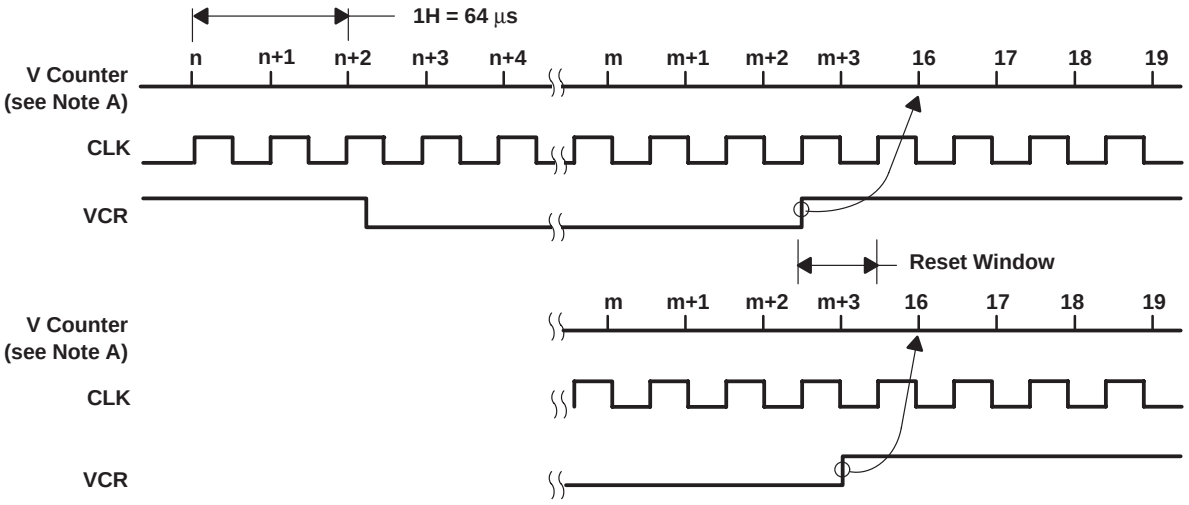
NOTES: A. When VD is low and GP goes low, 290 pulses are generated for PI, PS, and T after VD goes high.
B. When VD is high, GP goes low and 302 pulses are generated for PI, PS and T.
C. GPS is at a steady-state low level.

Figure 11. Normal Timing and Variable Integration



NOTES: A. The H counter is preset to the value 6 when HCR changes from low to high.
B. Output signals are changed one T1 clock after the change of the counter through the output latches.

Figure 12. Operation of HCR

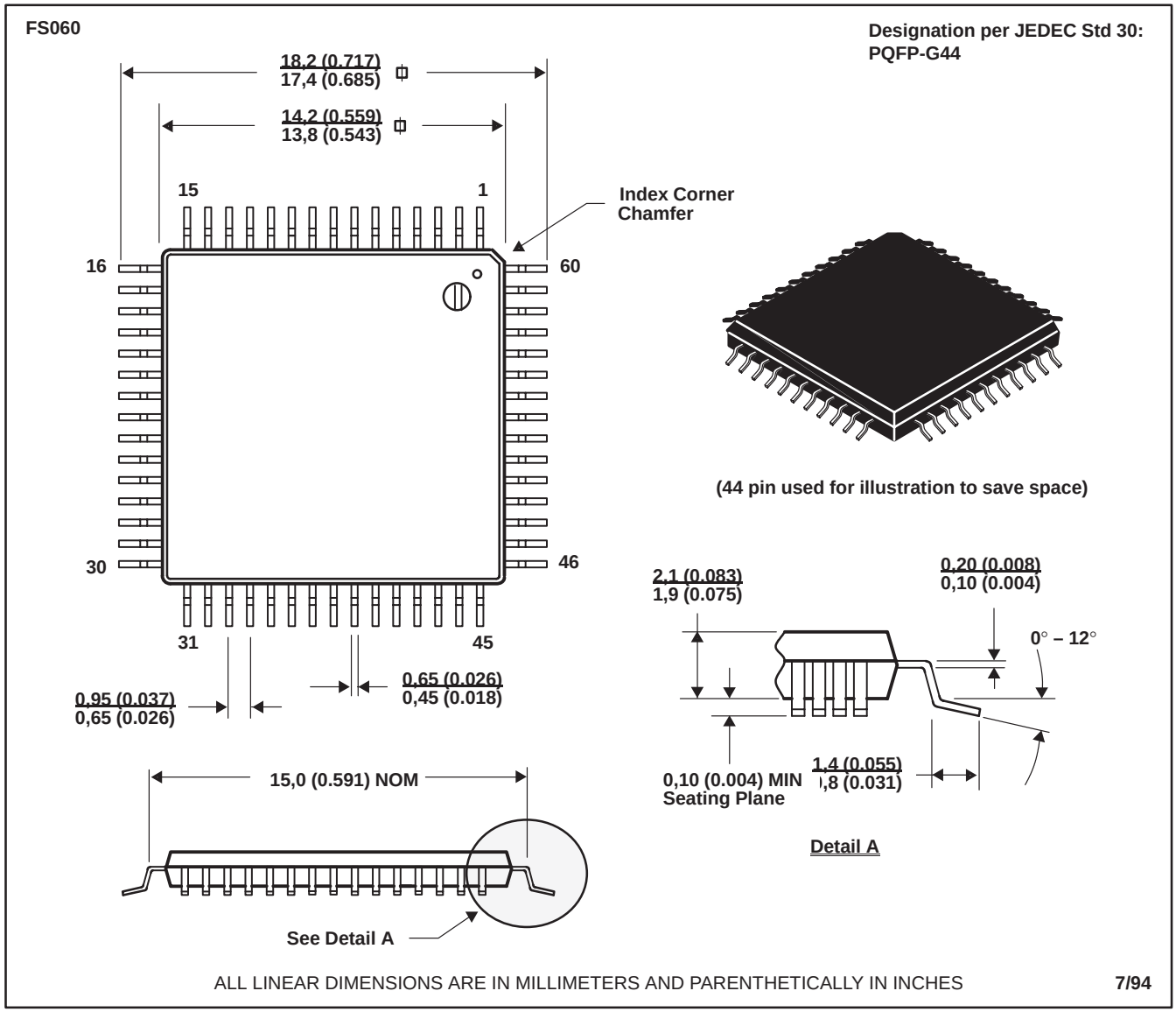


NOTE A: The V counter is preset to the value 16 when VCR changes from low to high.

Figure 13. Operation of VCR

MECHANICAL DATA

This plastic package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when operated in high-humidity conditions. The package is intended for surface mounting, and leads are spaced on 1,0-mm centers with a 0,8-mm foot length. Leads require no additional cleaning or processing when used in soldered assembly.



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