

# SN54AC373, SN74AC373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SCAS540C – OCTOBER 1995 – REVISED SEPTEMBER 2002

- 2-V to 6-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 6 V
- Max  $t_{pd}$  of 9.5 ns at 5 V
- 3-State Noninverting Outputs Drive Bus Lines Directly
- Full Parallel Access for Loading

## description/ordering information

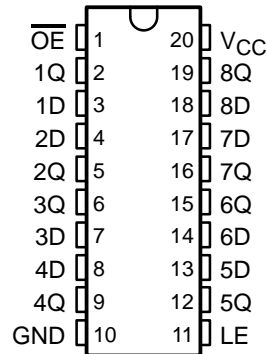
These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are D-type transparent latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

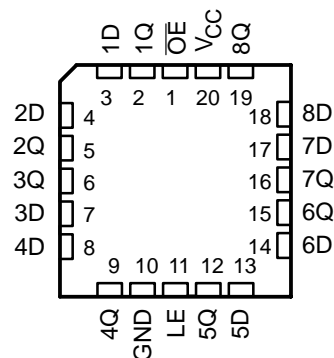
A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines in bus-organized systems without need for interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

SN54AC373 . . . J OR W PACKAGE  
SN74AC373 . . . DB, DW, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54AC373 . . . FK PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74AC373N	SN74AC373N
	SOIC – DW	Tube	SN74AC373DW	AC373
		Tape and reel	SN74AC373DWR	
	SOP – NS	Tape and reel	SN74AC373NSR	AC373
	SSOP – DB	Tape and reel	SN74AC373DBR	AC373
TSSOP – PW	Tape and reel	SN74AC373PWR	AC373	
-55°C to 125°C	CDIP – J	Tube	SNJ54AC373J	SNJ54AC373J
	CFP – W	Tube	SNJ54AC373W	SNJ54AC373W
	LCCC – FK	Tube	SNJ54AC373FK	SNJ54AC373FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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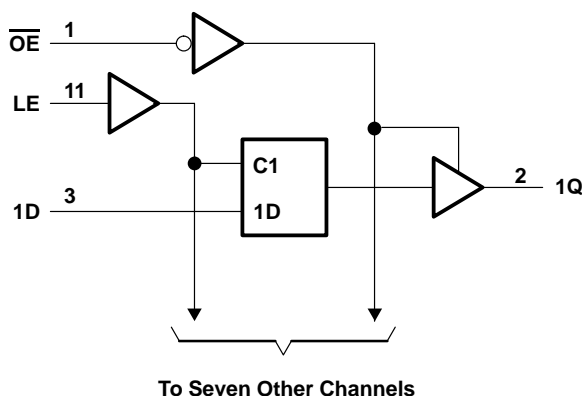
## description/ordering information (continued)

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE  
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND	$\pm 200$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
DB package	70°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
PW package	83°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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## recommended operating conditions (see Note 3)

		SN54AC373		SN74AC373		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	2	6	2	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 3 V		2.1	2.1	V
		V <sub>CC</sub> = 4.5 V		3.15	3.15	
		V <sub>CC</sub> = 5.5 V		3.85	3.85	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 3 V		0.9	0.9	V
		V <sub>CC</sub> = 4.5 V		1.35	1.35	
		V <sub>CC</sub> = 5.5 V		1.65	1.65	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 3 V		-12	-12	mA
		V <sub>CC</sub> = 4.5 V		-24	-24	
		V <sub>CC</sub> = 5.5 V		-24	-24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 3 V		12	12	mA
		V <sub>CC</sub> = 4.5 V		24	24	
		V <sub>CC</sub> = 5.5 V		24	24	
Δt/Δv	Input transition rise or fall rate			8	8	ns/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AC373		SN74AC373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	3 V	2.9			2.9		2.9	V	
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I <sub>OH</sub> = -12 mA	3 V	2.56			2.4		2.46		
		4.5 V	3.86			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	3 V				0.1		0.1	V	
		4.5 V				0.1		0.1		
		5.5 V				0.1		0.1		
	I <sub>OL</sub> = 12 mA	3 V				0.36		0.44		
		4.5 V				0.36		0.44		
		5.5 V				0.36		0.44		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1		μA	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25		±5		μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		80		μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V			4.5				pF	

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timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3 V \pm 0.3 V$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ C$		SN54AC373		SN74AC373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration, LE high	5.5		6.5		6		ns
$t_{su}$	Setup time, data before LE↓	5.5		6.5		6		ns
$t_h$	Hold time, data after LE↓	1		1		1		ns

timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5 V \pm 0.5 V$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ C$		SN54AC373		SN74AC373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration, LE high	4		5		4.5		ns
$t_{su}$	Setup time, data before LE↓	4		5		4.5		ns
$t_h$	Hold time, data after LE↓	1		1		1		ns

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 3.3 V \pm 0.3 V$  (unless otherwise noted) (see Figure 1)

PARAMETER	TO (INPUT)	TO (OUTPUT)	$T_A = 25^\circ C$			SN54AC373		SN74AC373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	D	Q	1.5	10	13.5	1	16.5	1.5	15	ns
$t_{PHL}$			1.5	9.5	13.0	1	16	1.5	14.5	
$t_{PLH}$	LE	Q	1.5	10	13.5	1	16.5	1.5	15	ns
$t_{PHL}$			1.5	9.5	12.5	1	15	1.5	14	
$t_{PZH}$	$\overline{OE}$	Q	1.5	9	11.5	1	14	1	13	ns
$t_{PZL}$			1.5	8.5	11.5	1	13.5	1	13	
$t_{PHZ}$	$\overline{OE}$	Q	1.5	10	12.5	1	16	1	14.5	ns
$t_{PLZ}$			1.5	8	11.5	1	13	1	12.5	

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5 V \pm 0.5 V$  (unless otherwise noted) (see Figure 1)

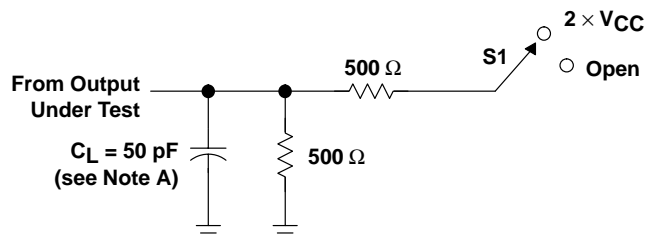
PARAMETER	TO (INPUT)	TO (OUTPUT)	$T_A = 25^\circ C$			SN54AC373		SN74AC373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	D	Q	1.5	7	9.5	1	11.5	1.5	10.5	ns
$t_{PHL}$			1.5	7	9.5	1	11.5	1.5	10.5	
$t_{PLH}$	LE	Q	1.5	7.5	9.5	1	12	1.5	10.5	ns
$t_{PHL}$			1.5	7	9.5	1	11	1.5	10.5	
$t_{PZH}$	$\overline{OE}$	Q	1.5	7	8.5	1	10.5	1	9.5	ns
$t_{PZL}$			1.5	6.5	8.5	1	10	1	9.5	
$t_{PHZ}$	$\overline{OE}$	Q	1.5	8	11	1	13.5	1	12.5	ns
$t_{PLZ}$			1.5	6.5	8.5	1	10.5	1	10	

operating characteristics,  $V_{CC} = 5 V, T_A = 25^\circ C$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50 pF, f = 1 MHz$	40	pF

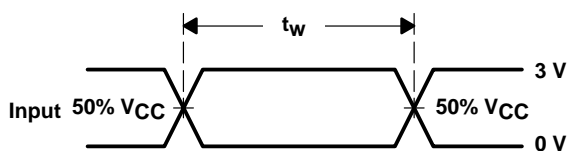


PARAMETER MEASUREMENT INFORMATION

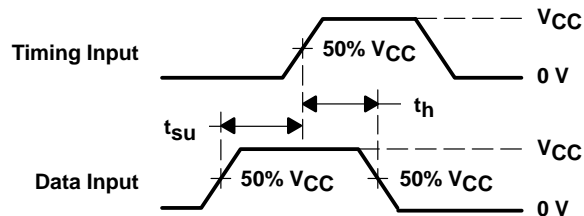


LOAD CIRCUIT

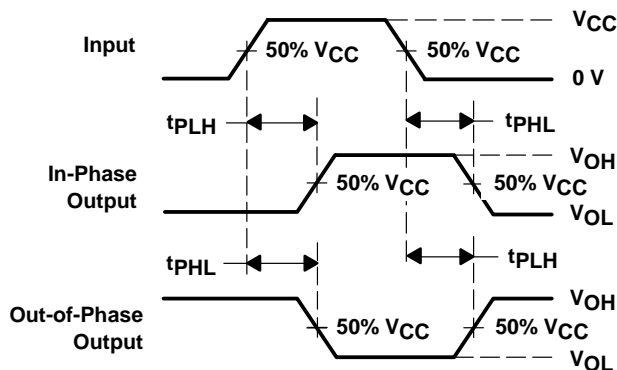
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	Open



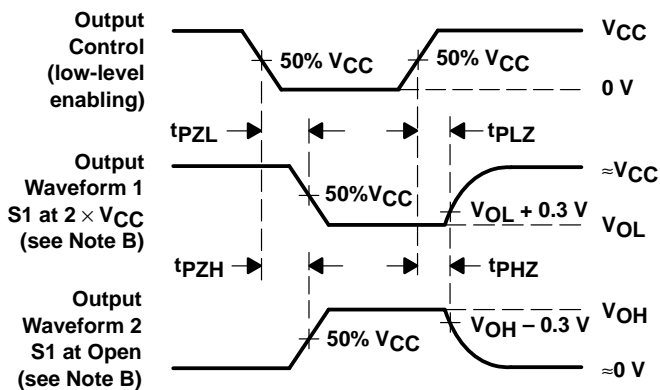
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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