

# SNx4AC574 Octal D-Type Edge-Triggered Flip-Flops with 3-State Outputs

## 1 Features

- Operation of 2V to 6V  $V_{CC}$
- Inputs accept voltages to 6V
- Max  $t_{pd}$  of 8.5ns at 5V
- 3-state outputs drive bus lines directly

## 2 Description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

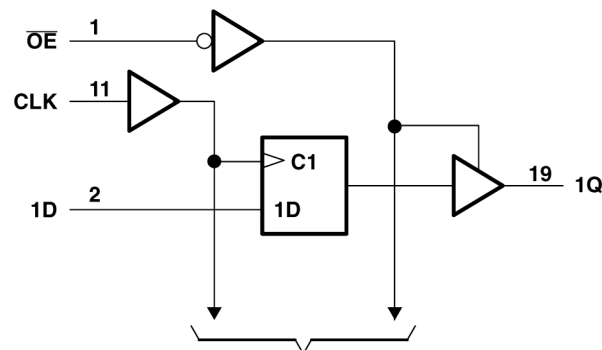
### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>	BODY SIZE <sup>(3)</sup>
SNx4AC574	DB (SSOP, 20)	7.2mm × 7.8mm	7.2mm × 5.30mm
	DW (SOIC, 20)	12.8mm × 10.3mm	12.80mm × 7.50mm
	N (PDIP, 20)	24.33mm × 9.4mm	24.33mm × 6.35mm
	PW (TSSOP, 20)	6.5mm × 6.4mm	6.50mm × 4.40mm

(1) For more information, see [Section 10](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.

(3) The body size (length × width) is a nominal value and does not include pins.



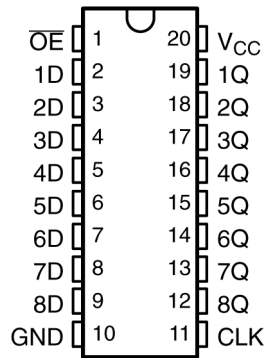
To Seven Other Channels  
**Logic Diagram (Positive Logic)**



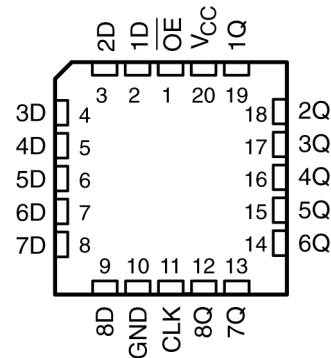
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### 3 Pin Configuration and Functions



**Figure 3-1. SN54AC574 J or W Package;  
SN74AC574 DB, DW, N, NS, or PW Package (Top  
View)**



**Figure 3-2. SN54AC574 FK Package (Top View)**

**Table 3-1. Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
OE	1	Input	Output enable for all channels, active low
D1	2	Input	Input for channel 1
D2	3	Input	Input for channel 2
D3	4	Input	Input for channel 3
D4	5	Input	Input for channel 4
D5	6	Input	Input for channel 5
D6	7	Input	Input for channel 6
D7	8	Input	Input for channel 7
D8	9	Input	Input for channel 8
GND	10	—	Ground
CLK	11	Input	Clock input for all channels, rising edge triggered
Q8	12	Output	Output for channel 8
Q7	13	Output	Output for channel 7
Q6	14	Output	Output for channel 6
Q5	15	Output	Output for channel 5
Q4	16	Output	Output for channel 4
Q3	17	Output	Output for channel 3
Q2	18	Output	Output for channel 2
Q1	19	Output	Output for channel 1
V <sub>CC</sub>	20	—	Positive supply
Thermal Pad		—	The thermal pad can be connect to GND or left floating. Do not connect to any other signal or supply.

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	7	V
V <sub>I</sub> <sup>(2)</sup>	Input voltage range	-0.5	V <sub>CC</sub> + 0.5	V
V <sub>O</sub> <sup>(2)</sup>	Output voltage range	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	(V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub> )		±20 mA
I <sub>OK</sub>	Output clamp current	(V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )		±20 mA
I <sub>O</sub>	Continuous output current	(V <sub>O</sub> = 0 to V <sub>CC</sub> )		±50 mA
Continuous current through V <sub>CC</sub> or GND				±200 mA
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 4.2 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		SN54AC574		SN74AC574		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	2	6	2	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 3 V	2.1	2.1		V
		V <sub>CC</sub> = 4.5 V	3.15	3.15		
		V <sub>CC</sub> = 5.5 V	3.85	3.85		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 3 V		0.9	0.9	V
		V <sub>CC</sub> = 4.5 V		1.35	1.35	
		V <sub>CC</sub> = 5.5 V		1.65	1.65	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 3 V		-12	-12	mA
		V <sub>CC</sub> = 4.5 V		-24	-24	
		V <sub>CC</sub> = 5.5 V		-24	-24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 3 V		12	12	mA
		V <sub>CC</sub> = 4.5 V		24	24	
		V <sub>CC</sub> = 5.5 V		24	24	
Δt/Δv	Input transition rise or fall rate		8		8	ns/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### 4.3 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SNx4AC574					UNIT	
	DB (SSOP)	DW (SOIC)	N (PDIP)	NS (SOP)	PW (TSSOP)		
	20 PINS						
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	70	101.2	69	60	126.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

### 4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AC574		SN74AC574		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	3 V	2.9			2.9		2.9	V	
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I <sub>OH</sub> = -12 mA	3 V	2.56			2.4		2.46		
		4.5 V	3.94			3.7		3.76		
		5.5 V	4.94			4.7		4.76		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	3 V			0.1		0.1	0.1	V	
		4.5 V			0.1		0.1	0.1		
		5.5 V			0.1		0.1	0.1		
	I <sub>OL</sub> = 12 mA	3 V			0.36		0.5	0.44		
		4.5 V			0.36		0.5	0.44		
		5.5 V			0.36		0.5	0.44		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1	±1	μA	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.5		±5	±2.5	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		80	40	μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V			4.5				pF	

### 4.5 Timing Requirements, V<sub>CC</sub> = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

		T <sub>A</sub> = 25°C		SN54AC574		SN74AC574		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency		75		55		60	MHz
t <sub>w</sub>	Pulse duration, CLK high or low		6		7.5		7	ns
t <sub>su</sub>	Setup time, data before CLK↑		2.5		6.5		3	ns
t <sub>h</sub>	Hold time, data after CLK↑		1.5		2.5		1.5	ns

#### 4.6 Timing Requirements, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

		$T_A = 25^\circ\text{C}$		SN54AC574		SN74AC574		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	95		85		85		MHz
$t_w$	Pulse duration, CLK high or low	4		5		5		ns
$t_{\text{su}}$	Setup time, data before CLK $\uparrow$	1.5		3.5		2		ns
$t_h$	Hold time, data after CLK $\uparrow$	1.5		2.5		1.5		ns

#### 4.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	TO (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN54AC574		SN74AC574		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			75	112		55		60	MHz	
$t_{\text{PLH}}$	CLK	Q	3.5	8.5	13.5	1	16.5	3.5	15	ns
$t_{\text{PHL}}$			3.5	7.5	12	1	15	3.5	13.5	
$t_{\text{PZH}}$	$\overline{\text{OE}}$	Q	2.5	7	11	1	13	2.5	12	ns
$t_{\text{PZL}}$			3	6.5	10.5	1	12.5	3	11.5	
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	Q	3.5	7.5	12	1	14	2.5	13	ns
$t_{\text{PLZ}}$			2	5.5	9	1	10.5	1.5	10	

#### 4.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

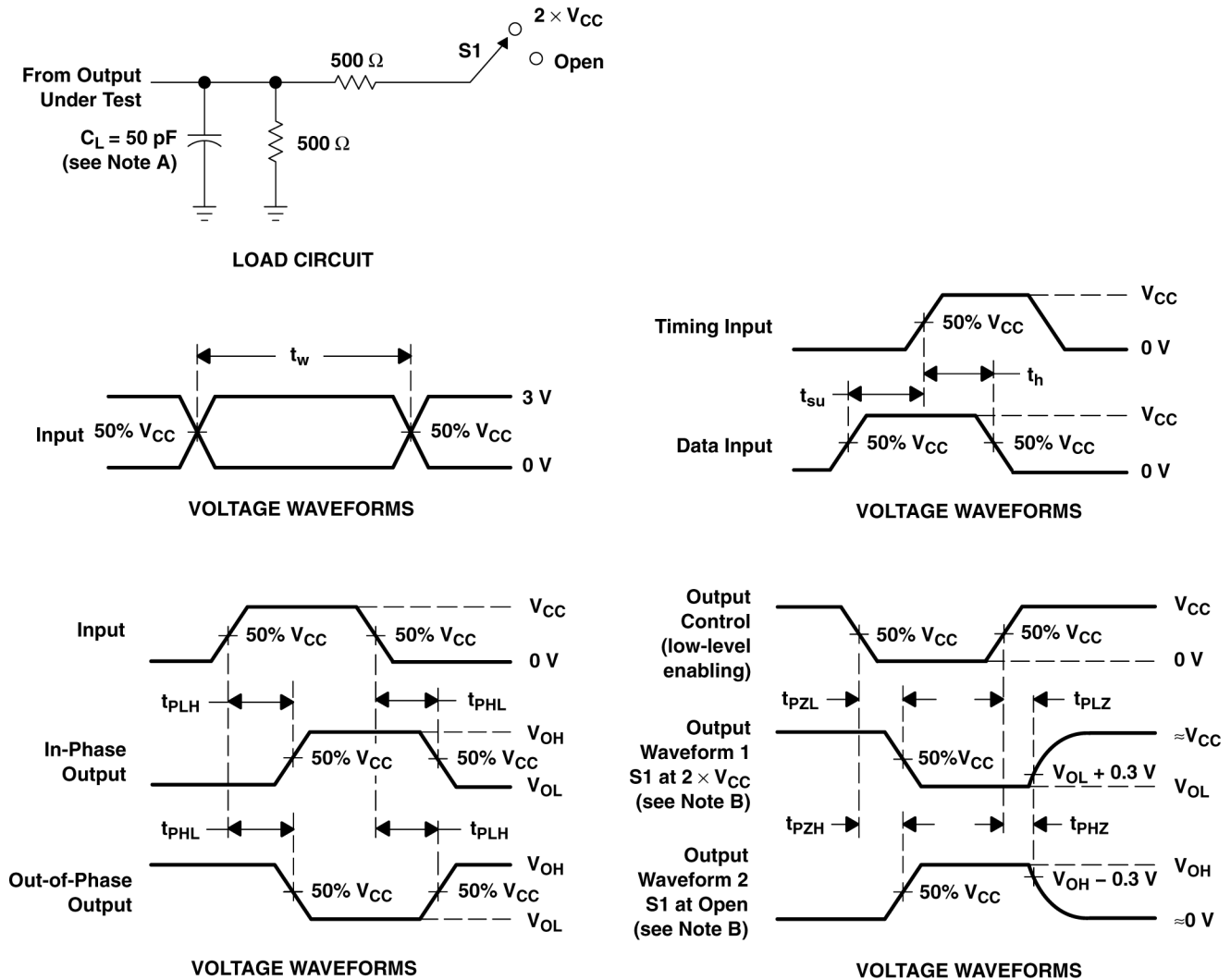
PARAMETER	TO (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN54AC574		SN74AC574		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			95	153		85		85	MHz	
$t_{\text{PLH}}$	CLK	Q	2	6	9.5	1.5	11.5	2	11	ns
$t_{\text{PHL}}$			2	5.5	8.5	1.5	10.5	2	9.5	
$t_{\text{PZH}}$	$\overline{\text{OE}}$	Q	2	5	8.5	1.5	9.5	2	9	ns
$t_{\text{PZL}}$			2	5	8	1.5	9.5	1.5	9	
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	Q	2	6	9.5	1.5	11.5	1.5	10.5	ns
$t_{\text{PLZ}}$			1	4.5	7.5	1.5	9	1	8.5	

#### 4.9 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{\text{pd}}$	Power dissipation capacitance $C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	40	pF

## 5 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 5-1. Load Circuit and Voltage Waveforms

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	Open

## 6 Detailed Description

### 6.1 Overview

The eight flip-flops of the 'AC574 devices are D-type edge-triggered flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines in a bus-organized system without need for interface or pullup components.

$\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

For the specified high-impedance state during power up or power down,  $\overline{OE}$  must be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 6.2 Functional Block Diagram

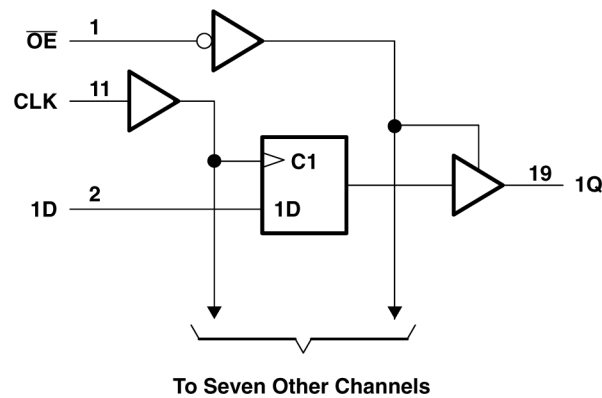


Figure 6-1. Logic Diagram (Positive Logic)

### 6.3 Device Functional Modes

Table 6-1. Function Table (Each Flip-flop)

INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
L	↑	H	H
L	↑	L	L
L	H or L	X	$Q_0$
H	X	X	Z



## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the Recommended Operating Conditions table.

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1  $\mu\text{F}$  capacitor is recommended. If there are multiple  $V_{CC}$  terminals then 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1  $\mu\text{F}$  and 1.0  $\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

### 7.2 Layout

#### 7.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [layout example](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

##### 7.2.1.1 Layout Example

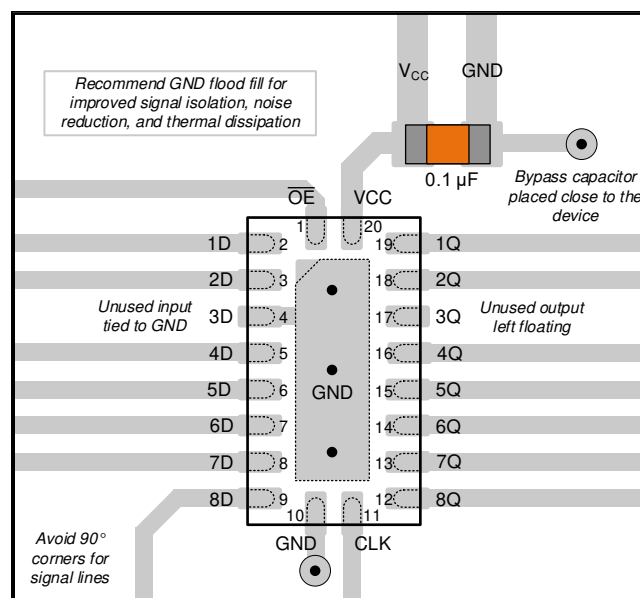


Figure 7-1. Layout example for the SNx4AC574

## 8 Device and Documentation Support

### 8.1 Documentation Support (Analog)

#### 8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and Cpd Calculation application report](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application report](#)

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision F (August 2023) to Revision G (March 2024)</b>	<b>Page</b>
• Updated RθJA values: DW = 58 to 101.2, PW = 83 to 126.2, all values in °C/W .....	5
• Added <i>Application and Implementation</i> section.....	9

<b>Changes from Revision E (October 2003) to Revision F ( August 2023)</b>	<b>Page</b>
• Added <i>Device Information</i> table, <i>Pin Functions</i> table, <i>Thermal Information</i> table, <i>Device Functional Modes, Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9677301Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9677301Q2A SNJ54AC 574FK	<a href="#">Samples</a>
5962-9677301QRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9677301QR A SNJ54AC574J	<a href="#">Samples</a>
5962-9677301QSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9677301QS A SNJ54AC574W	<a href="#">Samples</a>
SN74AC574DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC574	<a href="#">Samples</a>
SN74AC574DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC574	<a href="#">Samples</a>
SN74AC574N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AC574N	<a href="#">Samples</a>
SN74AC574PW	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85	AC574	
SN74AC574PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC574	<a href="#">Samples</a>
SN74AC574PWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC574	<a href="#">Samples</a>
SNJ54AC574FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9677301Q2A SNJ54AC 574FK	<a href="#">Samples</a>
SNJ54AC574J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9677301QR A SNJ54AC574J	<a href="#">Samples</a>
SNJ54AC574W	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9677301QS A SNJ54AC574W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54AC574, SN74AC574 :**

● Catalog : [SN74AC574](#)

● Military : [SN54AC574](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC574DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AC574DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74AC574DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AC574PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AC574PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC574DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74AC574DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AC574DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AC574PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AC574PWR	TSSOP	PW	20	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9677301Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9677301QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74AC574N	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AC574FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AC574W	W	CFP	20	25	506.98	26.16	6220	NA

# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019



# EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

PW0020A



# PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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