

SN54ALS580B, SN74ALS580B, SN74AS580 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SDAS277 – JANUARY 1995

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Inverting-Logic Outputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), Standard Plastic (N) and Ceramic (J) 300-mil DIPs, and Ceramic Flat (W) Packages

description

These octal D-type transparent latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

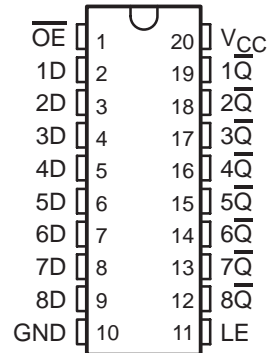
While the latch-enable (LE) input is high, outputs (\overline{Q}) respond to the data (D) inputs. When LE is low, the outputs are latched to retain the data that was set up.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

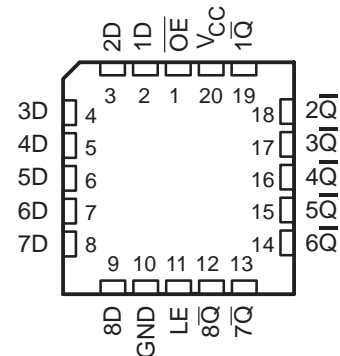
\overline{OE} does not affect internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS580B is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS580B and SN74AS580 are characterized for operation from 0°C to 70°C .

SN54ALS580B . . . J OR W PACKAGE
SN74ALS580B, SN74AS580 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS580B . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each latch)

INPUTS			OUTPUT \overline{Q}
\overline{OE}	LE	D	
L	H	H	L
L	H	L	H
L	L	X	\overline{Q}_0
H	X	X	Z

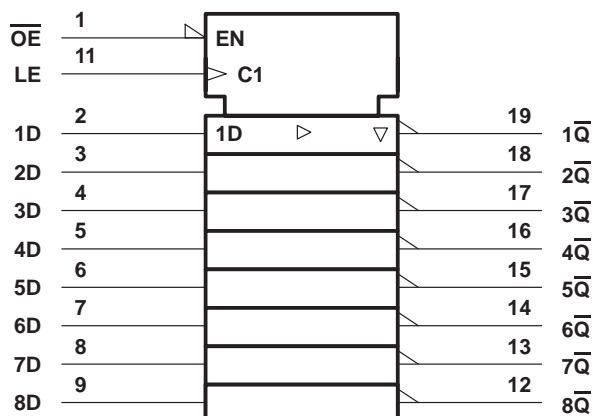
SN54ALS580B, SN74ALS580B, SN74AS580

OCTAL D-TYPE TRANSPARENT LATCHES

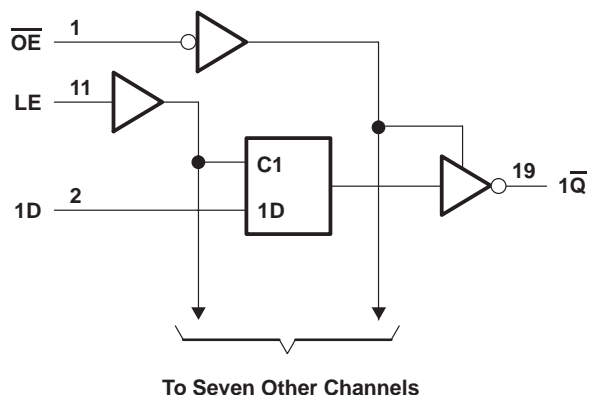
WITH 3-STATE OUTPUTS

SDAS277 – JANUARY 1995

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A : SN54ALS580B	–55°C to 125°C
SN74ALS580B	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS580B			SN74ALS580B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			–1			–2.6	mA
I_{OL}	Low-level output current			12			24	mA
t_w	Pulse duration, LE high	15			15			ns
t_{su}	Setup time, data before LE↓	20			10			ns
t_h	Hold time, data after LE↓	12			10			ns
T_A	Operating free-air temperature	–55		125	0		70	°C



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

SN54ALS580B, SN74ALS580B, SN74AS580

OCTAL D-TYPE TRANSPARENT LATCHES

WITH 3-STATE OUTPUTS

SDAS277 – JANUARY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS580B		SN74ALS580B		UNIT
			MIN	TYP†	MAX	MIN	
V _{IK}	V _{CC} = 4.5 V, I _I = −18 mA		−1.2		−1.2		V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = −0.4 mA		V _{CC} − 2		V _{CC} − 2		V
	V _{CC} = 4.5 V	I _{OH} = −1 mA	2.4	3.3			
		I _{OH} = −2.6 mA			2.4	3.2	
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 12 mA	0.25 0.4		0.25 0.4		V
		I _{OL} = 24 mA			0.35 0.5		
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V	20		20		μA	
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V	−20		−20		μA	
I _I	V _{CC} = 5.5 V, V _I = 7 V	0.1		0.1		mA	
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V	20		20		μA	
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V	−0.13		−0.1		mA	
I _O ‡	V _{CC} = 5.5 V, V _O = 2.25 V	−20	−112	−30	−112	mA	
I _{CC}	V _{CC} = 5.5 V	Outputs high	10	17	10	17	mA
		Outputs low	16	26	16	26	
		Outputs disabled	17	29	17	29	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX§				UNIT
			SN54ALS580B		SN74ALS580B		
			MIN	MAX	MIN	MAX	
t _{PLH}	D	Q1	3	26	3	18	ns
t _{PHL}			3	15	3	14	
t _{PLH}	LE	Q1	8	29	6	22	ns
t _{PHL}			4	22	6	21	
t _{PZH}	OE	Q1	4	25	3	18	ns
t _{PZL}			4	21	4	18	
t _{PHZ}	OE	Q1	2	12	1	10	ns
t _{PLZ}			3	22	1	15	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54ALS580B, SN74ALS580B, SN74AS580

OCTAL D-TYPE TRANSPARENT LATCHES

WITH 3-STATE OUTPUTS

SDAS277 – JANUARY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A : SN74AS580	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN74AS580			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–15	mA
I_{OL}	Low-level output current			48	mA
t_w^*	Pulse duration, LE high	2			ns
t_{su}^*	Setup time, data before LE↓	2			ns
t_h^*	Hold time, data after LE↓	3			ns
T_A	Operating free-air temperature	0		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN74AS580			UNIT
		MIN	TYP [‡]	MAX	
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2	V
V_{OH}	$V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -2$ mA	$V_{CC} - 2$			V
	$V_{CC} = 4.5$ V, $I_{OH} = -15$ mA	2.4	3.3		
V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 48$ mA		0.33	0.5	V
I_{OZH}	$V_{CC} = 5.5$ V, $V_O = 2.7$ V			50	μA
I_{OZL}	$V_{CC} = 5.5$ V, $V_O = 0.4$ V			–50	μA
I_I	$V_{CC} = 5.5$ V, $V_I = 7$ V			0.1	mA
I_{IH}	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20	μA
I_{IL}	$V_{CC} = 5.5$ V, $V_I = 0.4$ V			–0.5	mA
I_{O}^{\S}	$V_{CC} = 5.5$ V, $V_O = 2.25$ V	–30		–112	mA
I_{CC}	$V_{CC} = 5.5$ V	Outputs high		62	mA
		Outputs low		65	
		Outputs disabled		71	

[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

^{\S} The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .



SN54ALS580B, SN74ALS580B, SN74AS580 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SDAS277 – JANUARY 1995

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX†		UNIT
			SN74AS580		
			MIN	MAX	
t _{PLH}	D	\overline{Q}	3	7.5	ns
t _{PHL}			3	7	
t _{PLH}	LE	\overline{Q}	5	9	ns
t _{PHL}			4	8	
t _{PZH}	\overline{OE}	\overline{Q}	2	6.5	ns
t _{PZL}			4	9.5	
t _{PHZ}	\overline{OE}	\overline{Q}	2	6.5	ns
t _{PLZ}			2	7	

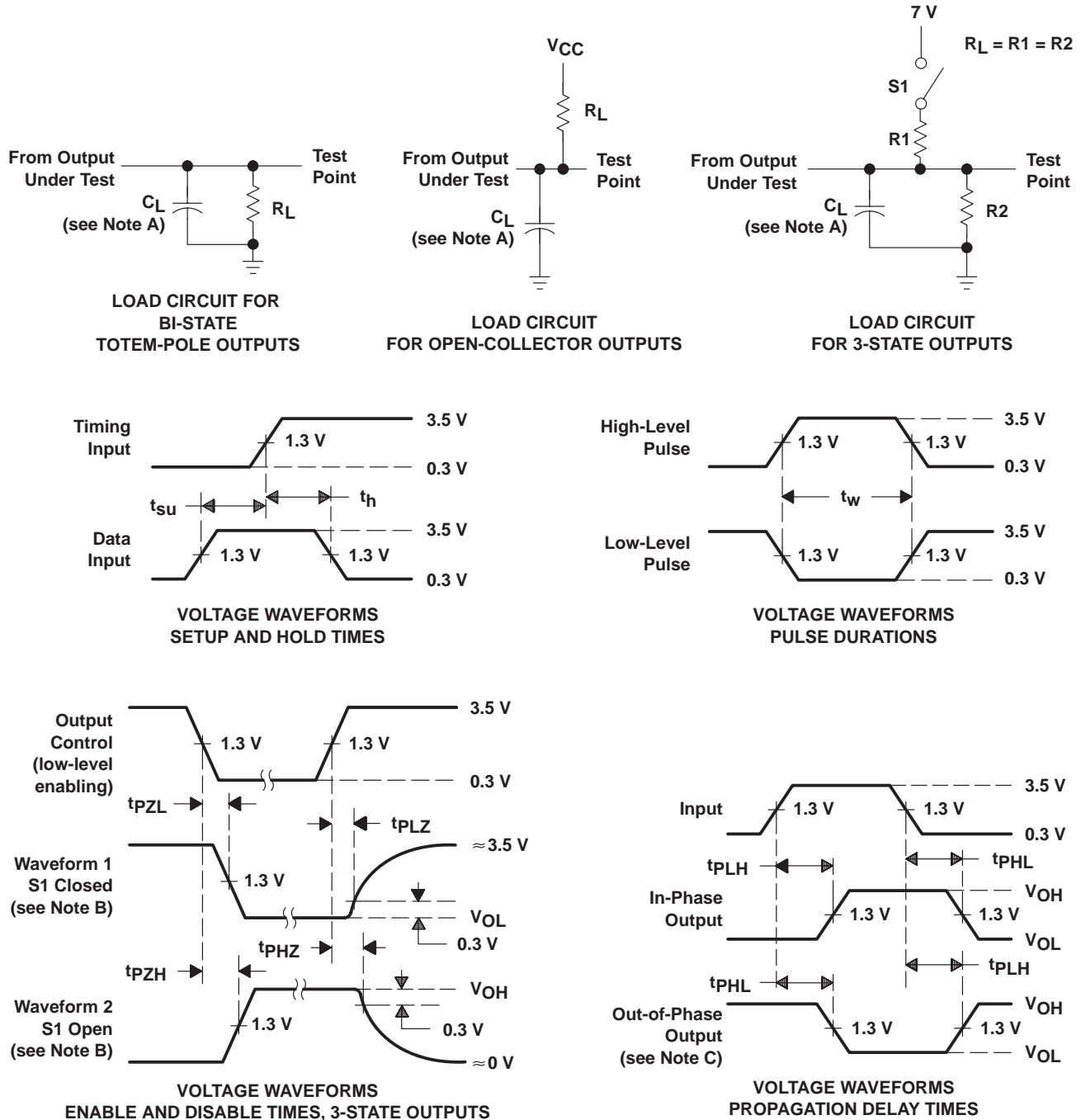
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54ALS580B, SN74ALS580B, SN74AS580 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SDAS277 – JANUARY 1995

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
84012022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84012022A SNJ54ALS 580BFBK	Samples
8401202RA	ACTIVE	CDIP	J	20	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	8401202RA SNJ54ALS580BJ	Samples
8401202SA	ACTIVE	CFP	W	20	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	8401202SA SNJ54ALS580BW	Samples
SN54ALS580BJ	ACTIVE	CDIP	J	20	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	SN54ALS580BJ	Samples
SN74ALS580BN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS580BN	Samples
SNJ54ALS580BFBK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84012022A SNJ54ALS 580BFBK	Samples
SNJ54ALS580BJ	ACTIVE	CDIP	J	20	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	8401202RA SNJ54ALS580BJ	Samples
SNJ54ALS580BW	ACTIVE	CFP	W	20	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	8401202SA SNJ54ALS580BW	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ALS580B, SN74ALS580B :

● Catalog: [SN74ALS580B](#)

● Military: [SN54ALS580B](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated