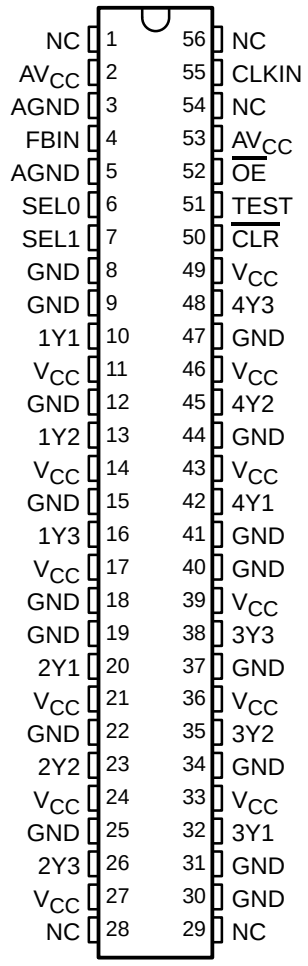
- **Low Output Skew for Clock-Distribution and Clock-Generation Applications**
- **Operates at 3.3-V V_{CC}**
- **Distributes One Clock Input to 12 Outputs**
- **Two Select Inputs Configure Up to Nine Outputs to Operate at One-Half or Double the Input Frequency**
- **No External RC Network Required**
- **External Feedback Pin (FBIN) Is Used to Synchronize the Outputs to the Clock Input**
- **Application for Synchronous DRAM, High-Speed Microprocessor**
- **TTL-Compatible Inputs and Outputs**
- **Outputs Drive Parallel 50-Ω Terminated Transmission Lines**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **Packaged in 56-Pin Ceramic Flat Package**

WD PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN54CDC586 is a high-performance, low-skew, low-jitter clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the clock output signals to the clock input (CLKIN) signal. It is specifically designed for use with popular microprocessors operating at speeds from 50 MHz to 100 MHz, or down to 25 MHz on outputs configured as half-frequency outputs. The SN54CDC586 operates at 3.3-V V_{CC} and is designed to drive a properly terminated 50-Ω transmission line.

The feedback input (FBIN) is used to synchronize the output clocks in frequency and phase to CLKIN. One of the 12 output clocks must be fed back to FBIN for the PLL to maintain synchronization between the CLKIN input and the outputs. The output used as the feedback pin is synchronized to the same frequency as the CLKIN input.

The Y outputs can be configured to switch in phase and at the same frequency as CLKIN. Select inputs (SEL1, SEL0) configure up to nine Y outputs, in banks of three, to operate at one-half or double the CLKIN frequency, depending on which pin is fed back to FBIN (see Tables 1 and 2). All output-signal duty cycles are adjusted to 50%, independent of the duty cycle at CLKIN.

description (continued)

Output-enable ($\overline{OE}$) is provided for output control. When $\overline{OE}$ is high, the outputs are in the high-impedance state. When $\overline{OE}$ is low, the outputs are active. $\overline{CLR}$ is negative-edge triggered and can be used to reset the outputs operating at half frequency. TEST is used for factory testing of the device and can be used to bypass the PLL. TEST should be strapped to GND for normal operation.

Unlike many products containing PLLs, the SN54CDC586 does not require external RC networks. The loop filter for the PLL is included on chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the SN54CDC586 requires stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLKIN, as well as following any changes to the PLL reference or feedback signals. Such changes occur upon change of the select inputs, enabling of the PLL via TEST, and upon enable of all outputs via $\overline{OE}$.

The SN54CDC586 is characterized for operation over the full military temperature range of –55°C to 125°C.

detailed description of output configurations

The voltage-controlled oscillator (VCO) used in the SN54CDC586 PLL has a frequency range of 100 MHz to 200 MHz, twice the operating frequency range of the SN54CDC586 outputs. The output of the VCO is divided by two and by four to provide reference frequencies with a 50% duty cycle of one-half and one-fourth the VCO frequency. SEL0 and SEL1 select which of the two signals are buffered to each bank of device outputs.

One device output must be externally wired to FBIN to complete the PLL. The VCO operates such that the frequency and phase of this output match that of CLKIN. In the case in which a VCO/2 output is wired to FBIN, the VCO must operate at twice the CLKIN frequency, resulting in device outputs that operate at either the same or one-half the CLKIN frequency. If a VCO/4 output is wired to FBIN, the device outputs operate at twice or the same frequency as the CLKIN frequency.

output configuration A

Output configuration A is valid when any output configured as a 1× frequency output in Table 1 is fed back to FBIN. The input frequency range for CLKIN is 50 MHz to 100 MHz when using output configuration A. Outputs configured as 1/2× outputs operate at one-half the CLKIN frequency, while outputs configured as 1× outputs operate at the same frequency as CLKIN.

Table 1. Output Configuration A

INPUTS		OUTPUTS	
SEL1	SEL0	1/2× FREQUENCY	1× FREQUENCY
L	L	None	All
L	H	1Yn	2Yn, 3Yn, 4Yn
H	L	1Yn, 2Yn	3Yn, 4Yn
H	H	1Yn, 2Yn, 3Yn	4Yn

NOTE: n = 1, 2, 3

output configuration B

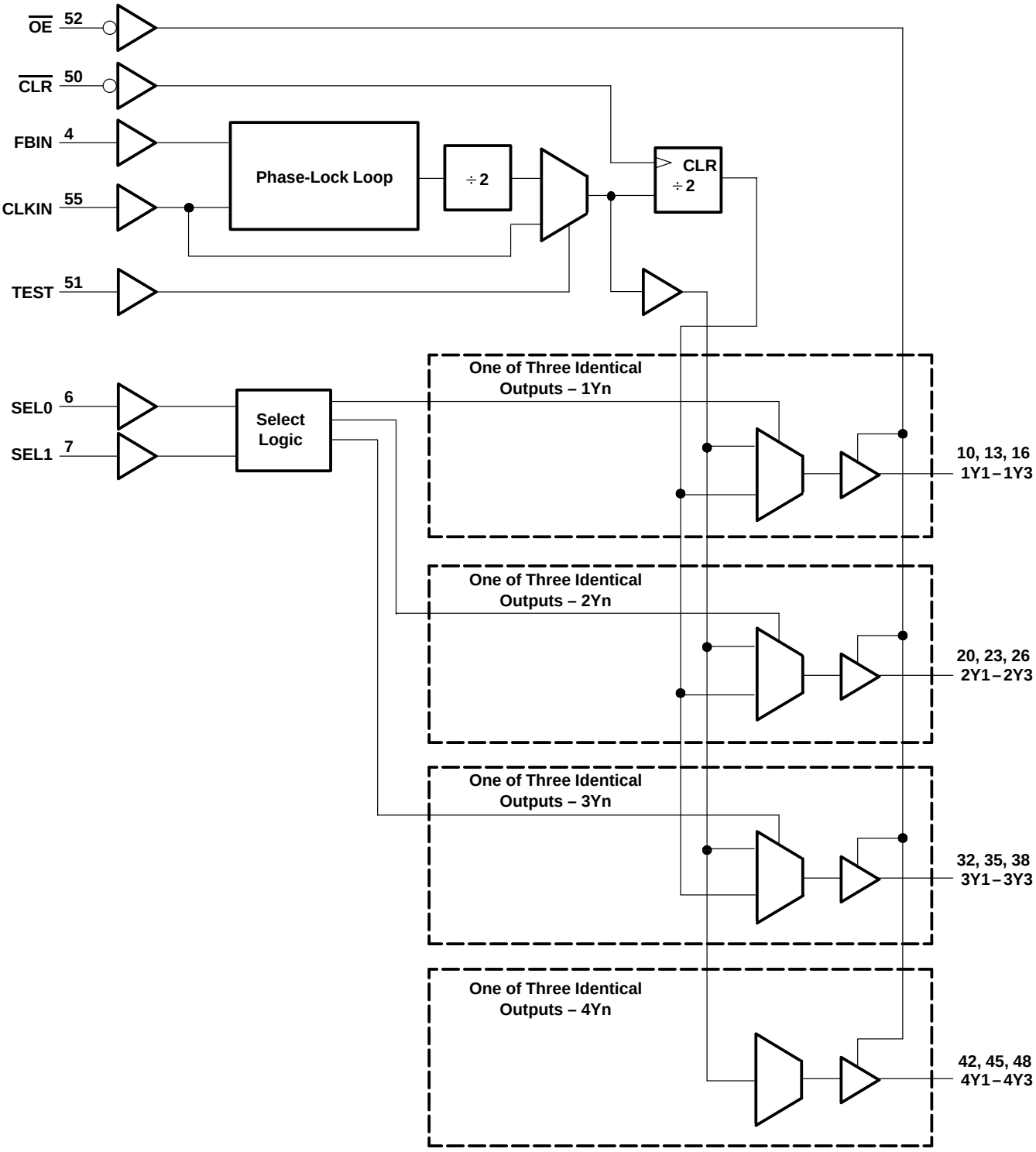
Output configuration B is valid when any output configured as a 1× frequency output in Table 2 is fed back to FBIN. The input frequency range for CLKIN is 25 MHz to 50 MHz when using output configuration B. Outputs configured as 1× outputs operate at the CLKIN frequency, while outputs configured as 2× outputs operate at double the frequency of CLKIN.

Table 2. Output Configuration B

INPUTS		OUTPUTS	
SEL1	SEL0	1× FREQUENCY	2× FREQUENCY
L	L	All	None
L	H	1Yn	2Yn, 3Yn, 4Yn
H	L	1Yn, 2Yn	3Yn, 4Yn
H	H	1Yn, 2Yn, 3Yn	4Yn

NOTE: n = 1, 2, 3

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLKIN	55	I	Clock input. CLKIN is the clock signal distributed by the SN54CDC586 clock-driver circuit. CLKIN provides the reference signal to the integrated PLL that generates the clock output signals. CLKIN must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLKIN signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
$\overline{CLR}$	50	I	Clear. $\overline{CLR}$ resets the VCO/4 reference frequency. $\overline{CLR}$ is negative-edge triggered and should be strapped to GND or V_{CC} for normal operation.
FBIN	4	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hardwired to one of the 12 clock outputs to provide frequency and phase lock. The internal PLL adjusts the output clocks to obtain zero phase delay between FBIN and CLKIN.
$\overline{OE}$	52	I	Output enable. $\overline{OE}$ is the output enable for all outputs. When $\overline{OE}$ is low, all outputs are enabled. When $\overline{OE}$ is high, all outputs are in the high-impedance state. Since the feedback signal for the PLL is taken directly from an output terminal, placing the outputs in the high-impedance state interrupts the feedback loop; therefore, when a high-to-low transition occurs at $\overline{OE}$, enabling the output buffers, a stabilization time is required before the PLL obtains phase lock.
SEL1, SEL0	7, 6	I	Output configuration select. SEL0 and SEL1 select the output configuration for each output bank (e.g., 1×, 1/2×, or 2×). (see Tables 1 and 2).
TEST	51	I	TEST is used to bypass the PLL circuitry for factory testing of the device. When TEST is low, all outputs operate using the PLL circuitry. When TEST is high, the outputs are placed in a test mode that bypasses the PLL circuitry. TEST should be strapped to GND for normal operation.
1Y1–1Y3 2Y1–2Y3 3Y1–3Y3	10, 13, 16 20, 23, 26 32, 35, 38	O	Output ports. These outputs are configured by SEL1 and SEL0 to transmit one-half or one-fourth the frequency of the VCO. The relationship between the CLKIN frequency and the output frequency is dependent on SEL1 and SEL0 and the frequency of the output being fed back to FBIN. The duty cycle of the Y-output signals is nominally 50%, independent of the duty cycle of CLKIN.
4Y1–4Y3	42, 45, 48	O	Output ports. 4Y1–4Y3 transmit one-half the frequency of the VCO, regardless of the state of SEL1 and SEL0. The relationship between the CLKIN frequency and the output frequency is dependent on the frequency of the output being fed back to FBIN. The duty cycle of the Y-output signals nominally is 50%, independent of the duty cycle of CLKIN.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state,
V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O . . . . . 64 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –20 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
T_A	Operating free-air temperature	–55	125	°C

NOTE 2: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C		UNIT
				MIN	MAX	
V_{IK}	V_{CC} = 3 V,	I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = MIN to MAX†,	I_{OH} = –100 µA		V_{CC}–0.2		V
	V_{CC} = 3 V,	I_{OH} = – 32 mA		2		
V_{OL}	V_{CC} = 3 V	I_{OL} = 100 µA			0.2	V
		I_{OL} = 32 mA			0.5	
I_I	V_{CC} = 0 or MAX†,	V_I = 3.6 V			±10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1	
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			10	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0			–10	µA
I_{CC}	V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND		Outputs high		1	mA
			Outputs low		1	
			Outputs disabled		1	
C_i	V_I = V_{CC} or GND				4	pF
C_o	V_O = V_{CC} or GND				8	pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency	VCO is operating at four times the CLKIN frequency	25	50	MHz
		VCO is operating at double the CLKIN frequency	50	100	
	Input clock duty cycle		40%	60%	
	Stabilization time†	After SEL1, SEL0		50	µs
		After $\overline{OE}\downarrow$		50	
		After power up		50	
		After CLKIN		50	

† Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF, unless otherwise noted (see Note 3 and Figures 1 through 3)

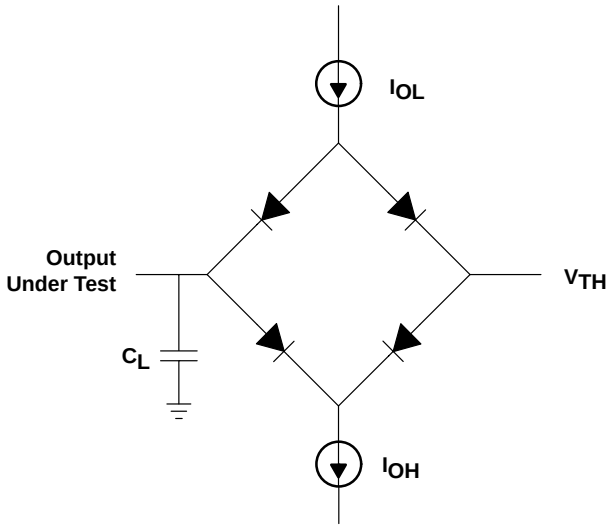
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}			100		MHz
Duty cycle		Y	42%	58%	
$t_{phase\ error}$‡	CLKIN↑	Y	–500	500	ps
$Jitter_{(pk\text{-}pk)}$*	CLKIN↑	Y		200	ps
$t_{sk(o)}$‡				0.75	ns
$t_{sk(pr)}$‡*				1.1	ns
t_r				1.4	ns
t_f				1.4	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

‡ The propagation delay, $t_{phase\ error}$, is dependent on the feedback path from any output to FBIN. The $t_{phase\ error}$, $t_{sk(o)}$, and $t_{sk(pr)}$ specifications are valid only for equal loading of all outputs.

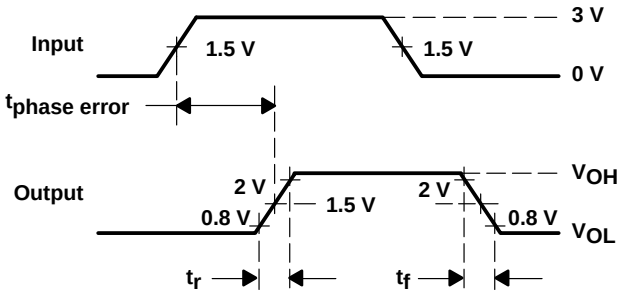
NOTE 3: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

PARAMETER MEASUREMENT INFORMATION



PARAMETER	I_{OL}	I_{OH}	V_{TH}	C_L (typical)
$t_{phase\ error}$	32 mA	32 mA	1.5 V	20 pF
t_r, t_f	16 mA	16 mA	1.5 V	20 pF

LOAD CIRCUIT

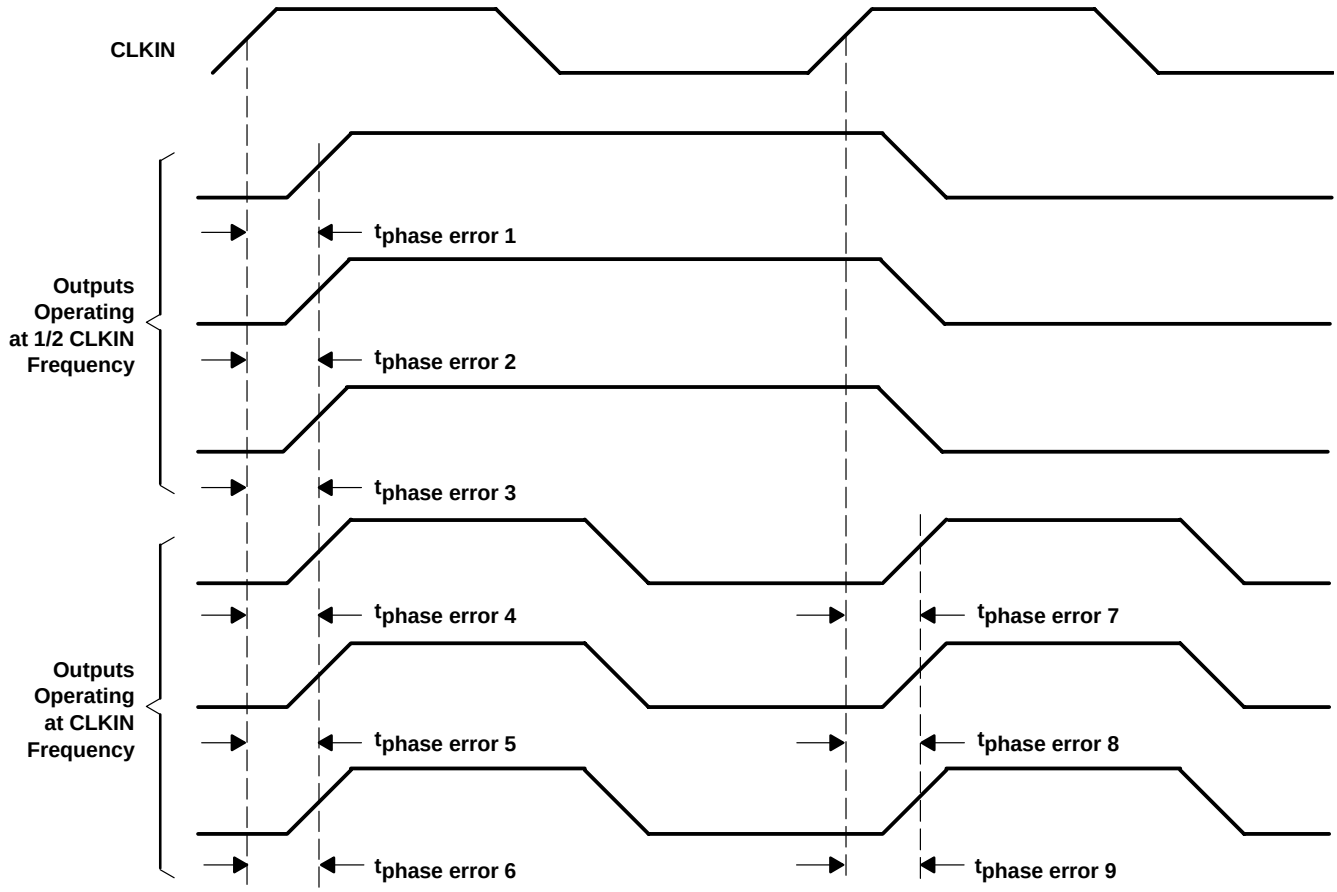


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The outputs are measured one at a time with one transition per measurement.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 100 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

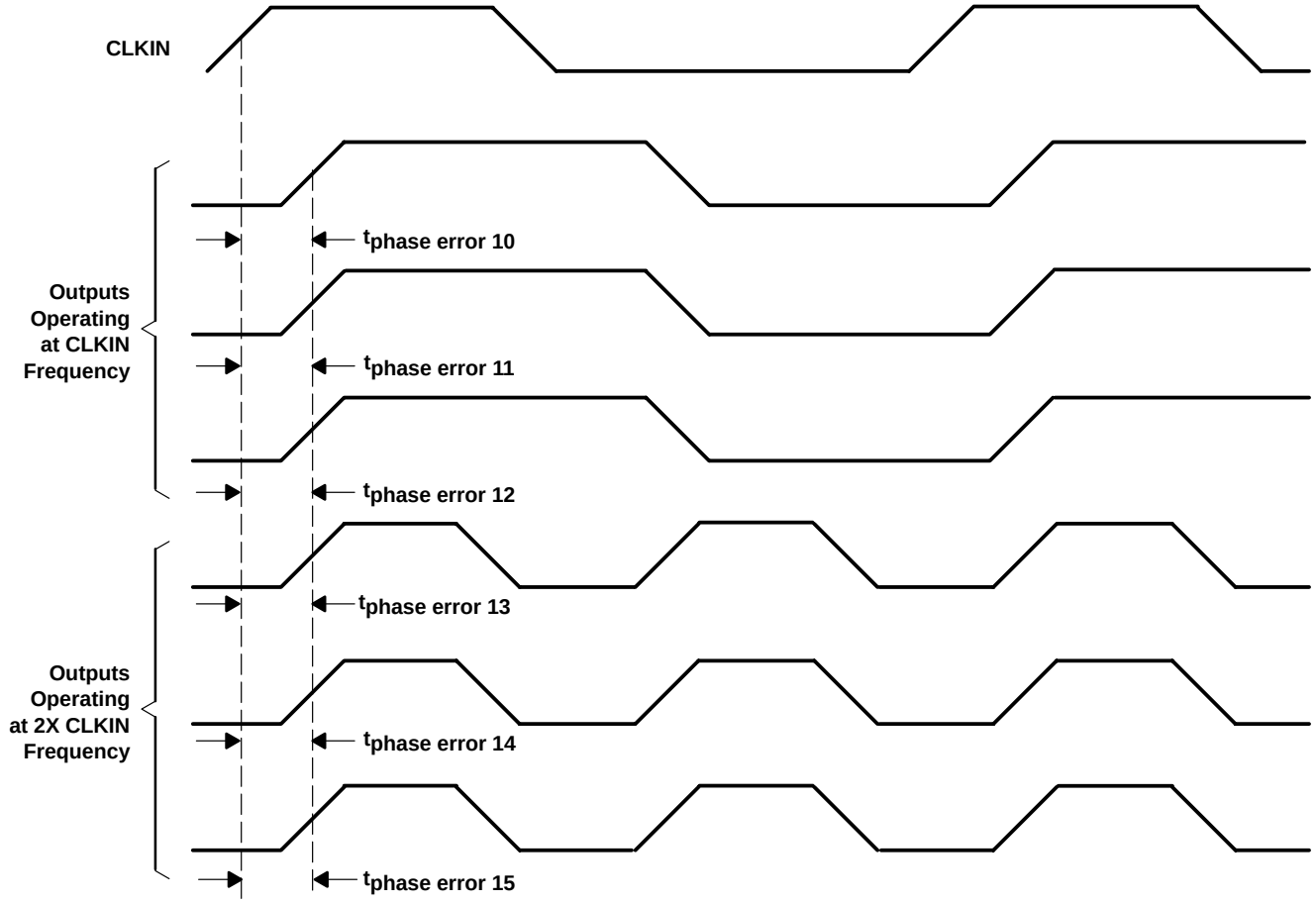


NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 1, 2, . . . 6)
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 7, 8, 9)

B. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
- The difference between the maximum and minimum $t_{phase\ error\ n}$ (n = 1, 2, . . . 6) across multiple devices under identical operating conditions.
- The difference between the maximum and minimum $t_{phase\ error\ n}$ (n = 7, 8, 9) across multiple devices under identical operating conditions.

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
– The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 10, 11, . . . 15)
B. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
– The difference between the maximum and minimum $t_{phase\ error\ n}$ (n = 10, 11, . . . 15) across multiple devices under identical operating conditions.

Figure 3. Waveforms for Calculation of $t_{sk(o)}$ and $t_{sk(pr)}$

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Post Office Box 655303 Dallas, Texas 75265