SNx4HCT125 Quadruple Bus Buffer Gates With 3-State Outputs

1 Features

- Operating voltage range of 4.5 V to 5.5 V
- High-current can drive up to 15 LSTTL loads
- Low power consumption, 80-µA max I_{CC}
- Typical t_{pd} = 12 ns
- ±6-mA output drive at 5 V
- Low input current of 1 µA max
- Inputs are TTL-voltage compatible
- High-current 3-state outputs drive bus lines or buffer memory address registers

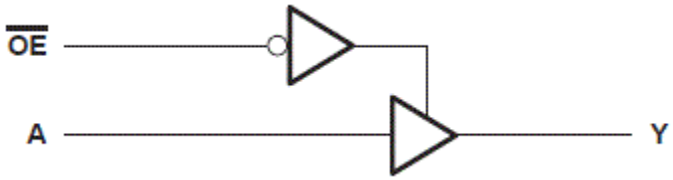
2 Description

The SNx4HCT125 contains four independent buffers with TTL-compatible inputs and 3-state outputs. Each gate performs the Boolean function Y = A in positive logic.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
SN74HCT125D	SOIC (14)	8.65 mm × 3.90 mm
SN74HCT125N	PDIP (14)	19.31 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram

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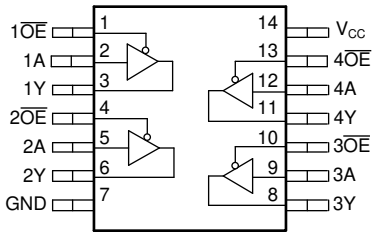
3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

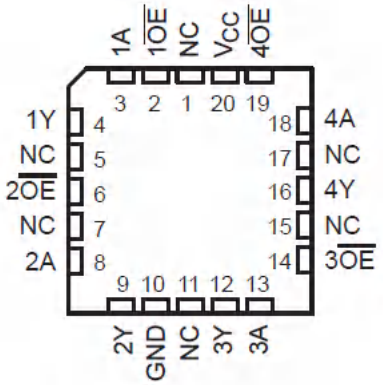
Changes from Revision F (February 2022) to Revision G (October 2022)	Page
• Increased RθJA for packages: D (86 to 138.7); N (80 to 75.3)	4

Changes from Revision E (August 2003) to Revision F (February 2022)	Page
• Updated the numbering, formatting, tables, figures, and cross-references throughout the doucment to reflect modern data sheet standards	1

4 Pin Configuration and Functions



D, N, J or W Package
14-Pin SOIC or PDIP
Top View



FK Package
20-Pin LCCC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
I_{IK}	Input clamp current(2)	(V_I < 0 or V_I > V_{CC})		±20	mA
I_{OK}	Output clamp current(2)	(V_O < 0 or V_O > V_{CC})		±20	mA
I_O	Continuous output current	(V_O = 0 to V_{CC})		±35	mA
V_{CC} or GND	Continuous current through			±70	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions(1)

			SN54HCT125(2)			SN74HCT125			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V			0.8			0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition rise/fall time				500			500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report Implications of Slow or Floating SMOS Inputs, literature number SCBA004.
(2) SN54HCT125 is in product preview.

5.3 Thermal Information

THERMAL METRIC		D (SOIC) 14 PINS	N (PDIP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	138.7	75.3	°C/W
$R_{\theta JC}$	Junction-to-case (top) thermal resistance	93.8	68.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.7	55.1	°C/W
ψ_{JT}	Junction-to-top characterization paramete	49.1	41.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	94.3	54.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS[1]	V_{CC} (V)	T_A = 25°C			SN54HCT125[3]		SN74HCT125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = –20 µA	4.5	4.4	4.499		4.4		4.4		V
		I_{OH} = –6 mA		3.98	4.3		3.7		3.84		
V_{OL}	Low-level output voltage	I_{OL} = 20 µA	5.5		0.001	0.1		0.1		0.1	V
		I_{OL} = 6 mA			0.17	0.26		0.4		0.33	
I_I	Input hold current	V_I = V_{CC} or 0	5.5		±0.1	±100		±1000		±1000	nA
I_{OZ}	Off-state output current	V_o = V_{CC} or 0	5.5		±0.01	±0.5		±10		±5	µA
I_{CC}	Supply current	V_I = V_{CC} or 0. I_O = 0	5.5			8		160		80	µA
ΔI_{CC} [2]	Supply-current change	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}	5.5		1.4	2.4		3		2.9	mA
C_i	Input capacitance		4.5 to 5.5		3	10		10[4]		10	pF

(1) V_I = V_{IH} or V_{IL}, unless otherwise noted.
(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.
(3) SN54HCT125 is in product preview.
(4) On products compliant to MIL-PRF-38535, this parameter is not production tested.

5.5 Switching Characteristics

C_L = 50 pF. See Figure 6

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC} (V)	T_A = 25°C			SN54HCT125 [1]		SN74HCT125		
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	Y	4.5		11	20		39		25	ns
				5.5		10	18		35		22	
t_{en}	Enable time	$\overline{OE}$	Y	4.5		18	28		42		35	ns
				5.5		15	25		38		31	
t_{dis}	Diable time	$\overline{OE}$	Y	4.5		15	26		39		33	ns
				5.5		13	23		35		30	
t_t	Transition time		Any	4.5		8	15		22		19	ns
				5.5		7	14		21		17	

(1) SN54HCT125 is in product preview.

5.5 Switching Characteristics

C_L = 150 pF. See Figure 6

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC} (V)	T_A = 25°C			SN54HCT125 [1]		SN74HCT125		
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	Y	4.5		19	36		58		46	ns
				5.5		16	32		48		42	
t_{en}	Enable time	$\overline{OE}$	Y	4.5		25	40		60		50	ns
				5.5		21	35		53		43	
t_t	Transition time		Any	4.5		17	42		63		53	ns
				5.5		14	38		57		48	

(1) SN54HCT125 is in product preview.

5.6 Operating Characteristics

T_A = 25°C

		Test Conditions	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	35	pF

6 Parameter Measurement Information

t_{pd} is the maximum between t_{PLH} and t_{PHL}

t_t is the maximum between t_{TLH} and t_{THL}

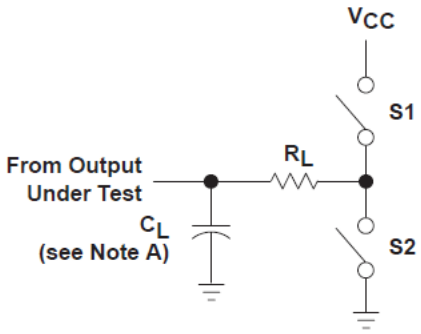


Figure 6-1. Load Circuit

PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open

Figure 6-2.

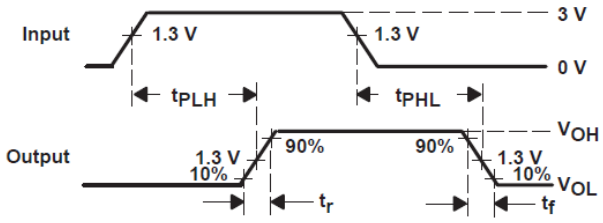


Figure 6-3. Voltage Waveforms Propagation Delay Times

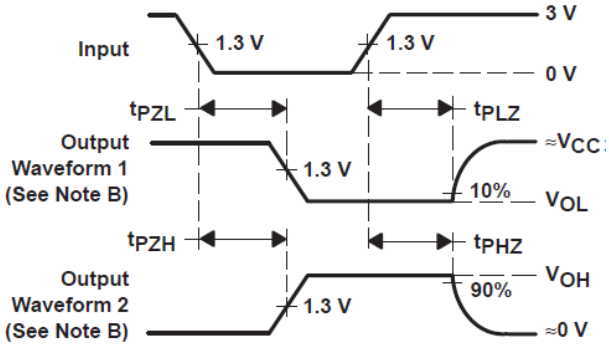


Figure 6-4. Voltage Waveforms Enable and Disable Times For 3-state Outputs

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when diabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when diabled by the output control.

C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following charactersitics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.

D. The outputs are measured one at a time with one input transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

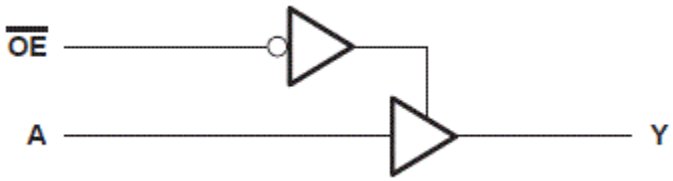
7 Detailed Description

7.1 Overview

These bus buffer gates feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram



7.3 Device Functional Modes

Table 7-1. Function Table (each gate)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCT125DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HCT125	Samples
SN74HCT125DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT125	Samples
SN74HCT125N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT125N	Samples
SN74HCT125NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT125N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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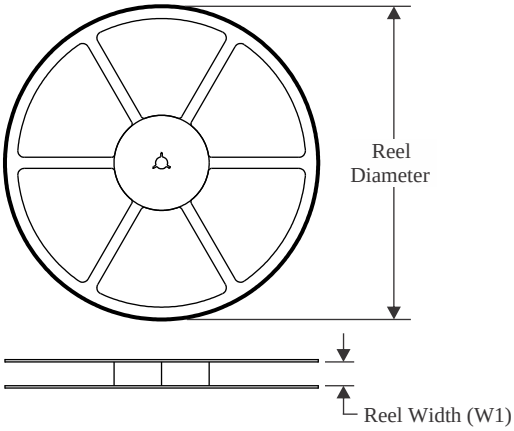
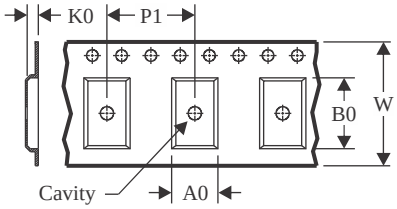
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

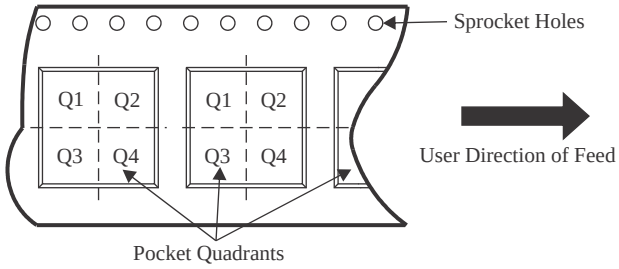


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

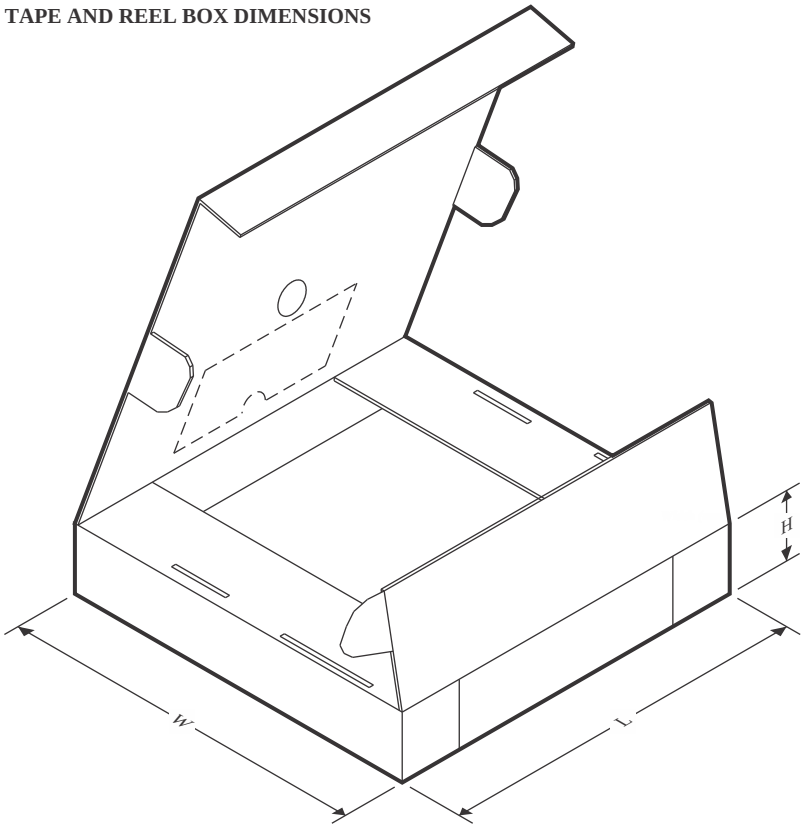
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT125DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCT125DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCT125DR	SOIC	D	14	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1

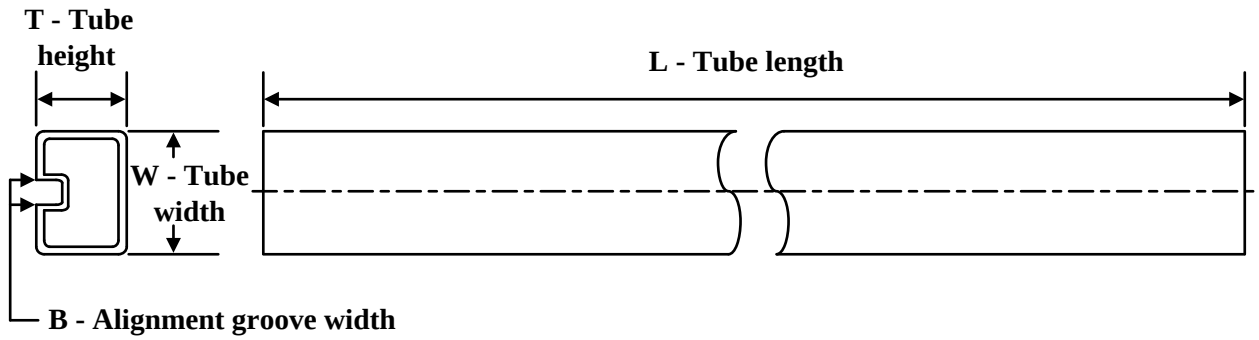
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT125DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74HCT125DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74HCT125DR	SOIC	D	14	2500	366.0	364.0	50.0

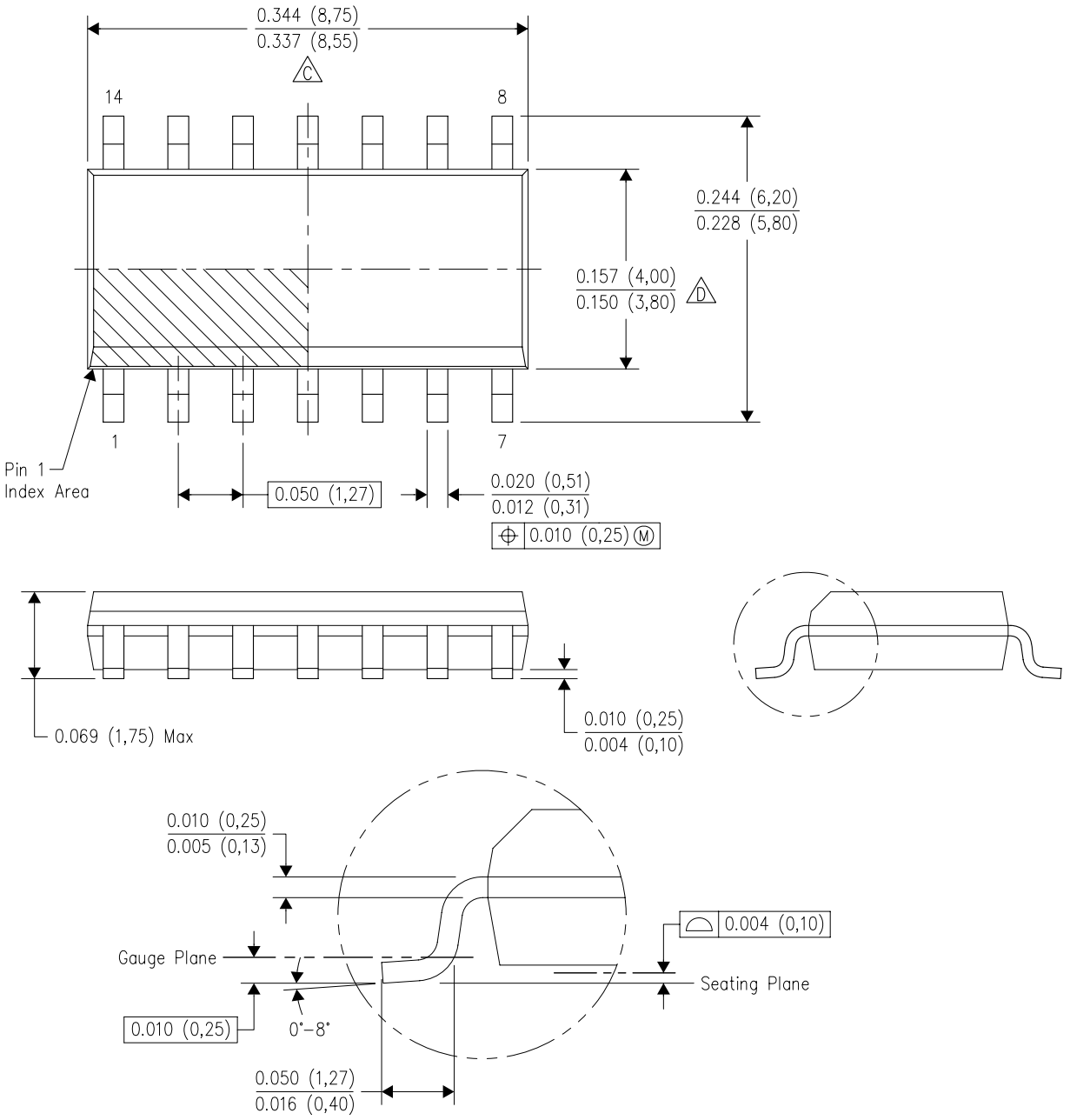
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74HCT125N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT125N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT125NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT125NE4	N	PDIP	14	25	506	13.97	11230	4.32

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



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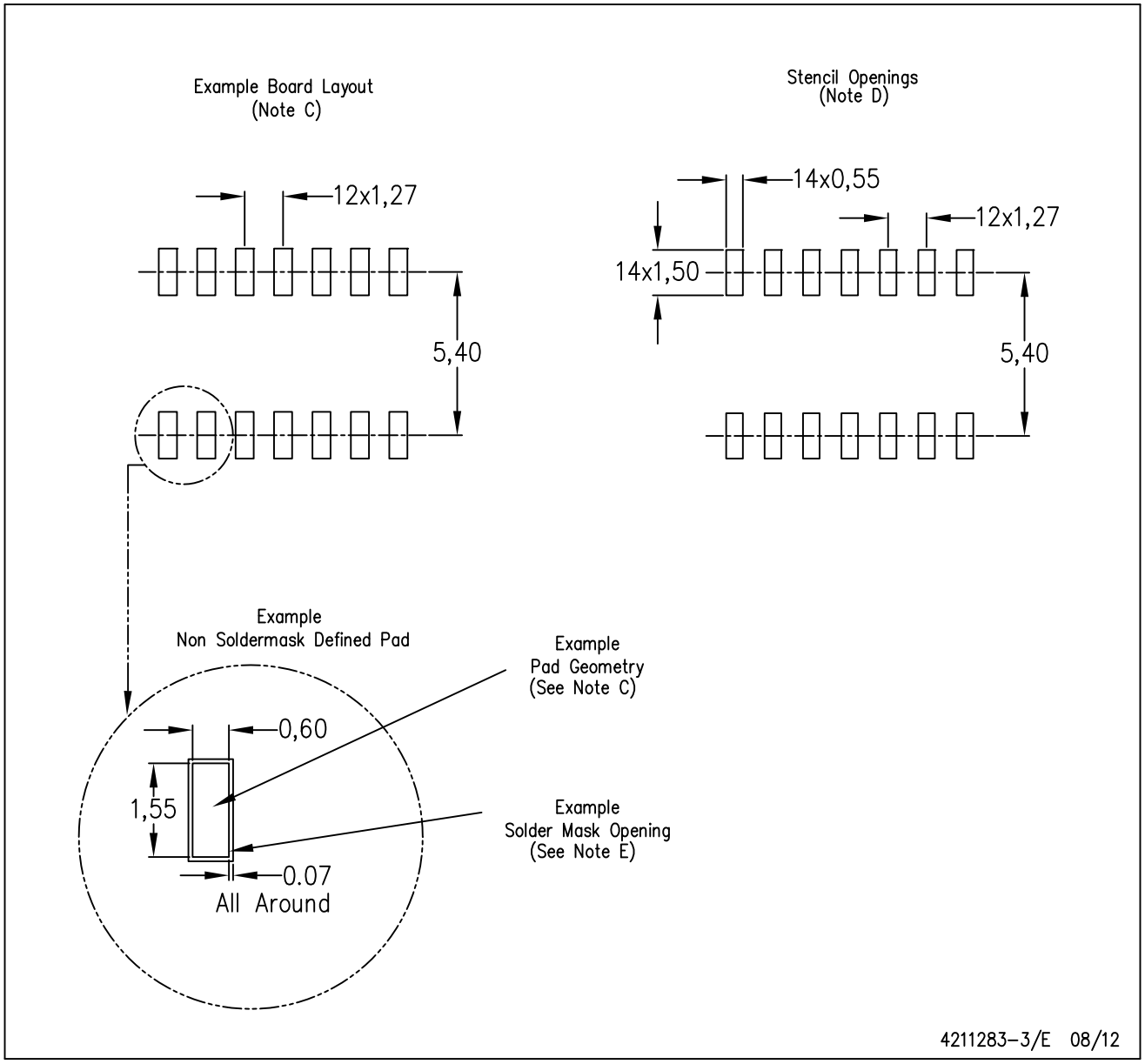
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE

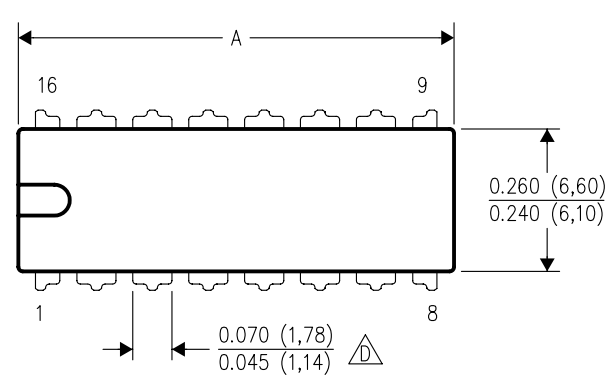


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

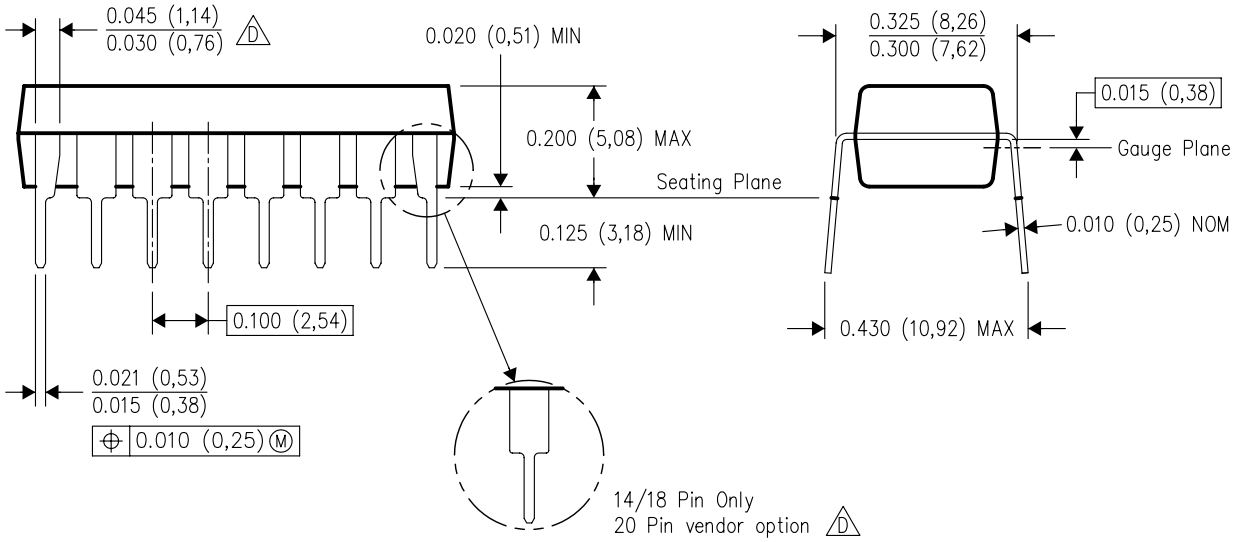
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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