

SN65518, SN75518 VACUUM FLUORESCENT DISPLAY DRIVERS

SLDS004B – MARCH 1983 – REVISED MAY 1990

- Each Device Drives 32 Lines
- 60-V Output Voltage Swing Capability
- 25-mA Output Source Current Capability
- High-Speed Serially Shifted Data Input
- Latches on All Driver Outputs

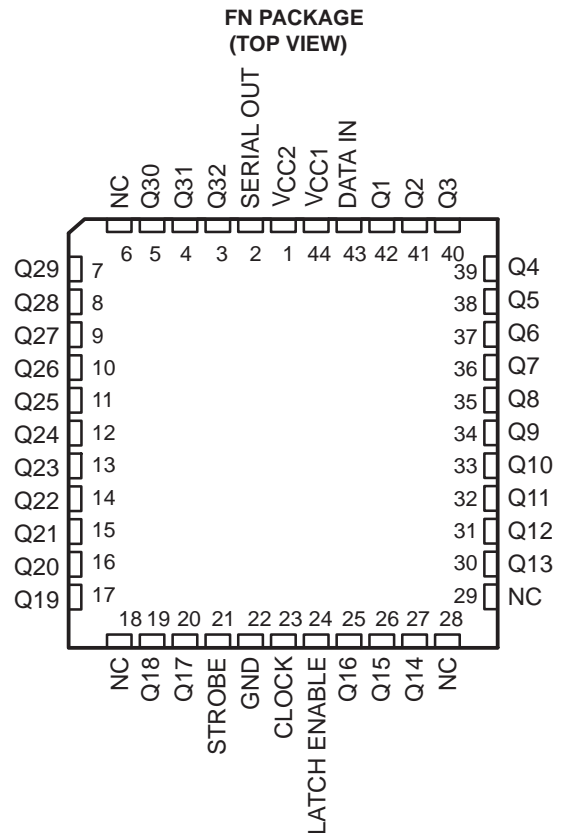
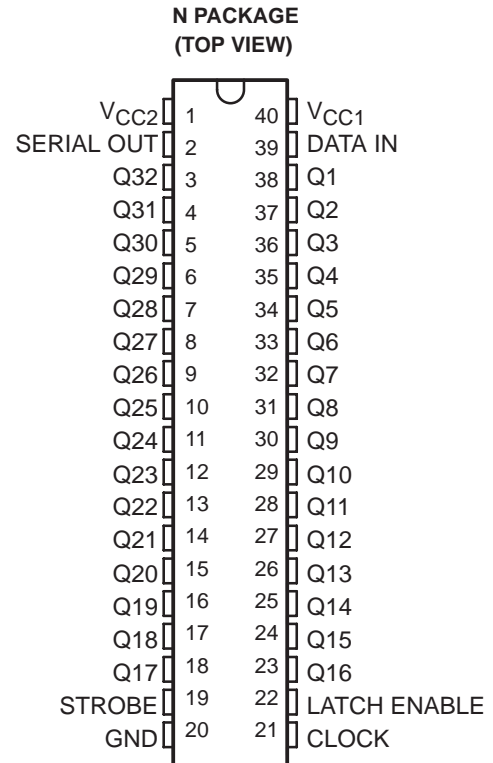
description

The SN65518 and SN75518 are monolithic BIDFET† integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display.

Each device consists of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. While LATCH ENABLE is high, parallel data is transferred to the output buffers through a 32-bit latch. Data present in the latch during the high-to-low transition of LATCH ENABLE is latched. When STROBE is low, all Q outputs are enabled. When STROBE is high, all Q outputs are low.

Serial data output from the shift register may be used to cascade additional devices. This output is not affected by LATCH ENABLE or STROBE.

The SN65518 is characterized for operation from -40°C to 85°C. The SN75518 is characterized for operation from 0°C to 70°C.



NC – No internal connection

† BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

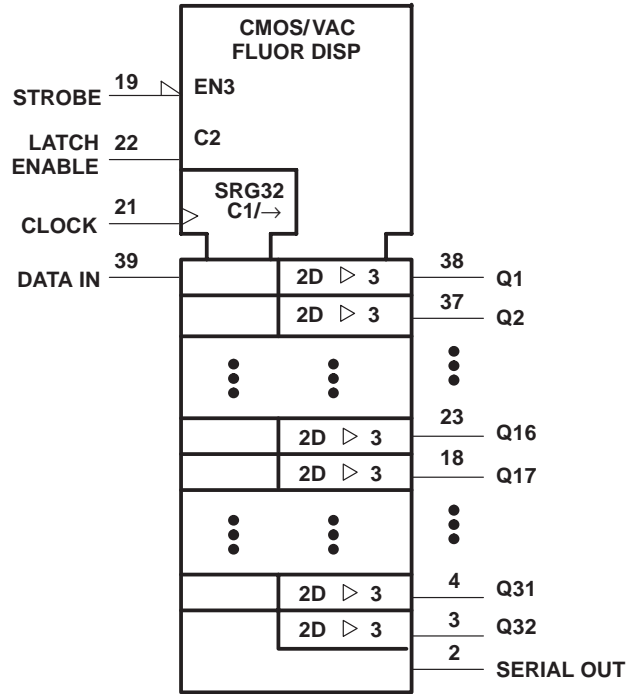


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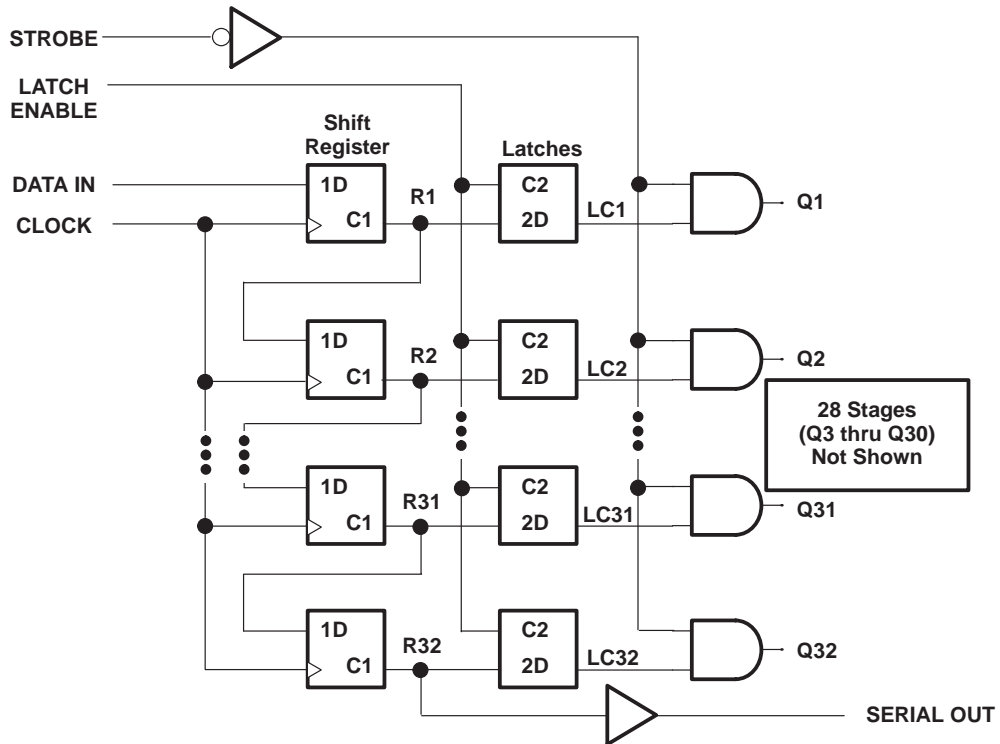
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the N package.

logic diagram (positive logic)



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FUNCTION TABLE

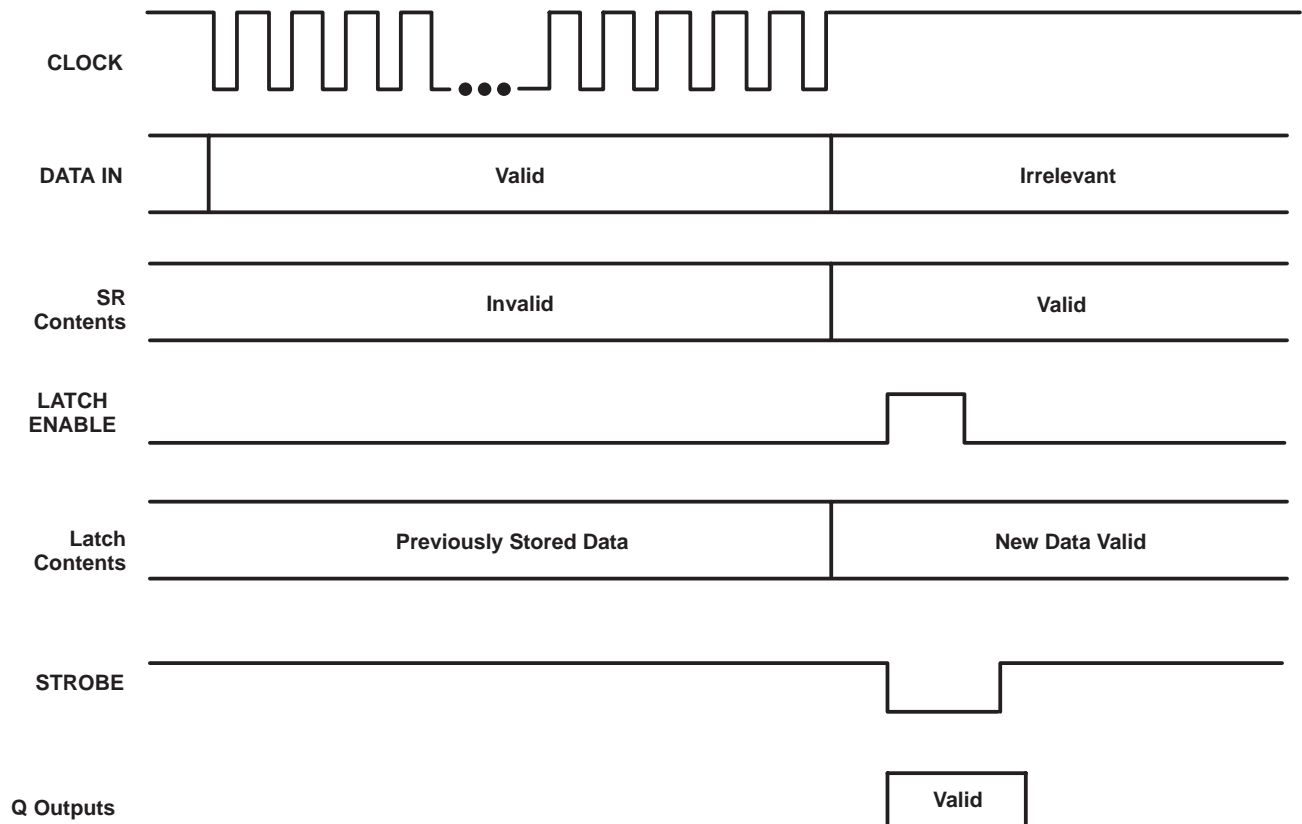
| FUNCTION | CONTROL INPUTS | | | SHIFT REGISTERS R1 THRU R32 | LATCHES LC1 THRU LC32 | OUTPUTS | |
|----------|----------------|-----------------|--------|--------------------------------|--------------------------------|---------|--------------------------------------|
| | CLOCK | LATCH ENABLE | STROBE | | | SERIAL | Q1 THRU Q32 |
| Load | ↑ No ↑ | X X | X X | Load and shift† No change | Determined by LATCH ENABLE‡ | R32 | Determined by STROBE |
| Latch | X X | L H | X X | As determined above | Stored data New data | R32 | Determined by STROBE |
| Strobe | X X | X X | H L | As determined above | Determined by LATCH ENABLE‡ | R32 | All L LC1 thru LC32, respectively |

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.

† R32 and the serial output take on the state of R31, R31 takes on the state of R30, ... R2 takes on the state of R1, and R1 takes on the state of the data input.

‡ New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

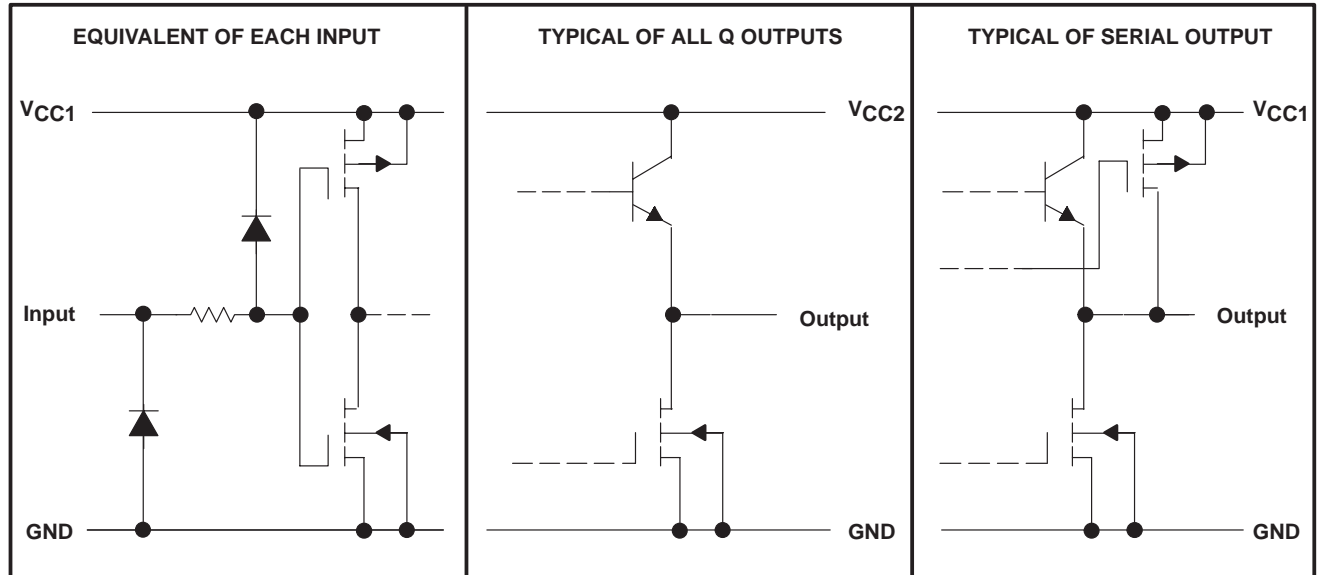
typical operating sequence



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schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|------------------------------|
| Supply voltage, V_{CC1} (see Note 1) | 15 V |
| Supply voltage, V_{CC2} | 70 V |
| Input voltage, V_I | V_{CC1} |
| Continuous total power dissipation | See Dissipation Rating Table |
| Operating free-air temperature range, T_A : SN65518 | -40°C to 85°C |
| SN75518 | 0°C to 70°C |
| Storage temperature range, T_{stg} | -65°C to 150°C |
| Case temperature for 10 seconds: FN package | 260°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package | 260°C |

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$ POWER RATING | $T_A = 85^\circ\text{C}$ POWER RATING |
|---------|---|---|--|--|
| FN | 1700 mW | 13.6 mW/°C | 1088 mW | 884 mW |
| N | 1250 mW | 10.0 mW/°C | 800 mW | 650 mW |

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recommended operating conditions, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| | | MIN | MAX | UNIT |
|--|--|------|-----|------------------|
| Supply voltage, V_{CC1} | | 4.5 | 15 | V |
| Supply voltage, V_{CC2} | | 0 | 60 | V |
| High-level input voltage, V_{IH} (see Figure 1) | $V_{CC1} = 4.5\text{ V}$ | 3.5 | | V |
| | $V_{CC1} = 15\text{ V}$ | 12 | | |
| Low-level input voltage, V_{IL} (see Figure 1) | | -0.3 | 0.8 | V |
| High-level output current, I_{OH} | | | -25 | mA |
| Low-level output current, I_{OL} | | | 2 | mA |
| Clock frequency, f_{clock} (see Figure 2) | $V_{CC1} = 10\text{ V to }15\text{ V}$ | 0 | 5 | MHz |
| | $V_{CC1} = 4.5\text{ V}$ | 0 | 1 | |
| Pulse duration, CLOCK high, $t_w(\text{CKH})$ | $V_{CC1} = 10\text{ V to }15\text{ V}$ | 100 | | ns |
| | $V_{CC1} = 4.5\text{ V}$ | 500 | | |
| Pulse duration, CLOCK low, $t_w(\text{CKL})$ | $V_{CC1} = 10\text{ V to }15\text{ V}$ | 100 | | ns |
| | $V_{CC1} = 4.5\text{ V}$ | 500 | | |
| Setup time, DATA IN before CLOCK \uparrow , t_{su} | $V_{CC1} = 10\text{ V to }15\text{ V}$ | 75 | | ns |
| | $V_{CC1} = 4.5\text{ V}$ | 150 | | |
| Hold time, DATA IN after CLOCK \uparrow , t_h | $V_{CC1} = 10\text{ V to }15\text{ V}$ | 75 | | ns |
| | $V_{CC1} = 4.5\text{ V}$ | 150 | | |
| Operating free-air temperature, T_A | SN65518 | -40 | 85 | $^\circ\text{C}$ |
| | SN75518 | 0 | 70 | |

electrical characteristics over recommended ranges of operating free-air temperature and V_{CC1} , $V_{CC2} = 60\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP \dagger | MAX | UNIT |
|-----------|---------------------------|---------------------------|---|------|---------------|------|---------------|
| V_{IK} | Input clamp voltage | $I_I = -12\text{ mA}$ | | | | -1.5 | V |
| V_{OH} | High-level output voltage | Q outputs | $I_{OH} = -25\text{ mA}$ | 57.5 | 58 | | V |
| | | SERIAL OUT | $V_{CC1} = 5\text{ V}$, $I_{OH} = -20\text{ }\mu\text{A}$ | 4.5 | 4.9 | 5 | |
| V_{OL} | Low-level output voltage | Q outputs | $I_{OL} = 1\text{ mA}$ | | | 5 | V |
| | | SERIAL OUT | $I_{OL} = 20\text{ }\mu\text{A}$ | 0.06 | 0.8 | | |
| I_{IH} | High-level input current | $V_{CC1} = 15\text{ V}$, | $V_I = 15\text{ V}$ | 0.1 | | 1 | μA |
| I_{IL} | Low-level input current | $V_{CC1} = 15\text{ V}$, | $V_I = 0\text{ V}$ | -0.1 | | -1 | μA |
| I_{CC1} | Supply current | $V_{CC1} = 4.5\text{ V}$ | | 1.8 | | 4 | mA |
| | | $V_{CC1} = 15\text{ V}$ | | 2 | | 5 | |
| I_{CC2} | Supply current | SN65518 | Outputs high, $T_A = -40^\circ\text{C}$ | | | 12 | mA |
| | | SN65518, SN75518 | Outputs high, $T_A = 0^\circ\text{C to MAX}$ | 7 | | 10 | |
| | | | Outputs low | 0.01 | | 0.5 | |

\dagger All typical values are at $T_A = 25^\circ\text{C}$.



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switching characteristics, $V_{CC2} = 60\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | MAX | UNIT |
|-----------|---|--------------------------|--|--------------|-----|---------------|
| t_d | Delay time, CLOCK to DATA OUT | $V_{CC1} = 4.5\text{ V}$ | $C_L = 15\text{ pF}$, See Figure 4 | 600 | | ns |
| | | $V_{CC1} = 15\text{ V}$ | | 150 | | |
| t_{DHL} | Delay time, high-to-low-level Q output | From LATCH ENABLE | $V_{CC1} = 4.5\text{ V}$ | See Figure 5 | | μs |
| | | From STROBE | | See Figure 6 | | |
| | | From LATCH ENABLE | $V_{CC1} = 15\text{ V}$ | See Figure 5 | | |
| | | From STROBE | | See Figure 6 | | |
| t_{DLH} | Delay time, low-to-high-level Q output | From LATCH ENABLE | $V_{CC1} = 4.5\text{ V}$ | See Figure 5 | | μs |
| | | From STROBE | | See Figure 6 | | |
| | | From LATCH ENABLE | $V_{CC1} = 15\text{ V}$ | See Figure 5 | | |
| | | From STROBE | | See Figure 6 | | |
| t_{THL} | Transition time, high-to-low-level Q output | $V_{CC1} = 4.5\text{ V}$ | See Figure 6 | 3 | | μs |
| | | $V_{CC1} = 15\text{ V}$ | | 1.5 | | |
| t_{TLH} | Transition time, low-to-high-level Q output | $V_{CC1} = 4.5\text{ V}$ | See Figure 6 | 2.5 | | μs |
| | | $V_{CC1} = 15\text{ V}$ | | 0.75 | | |

RECOMMENDED OPERATING CONDITIONS

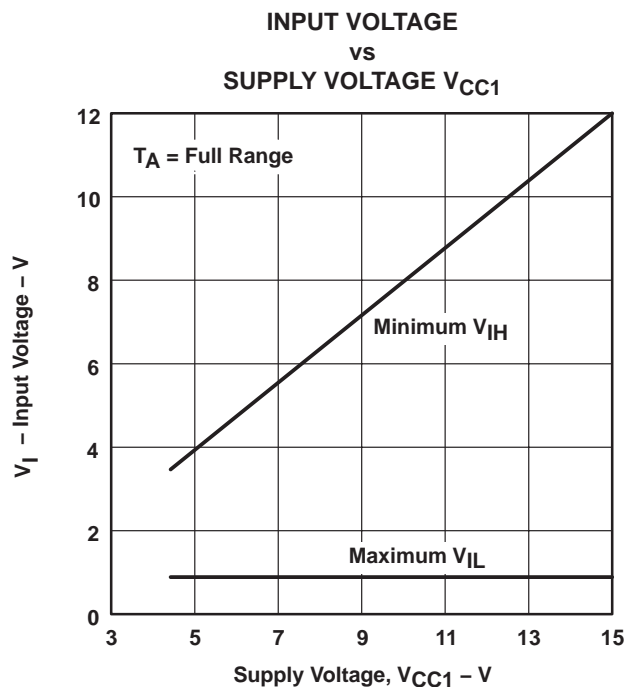


Figure 1

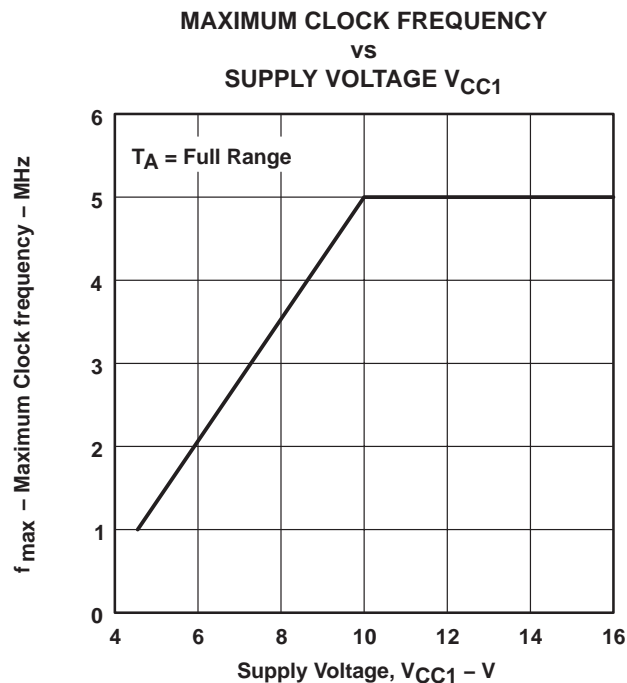


Figure 2



PARAMETER MEASUREMENT INFORMATION†

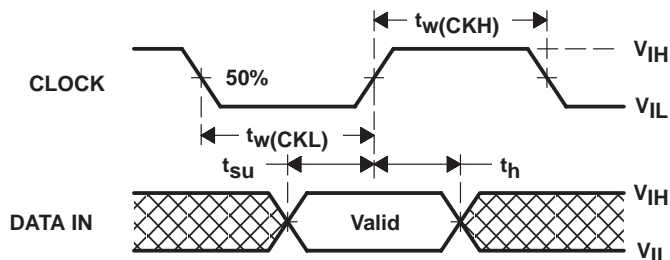


Figure 3. Input Timing Waveforms

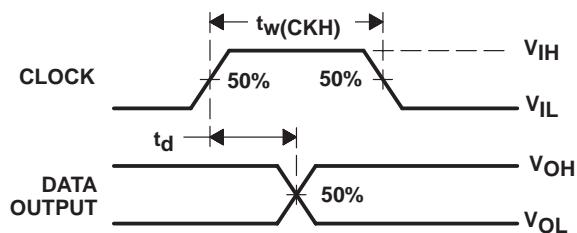


Figure 4. Data Output Switching Times

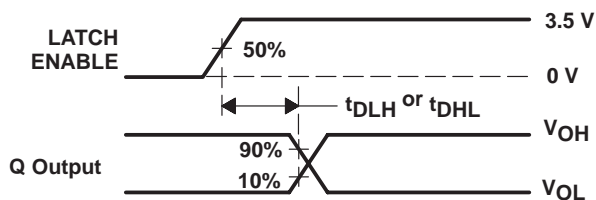


Figure 5. Q Output Switching Times

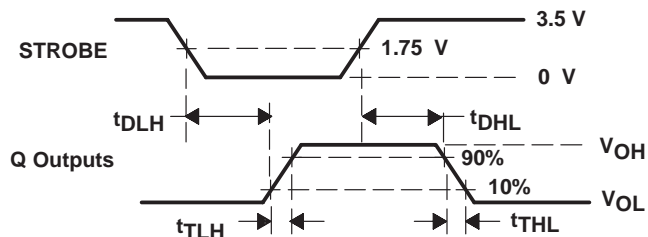


Figure 6. Switching Time Voltage Waveforms

† For testing purposes, all input pulses have maximum rise and fall times of 30 ns.

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