

9-CHANNEL RS-422 / RS-485 TRANSCEIVER

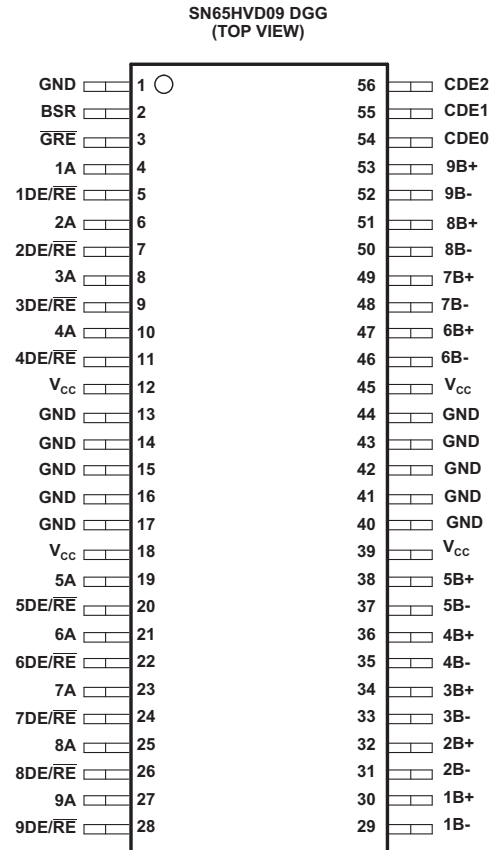
 Check for Samples: [SN65HVD09-EP](#)

FEATURES

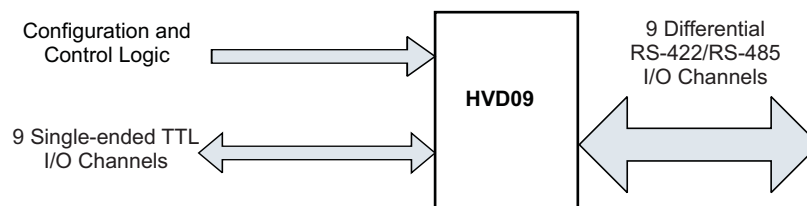
- Designed to Operate at up to 20 Million Data Transfers per Second on Each RS-422/RS-485 Channel
- SN65HVD09 Packaged in Thin Shrink Small-Outline Package with 0.5-mm Pin Pitch
- ESD Protection on Bus Pins Exceeds 12kV
- Low Disabled Supply Current 8 mA Typ
- Thermal Shutdown Protection
- Positive- and Negative-Current Limiting
- Power-Up/Down Glitch Protection

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability



Terminals 13 through 17, and 40 through 44 are connected together to the package lead frame and signal ground.



DESCRIPTION

The SN65HVD09 is a 9-channel RS-422 / RS-485 transceiver suitable for industrial applications. It offers improved switching performance, a small package, and high ESD protection. The precise skew limits ensures that the propagation delay times, not only from channel-to-channel but from device-to-device, are closely matched for the tight skew budgets associated with high-speed parallel data buses.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN65HVD09-EP

SLLSEA3 – DECEMBER 2011

www.ti.com

Patented thermal enhancements are used in the thin shrink, small-outline package (TSSOP), allowing operation over the industrial temperature range. The TSSOP package offers very small board area requirements while reducing the package height to 1 mm. This provides more board area and allows component mounting to both sides of the printed circuit boards for low-profile, space-restricted applications such as small form-factor hard disk drives.

The HVD09 can withstand electrostatic discharges exceeding 12 kV using the human-body model, and 600 V using the machine model on the RS-485 I/O terminals. This provides protection from the noise that can be coupled into external cables. The other terminals of the device can withstand discharges exceeding 4 kV and 400 V respectively.

Each of the nine half-duplex channels of the HVD09 is designed to operate with either RS-422 or RS-485 communication networks.

The SN65HVD09 is characterized for operation from -40°C to 85°C .



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–40°C to 85°C	TSSOP-DGG	SN65HVD09IDGGREP	SN65HVD09EP	V62/12607-01XE

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PIN FUNCTIONS

NAME	PIN NO.	LOGIC LEVEL	I/O	TERMINATION	DESCRIPTION
1A to 9A	4,6,8,10,19,21,23,25,27	TTL	I/O	Pullup	1A to 9A carry data to and from the communication controller.
1B– to 9B–	29,31,33,35,37,46,48,50,52	RS-485	I/O	Pulldown	1B– to 9B– are the inverted data signals of the balanced pair to/from the bus.
1B+ to 9B+	30,32,34,36,38,47,49,51,53	RS-485	I/O	Pullup	1B+ to 9B+ are the noninverted data signals of the balanced pair to/from the bus.
BSR	2	TTL	Input	Pullup	BSR is the bit significant response. BSR disables receivers 1 through 8 and enables wired-OR drivers when BSR and DE/RE and CDE1 or CDE2 are high. Channel 9 is placed in a high-impedance state with BSR high.
CDE0	54	TTL	Input	Pulldown	CDE0 is the common driver enable 0. Its input signal enables all drivers when CDE0 and 1DE/RE – 9DE/RE are high.
CDE1	55	TTL	Input	Pulldown	CDE1 is the common driver enable 1. Its input signal enables drivers 1 to 4 when CDE1 is high and BSR is low.
CDE2	56	TTL	Input	Pulldown	CDE2 is the common driver enable 2. When CDE2 is high and BSR is low, drivers 5 to 8 are enabled.
$\overline{\text{CRE}}$	3	TTL	Input	Pullup	$\overline{\text{CRE}}$ is the common receiver enable. When high, CRE disables receiver channels 5 to 9.
1DE/RE to 9DE/RE	5,7,9,11,20,22,24,26,28	TTL	Input	Pullup	1DE/RE–9DE/RE are direction controls that transmit data to the bus when it and CDE0 are high. Data is received from the bus when 1DE/RE–9DE/RE and CRE and BSR are low and CDE1 and CDE2 are low.
GND	1,13,14,15,16,17,40,41,42,43,44	NA	Power	NA	GND is the circuit ground. All GND terminals except terminal 1 are physically tied to the die pad for improved thermal conductivity. ⁽¹⁾
V _{CC}	12,18,39,45	NA	Power	NA	Supply voltage

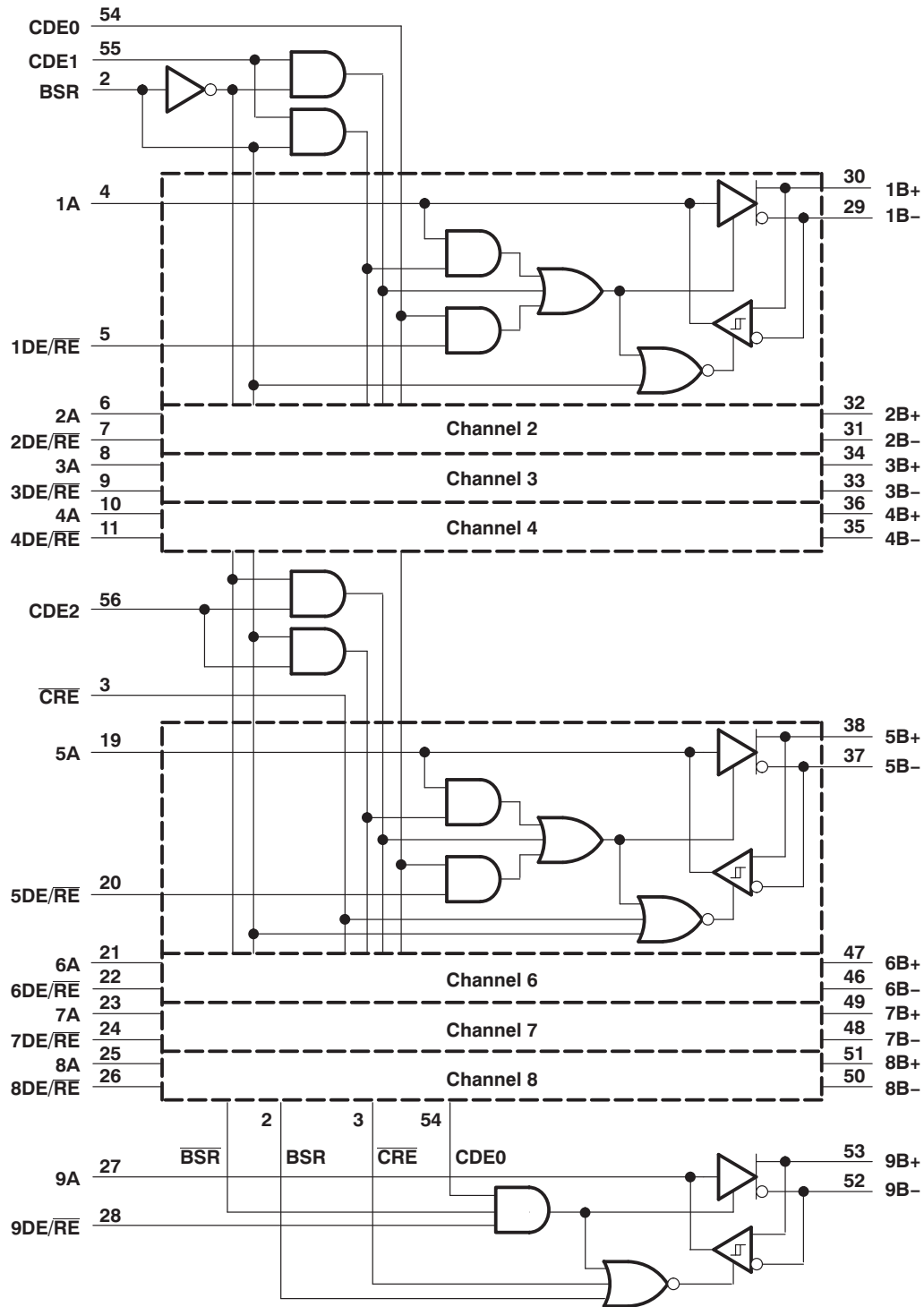
- (1) Terminal 1 must be connected to signal ground for proper operation.

SN65HVD09-EP

SLLSEA3 – DECEMBER 2011

www.ti.com

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

		VALUE	UNIT
V _{CC}	Supply voltage range ⁽²⁾	–0.3 to 6	V
	Bus voltage range	–10 to 15	V
	Data I/O and control (A side) voltage range	–0.3 to V _{CC} +0.5	V
I _O	Receiver output current	±40	mA
Electrostatic discharge	B side and GND, ESD HBM	12	kV
	B side and GND, ESD MM	400	V
	All terminals, ESD HBM	4	kV
	All terminals, ESD MM	400	V
Continuous total power dissipation ⁽³⁾		Internally Limited	

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the GND terminals.
- (3) The maximum operating junction temperature is internally limited. Use the Dissipation Rating Table to operate below this temperature.

DISSIPATION RATINGS

PACKAGE	T _A ≤ 25°C	OPERATING FACTOR ⁽¹⁾ ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
DGG	2500 mW	20 mW/°C	1600 mW	1300 mW

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

PACKAGE THERMAL CHARACTERISTICS

		MIN	NOM	MAX	UNIT
θ _{JA}	Junction-to-ambient thermal resistance	DGG, board-mounted, no air flow			°C/W
θ _{JC}	Junction-to-case thermal resistance	DGG			°C/W
T _{SD}	Thermal shutdown temperature				°C

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.75	5	5.25	V
V _{IH}	High-level input voltage	2		0.8	V
V _{IL}	Low-level input voltage				
V _O , V _I , or V _{IC}	Voltage at any bus terminal (separately or common-mode)	–7		12	V
I _O	Output current	Driver	–60	60	mA
		Receiver	–8	8	mA
T _A	Operating free-air temperature	–40		85	°C

- (1) n = 1 - 9

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN65HVD09			UNIT
			MIN	TYP ⁽¹⁾	MAX	
V _{OD} Driver differential output voltage magnitude	RS-422 load, R _L = 100 Ω	See Figure 1	0.56	1.6	V	
	RS-485 load, R _L = 54 Ω		1.4			
	Pull-Up Pull-Down Load	See Figure 2	1	1.5		
V _{OH} High-level output voltage	A side, I _{OH} = -8 mA, V _{ID} = 200 mV,	See Figure 4	4	4.5	V	
	B side,	See Figure 2		3	V	
V _{OL} Low-level output voltage	A side, I _{OH} = 8 mA, V _{ID} = -200 mV,	See Figure 4		0.6	0.8	V
	B side,	See Figure 2		1		V
V _{IT+} Receiver positive-going differential input threshold voltages	I _{OH} = -8 mA,	See Figure 4			0.2	V
V _{IT-} Receiver negativegoing differential input threshold voltage	I _{OL} = 8 mA,	See Figure 4	-0.2			V
V _{hys} Receiver input hysteresis (V _{IT+} - V _{IT-})	V _{CC} = 5 V, T _A = 25°C		24	45		mV
I _I Bus input current	V _{IH} = 12 V, V _{CC} = 5 V,	Other input at 0 V			1	mA
	V _{IH} = 12 V, V _{CC} = 0,				1	mA
	V _{IH} = -7 V, V _{CC} = 5 V,		-0.8	-0.4		mA
	V _{IH} = -7 V, V _{CC} = 0,		-0.8	-0.3		mA
I _{IH} High-level input current	nA, BSR, DE/ \overline{RE} , and \overline{CRE} ,	V _{IH} = 2 V	-100			μA
	CDE0, CDE1, and CDE2,	V _{IH} = 2V			100	μA
I _{IL} Low-level input current	nA, BSR, DE/ \overline{RE} , and \overline{CRE} ,	V _{IL} = 0.8 V	-100			μA
	CDE1, CDE1, and CDE2,	V _{IL} = 0.8 V			100	μA
I _{OS} Short circuit output current	nB+ or nB-				±260	mA
I _{OZ} High-impedance-state output current	nA		See I _{IH} and I _{IL}			
	nB+ or nB-		See I _{II}			
I _{CC} Supply current	Disabled				10	mA
	All drivers enabled, no load				60	
	All receivers enabled, no load				45	
C _O Output capacitance	nB+ or nB- to GND			18		pF
C _{pd} Power dissipation capacitance ⁽²⁾	Receiver			40		pF
	Driver			100		

 (1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

 (2) C_{pd} determines the no-load dynamic supply current consumption, I_S = C_{PD} × V_{CC} × f + I_{CC}

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN65HVD09			UNIT
		MIN	TYP ⁽¹⁾	MAX	
t_{pd} Propagation delay time, t_{PHL} or t_{PLH} (see Figure 2 and Figure 3)		2.5		13.5	ns
$t_{sk(p)}$ Pulse skew, $ t_{PHL} - t_{PLH} $				5	ns
t_f Fall time	S1 to B, See Figure 3		4		ns
t_r Rise time	See Figure 3		8		ns
t_{en} Enable time, control inputs to active output				50	ns
t_{dis} Disable time, control inputs to high-impedance output				225	ns
t_{PHZ} Propagation delay time, high-level to high-impedance output	See Figure 6 and Figure 7		17	225	ns
t_{PLZ} Propagation delay time, low-level to high-impedance output			25	225	ns
t_{PZH} Propagation delay time, high-impedance to high-level output			17	50	ns
t_{PZL} Propagation delay time, high-impedance to low-level output			17	50	ns

(1) All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN65HVD09			UNIT
		MIN	TYP ⁽¹⁾	MAX	
t_{pd} Propagation delay time, t_{PHL} or t_{PLH} (see Figure 2 and Figure 3)		8		14.5	ns
$t_{sk(lim)}$ Skew limit, maximum t_{pd} – minimum t_{pd} ⁽²⁾				5	ns
$t_{sk(p)}$ Pulse skew, $ t_{PHL} - t_{PLH} $			0.6	5	ns
t_t Transition time (t_r or t_f)	See Figure 5		2		ns
t_{en} Enable time, control inputs to active output			31		ns
t_{dis} Disable time, control inputs to high-impedance output			41		ns
t_{PHZ} Propagation delay time, high-level to high-impedance output	See Figure 8 and Figure 9		34		ns
t_{PLZ} Propagation delay time, low-level to high-impedance output			14		ns
t_{PZH} Propagation delay time, high-impedance to high-level output			30		ns
t_{PZL} Propagation delay time, high-impedance to low-level output			30		ns

(1) All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

(2) This parameter is applicable at one V_{CC} and operating temperature within the recommended operating conditions and to any two devices.

PARAMETER MEASUREMENT INFORMATION

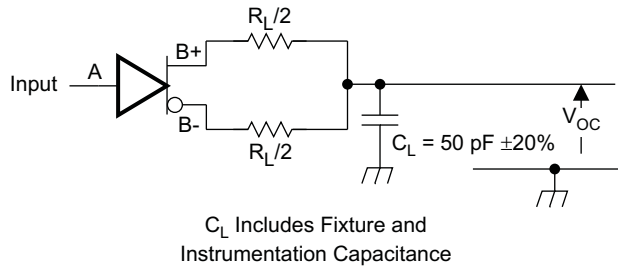
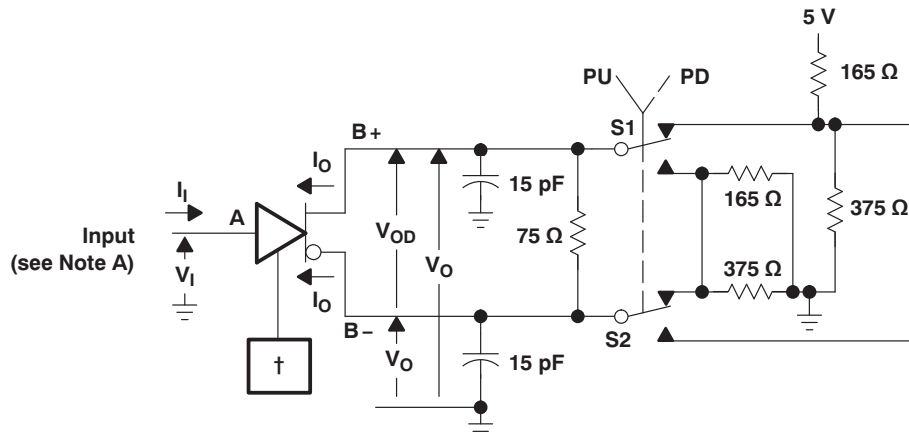


Figure 1. Driver Test Circuit, RS-422 and RS-485 Loading



† CDEO and DE/RE are at 2 V, BSR is at 0.8V, and all others are open.
‡ All nine drivers are enabled, similarly loaded, and switching.

Figure 2. Driver Test Circuit, Pull-Up and Pull-Down Loading[†]

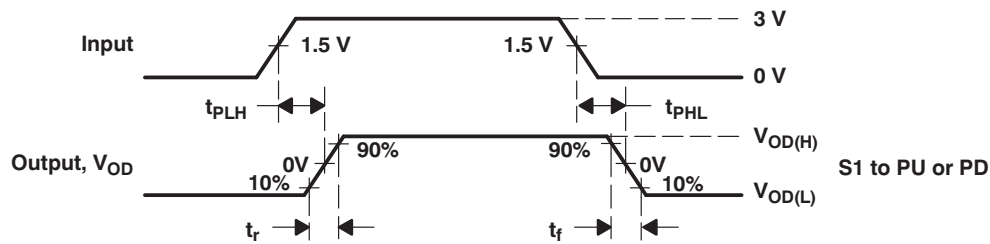
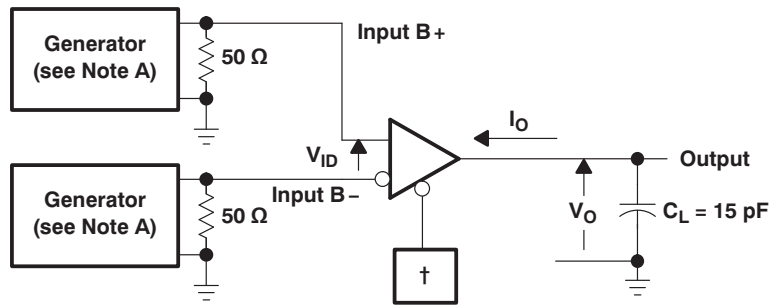


Figure 3. Driver Delay and Transition Time Test Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



† CDE0, CDE1, CDE2, BSR, CRE, and DE/RE at 0.8 V

‡ All nine receivers are enabled and switching.

Figure 4. Receiver Propagation Delay and Transition Time Test Circuit

- A. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50 \Omega$.
- B. All resistances are in Ω and $\pm 5\%$, unless otherwise indicated.
- C. All capacitances are in pF and $\pm 10\%$, unless otherwise indicated.
- D. All indicated voltages are ± 10 mV.

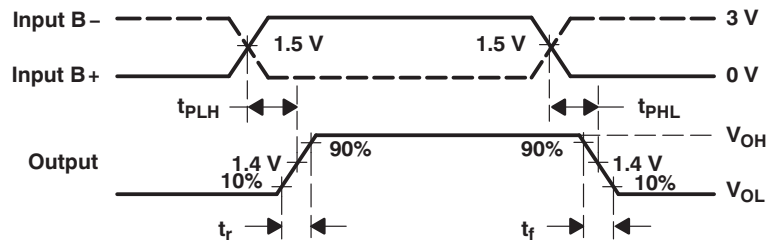
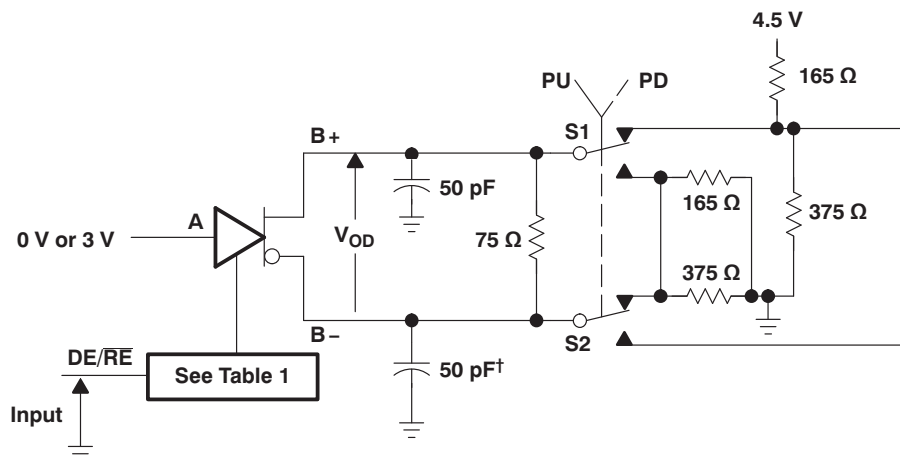


Figure 5. Receiver Delay and Transition Time Waveforms

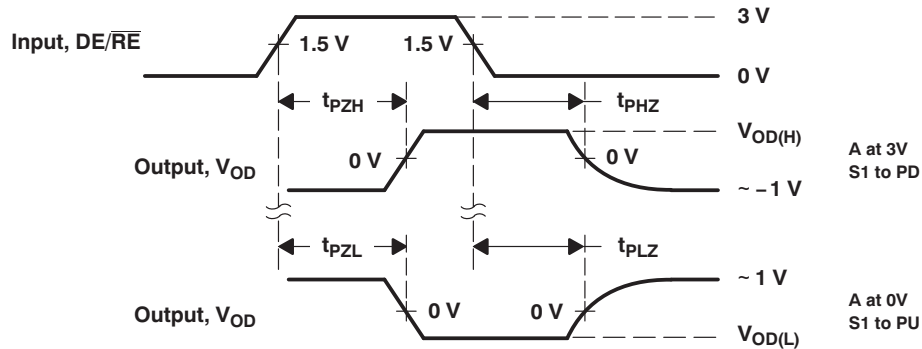


† Includes probe and jig capacitance in two places.

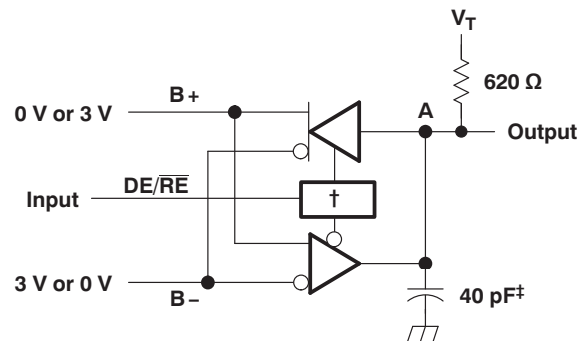
Figure 6. Driver Enable and Disable Time Test Circuit

Table 1. Enabling for Driver Enable and Disable Time

DRIVER	BSR	CDE0	CDE1	CDE2	$\overline{\text{CRE}}$
1–8	H	H	L	L	X
9	L	H	H	H	H


Figure 7. Driver Enable Time Waveforms

- NOTES:
- A. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50 \Omega$.
 - B. All resistances are in Ω and $\pm 5\%$, unless otherwise indicated.
 - C. All capacitances are in pF and $\pm 10\%$, unless otherwise indicated.
 - D. All indicated voltages are ± 10 mV.



† CDE0 is high, CDE1, CDE2, BSR, and $\overline{\text{CRE}}$ are low, all others are open.

‡ Includes probe and jig capacitance.

Figure 8. Receiver Enable and Disable Time Test Circuit

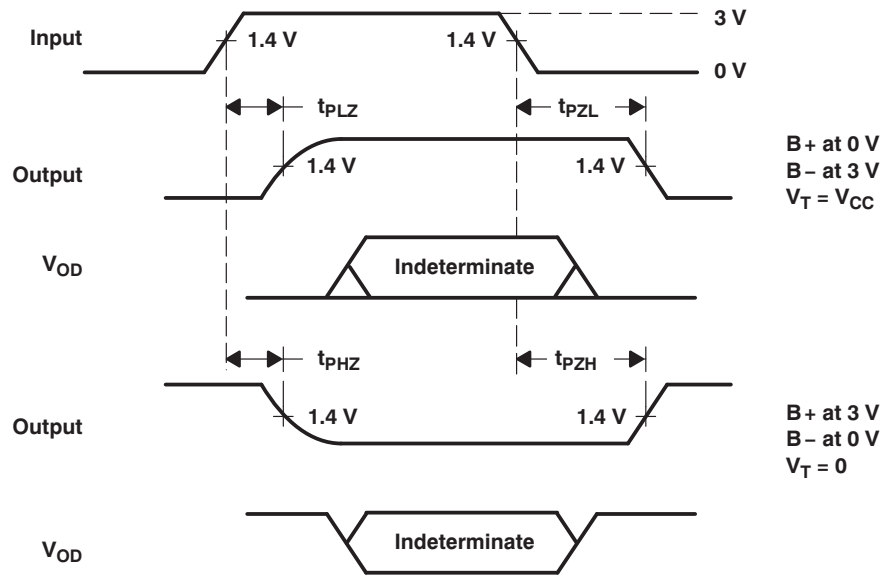


Figure 9. Receiver Enable and Disable Time Waveforms

- NOTES:
- All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50 \Omega$.
 - All resistances are in Ω and $\pm 5\%$, unless otherwise indicated.
 - All capacitances are in pF and $\pm 10\%$, unless otherwise indicated.
 - All indicated voltages are ± 10 mV.

TYPICAL CHARACTERISTICS

AVERAGE SUPPLY CURRENT
vs
FREQUENCY

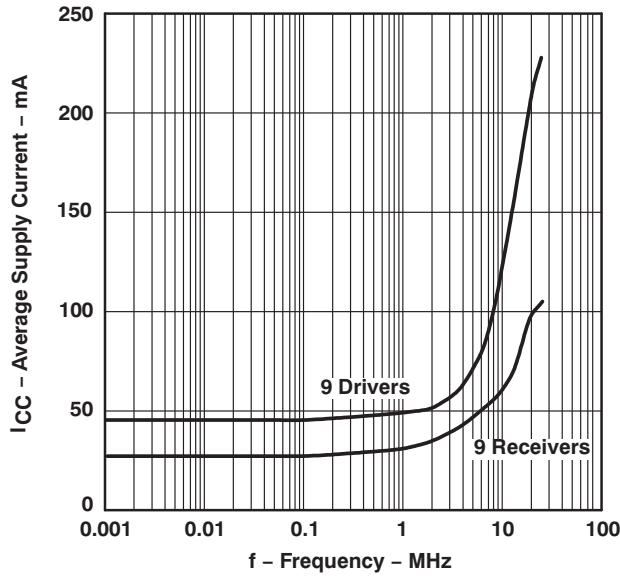


Figure 10.

LOGIC INPUT CURRENT
vs
INPUT VOLTAGE

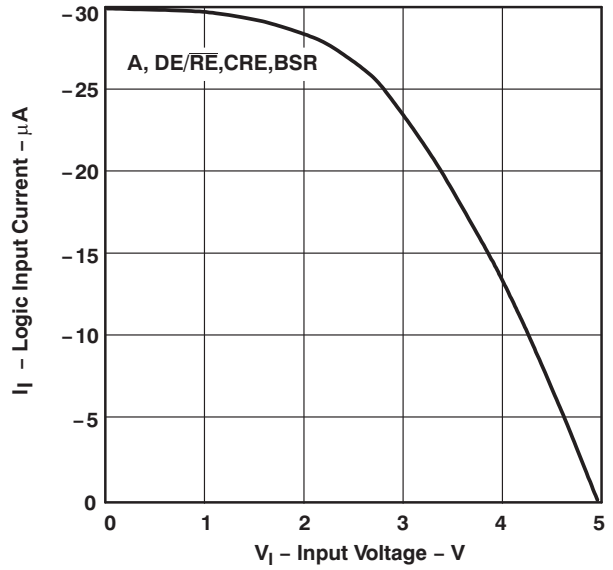


Figure 11.

BUS
INPUT CURRENT
vs
INPUT VOLTAGE

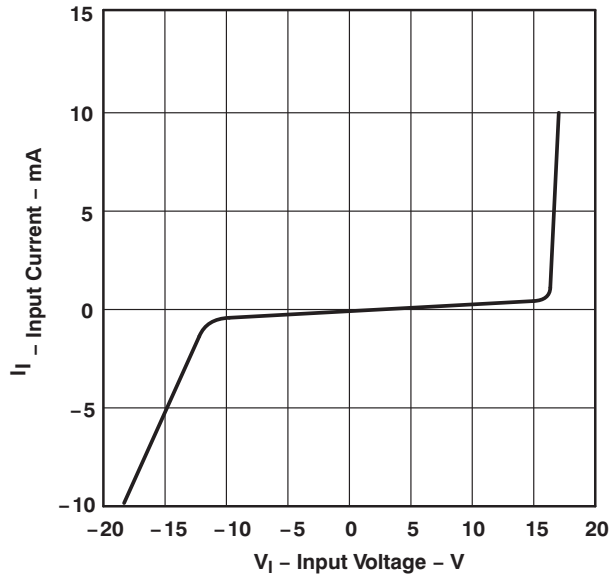


Figure 12.

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

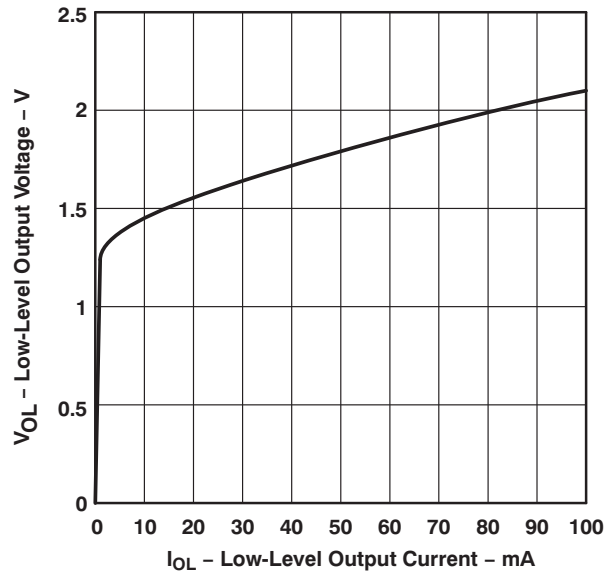
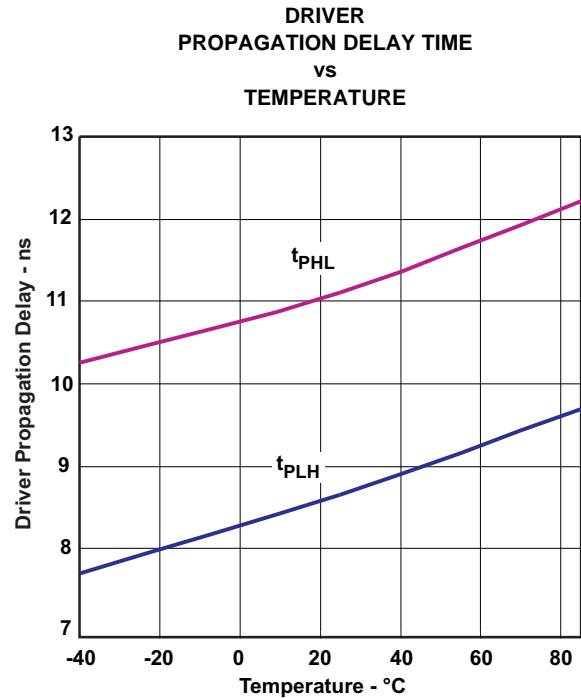
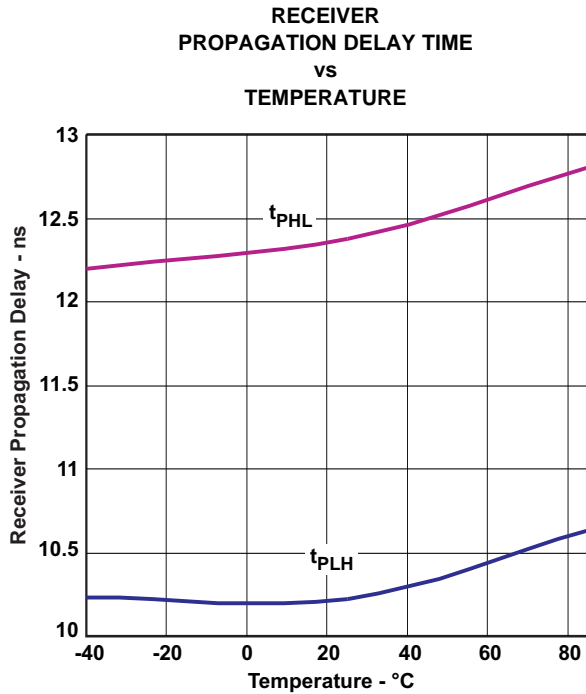
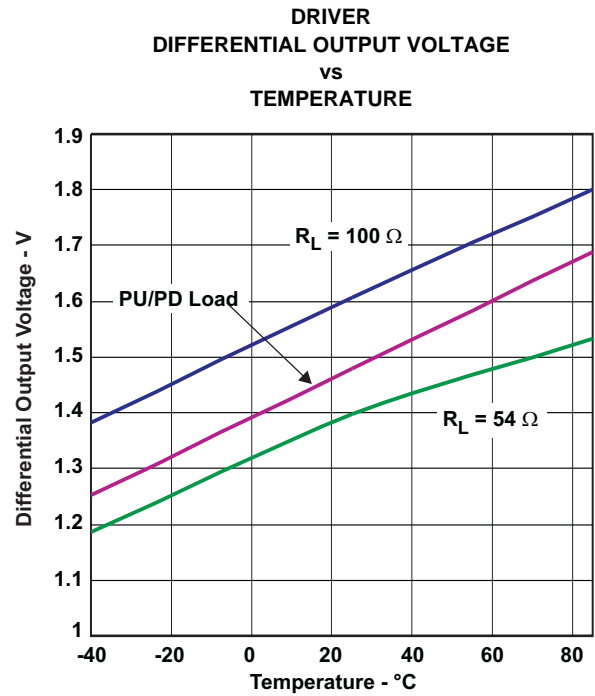
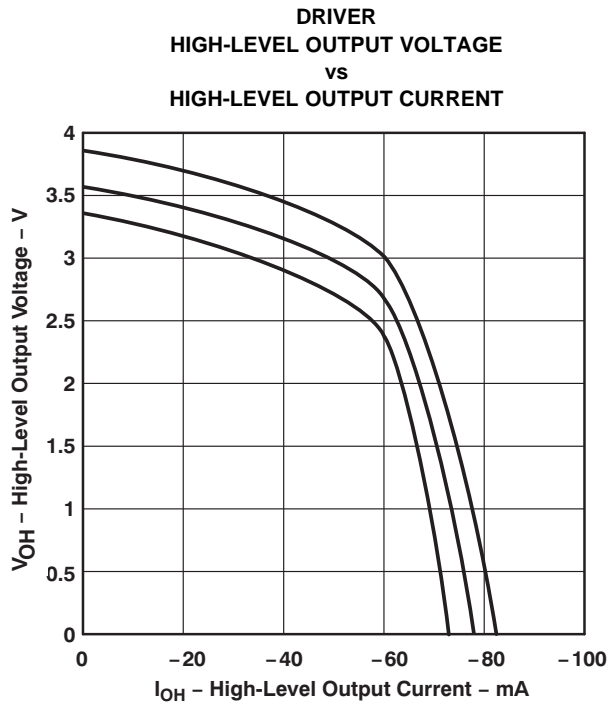


Figure 13.

TYPICAL CHARACTERISTICS (continued)



TYPICAL CHARACTERISTICS (continued)

DRIVER
OUTPUT CURRENT
vs
SUPPLY VOLTAGE

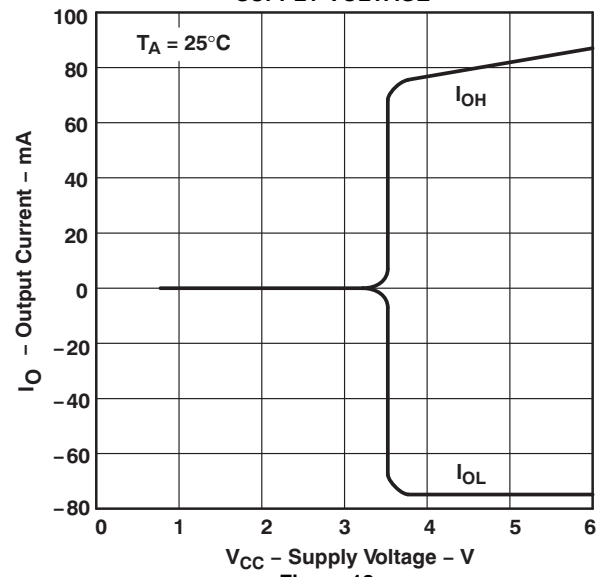
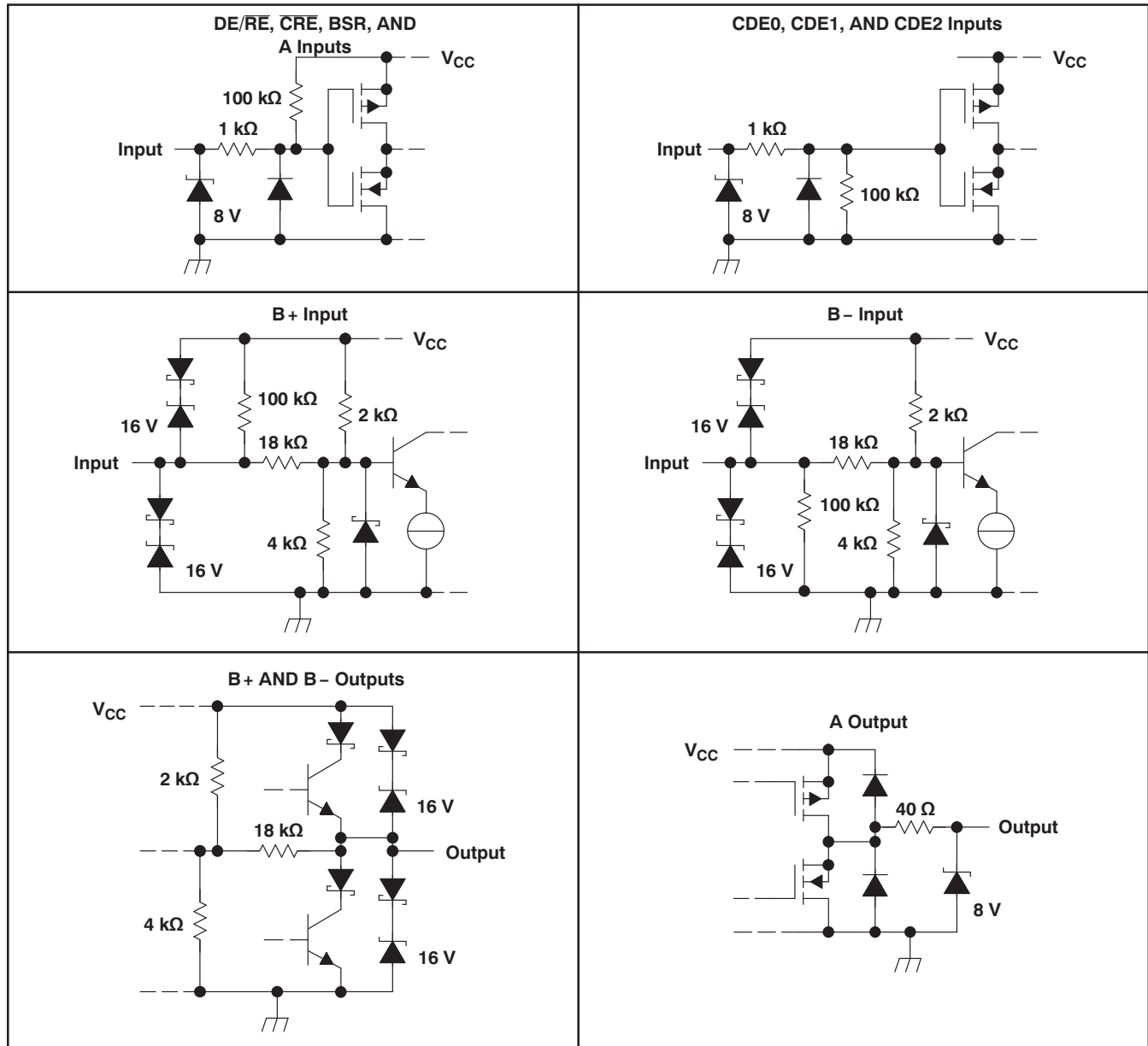


Figure 18.

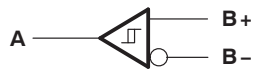
TYPICAL CHARACTERISTICS (continued)
SCHEMATICS OF INPUTS AND OUTPUTS



APPLICATION INFORMATION

FUNCTION TABLES

RECEIVER



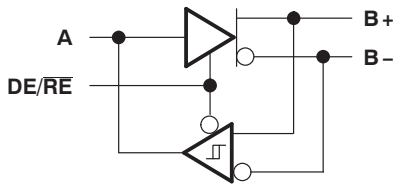
INPUTS		OUTPUT A
B+ ¹	B- ¹	
L	H	L
H	L	H

DRIVER



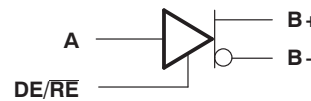
INPUT A	OUTPUTS	
	B+	B-
L	L	H
H	H	L

TRANSCEIVER



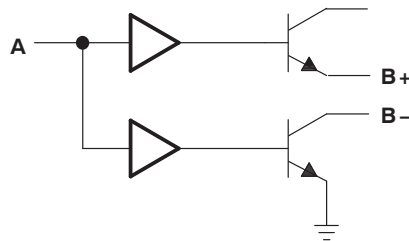
DE/RE	INPUTS			OUTPUTS		
	A	B+ ¹	B- ¹	A	B+	B-
L	-	L	H	L	-	-
L	-	H	L	H	-	-
H	L	-	-	-	L	H
H	H	-	-	-	H	L

DRIVER WITH ENABLE



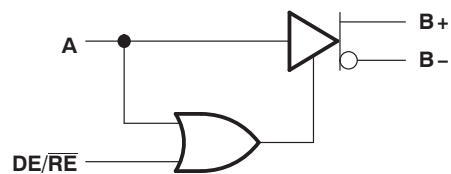
DE/RE	INPUTS		OUTPUTS	
	A	B+	B-	
L	L	Z	Z	
L	H	Z	Z	
H	L	L	H	
H	H	H	L	

WIRED-OR DRIVER



INPUT A	OUTPUTS	
	B+	B-
L	Z	Z
H	H	L

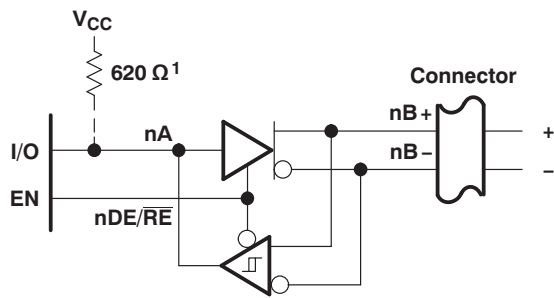
TWO-ENABLE INPUT DRIVER



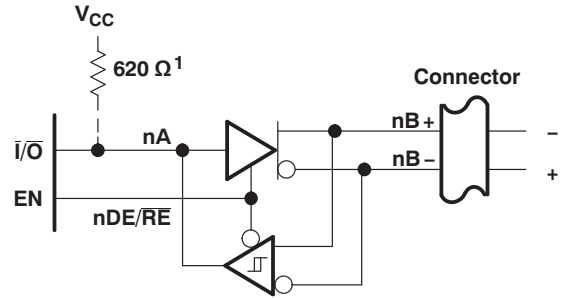
DE/RE	INPUTS		OUTPUTS	
	A	B+	B-	
L	L	Z	Z	
L	H	H	L	
H	L	L	H	
H	H	H	L	

NOTE: H = high level, L = low level, X = irrelevant, Z = high impedance (off)

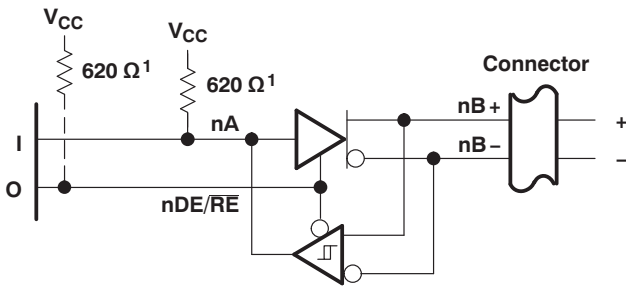
- (1) An H in this column represents a voltage of 200 mV or higher than the other bus input. An L represents a voltage of 200 mV or lower than the other bus input. Any voltage less than 200 mV results in an indeterminate receiver output.



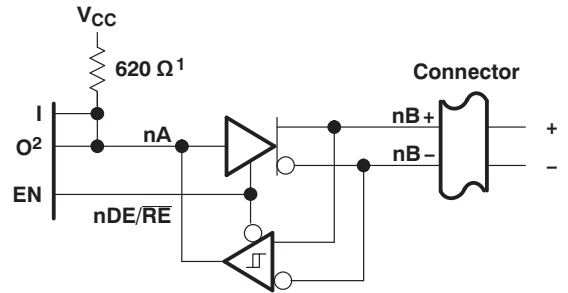
(a) ACTIVE-HIGH BIDIRECTIONAL I/O WITH SEPARATE ENABLE



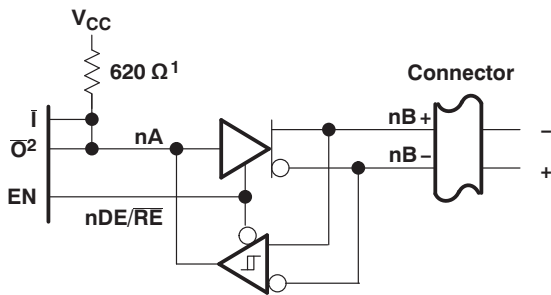
(b) ACTIVE-LOW BIDIRECTIONAL I/O WITH SEPARATE ENABLE



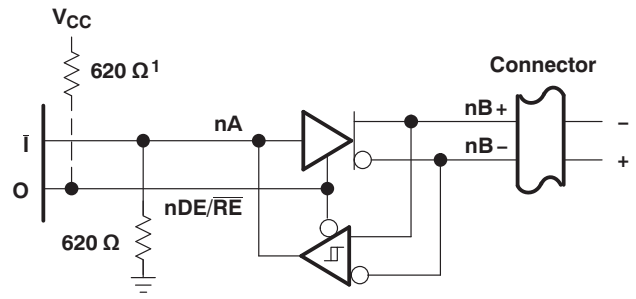
(c) WIRED-OR DRIVER AND ACTIVE-HIGH INPUT



(d) SEPARATE ACTIVE-HIGH INPUT, OUTPUT, AND ENABLE



(e) SEPARATE ACTIVE-LOW INPUT AND OUTPUT AND ACTIVE-HIGH ENABLE



(f) WIRED-OR DRIVER AND ACTIVE-LOW INPUT

1: When 0 is open drain
2: Must be open-drain or 3-state output

- (1) When 0 is open drain
- (2) Must be open-drain or 3-state output

NOTE: The BSR, $\overline{\text{CRE}}$, A, and $\text{DE}/\overline{\text{RE}}$ inputs have internal pullup resistors. CDE0, CDE1, and CDE2 have internal pulldown resistors.

Figure 19. Typical Transceiver Connections

CHANNEL LOGIC CONFIGURATIONS WITH CONTROL INPUT LOGIC

The following logic diagrams show the positive-logic representation for all combinations of control inputs. The control inputs are from MSB to LSB; the BSR, CDE0, CDE1, CDE2, and CRE bit values are shown below the diagrams. Channel 1 is at the top of the logic diagrams; channel 9 is at the bottom of the logic diagrams.

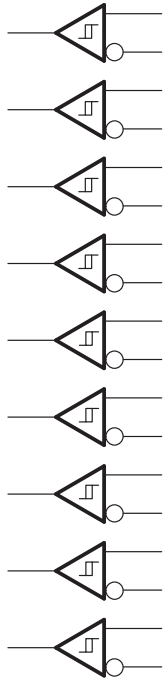


Figure 19. 00000

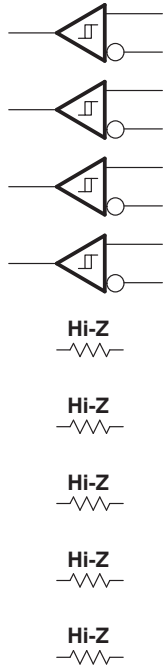


Figure 20. 00001

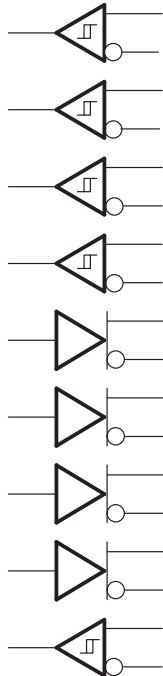


Figure 21. 00010

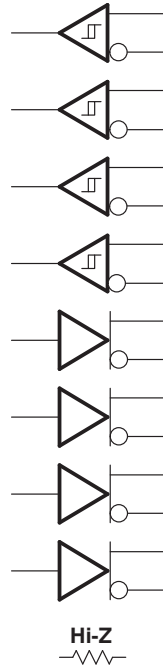


Figure 22. 00011

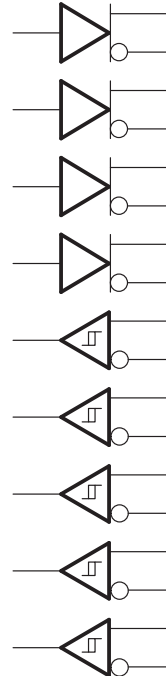


Figure 23. 00100

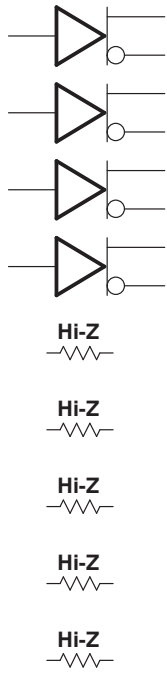


Figure 24. 00101

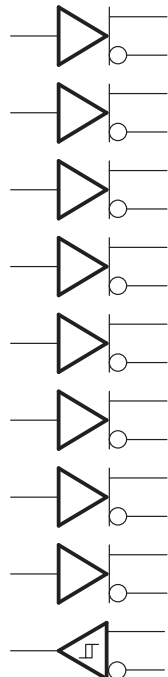


Figure 25. 00110

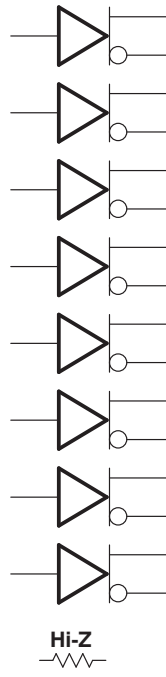


Figure 26. 00111

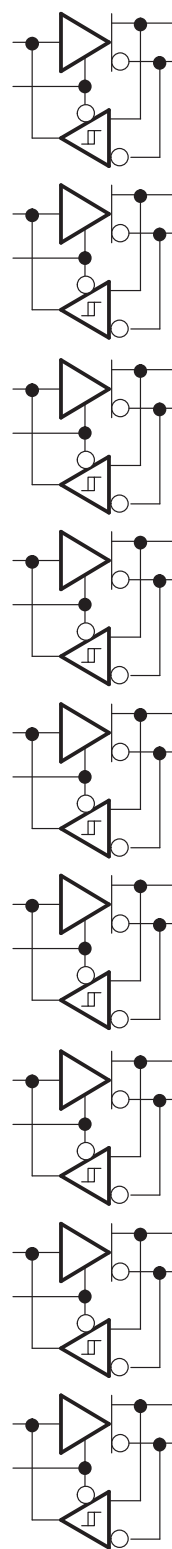


Figure 27. 01000

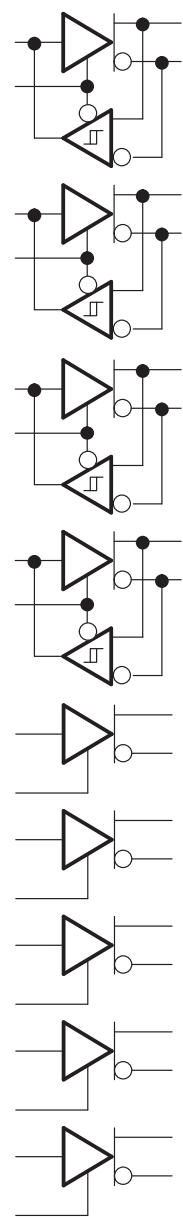


Figure 28. 01001

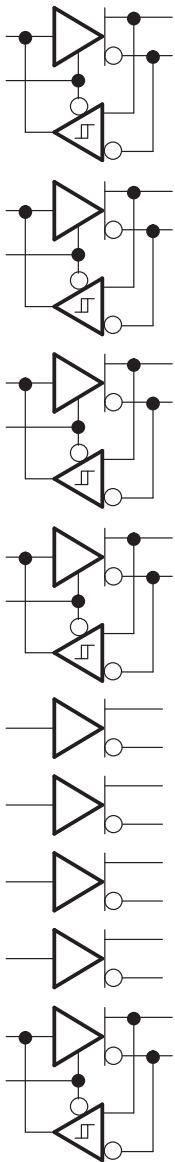


Figure 29. 01010

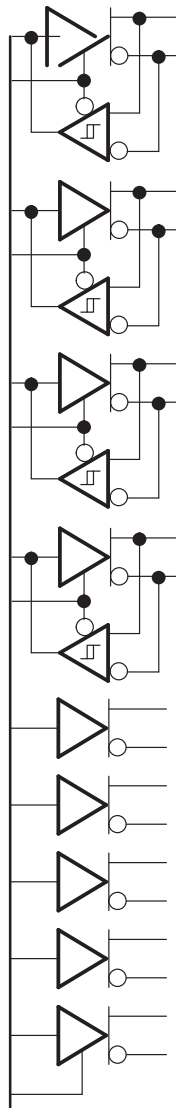


Figure 30. 01011

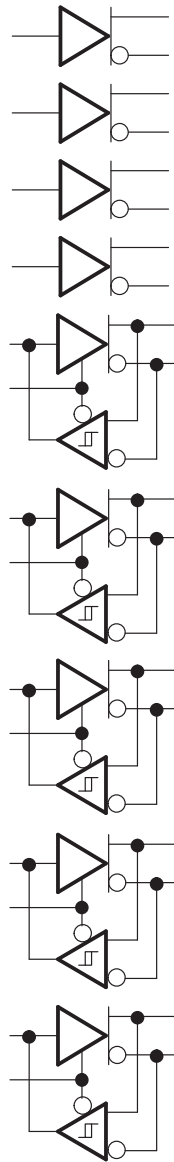


Figure 31. 01100

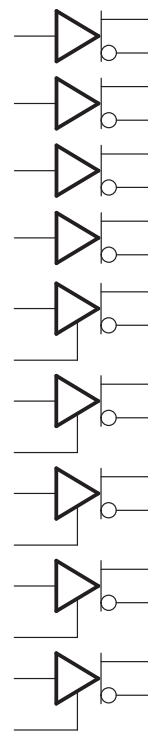


Figure 32. 01101

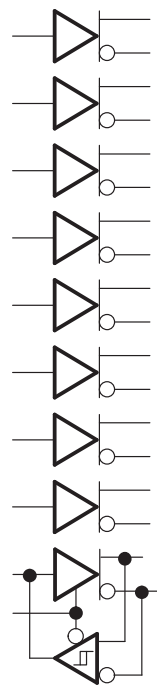


Figure 33. 01110

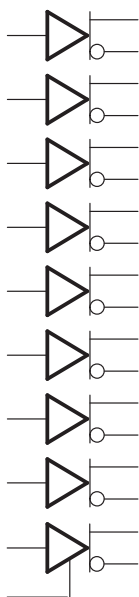


Figure 34. 01111



Figure 35. 10000 and 10001

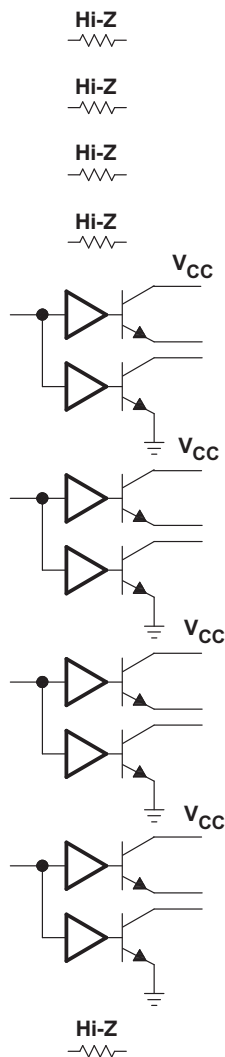


Figure 36. 10010 and 10011

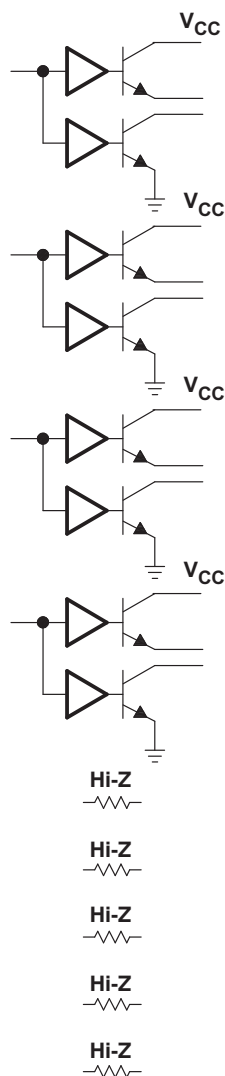


Figure 37. 10100 and 10101

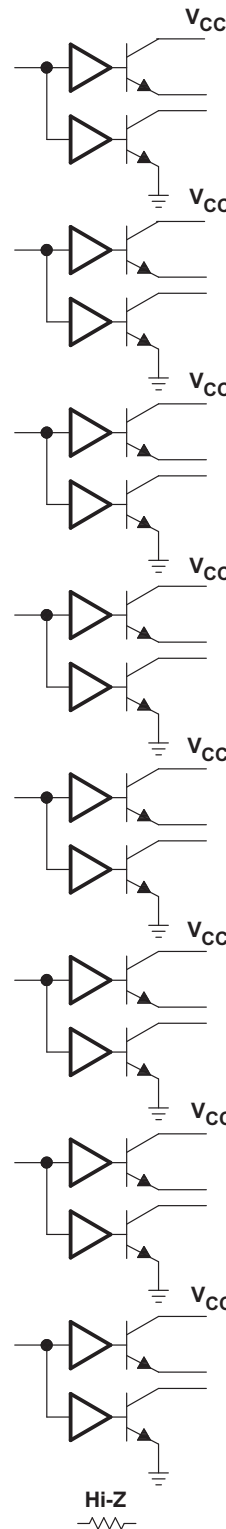


Figure 38. 10110 and 10111

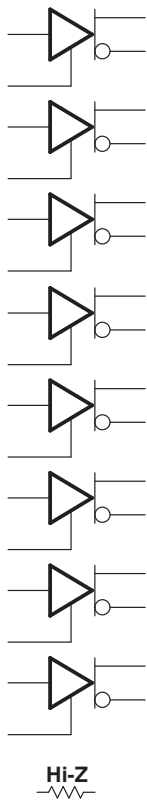


Figure 39. 11000 and 11001

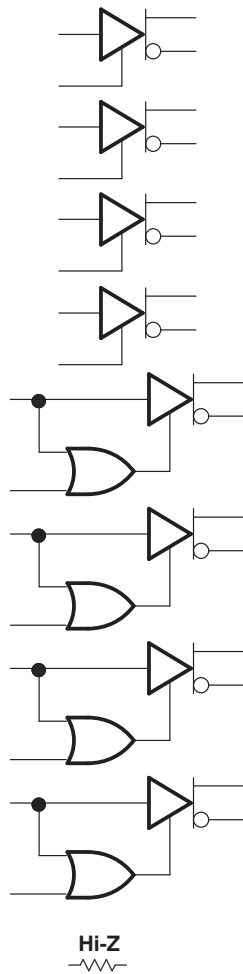


Figure 40. 11010 and 11011

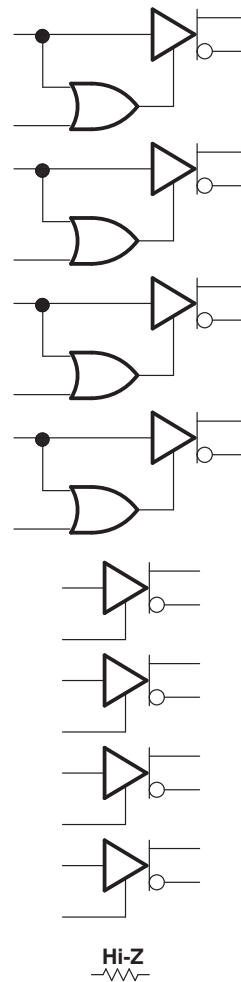


Figure 41. 11100 and 11101

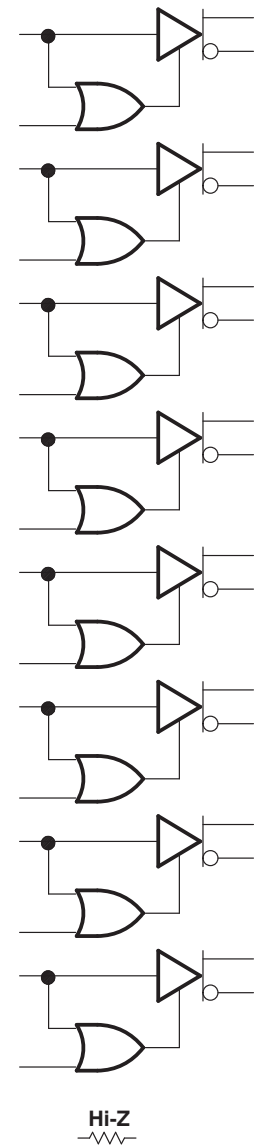


Figure 42. 11110 and 11111

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD09IDGGREP	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SN65HVD09EP	Samples
V62/12607-01XE	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SN65HVD09EP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN65HVD09-EP :

- Catalog: [SN65HVD09](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD09IDGGREP	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD09IDGGREP	TSSOP	DGG	56	2000	367.0	367.0	45.0

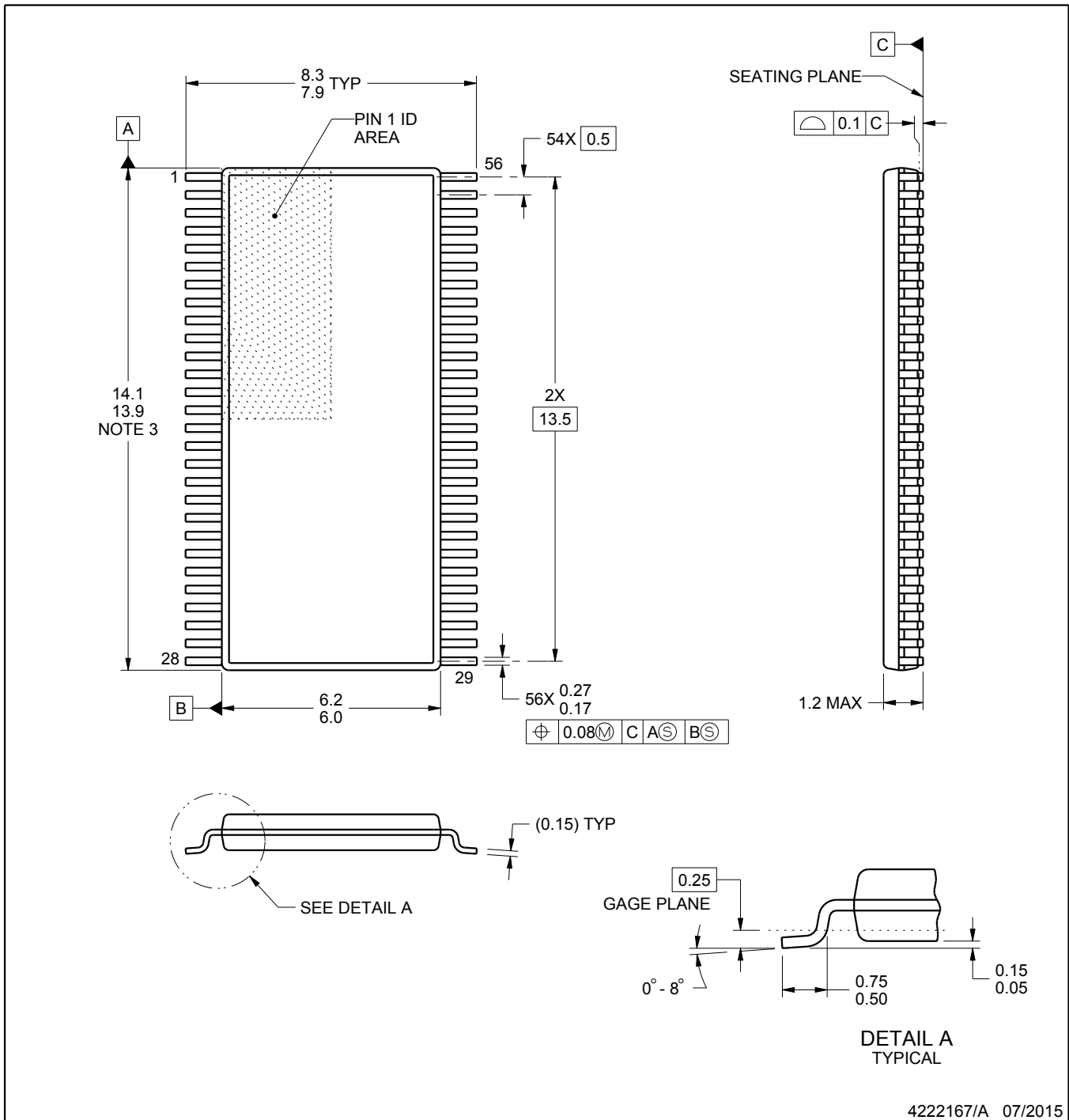
DGG0056A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4222167/A 07/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

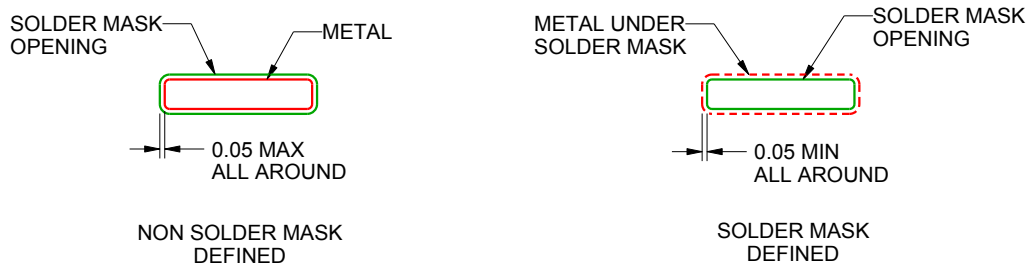
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com