

## 3.3-V CAN TRANSCEIVER

### FEATURES

- Bus-Pin Fault Protection Exceeds  $\pm 36$  V
- Bus-Pin ESD Protection Exceeds 16-kV HBM
- Compatible With ISO 11898
- Signaling Rates<sup>(1)</sup> up to 1 Mbps
- Extended  $-7$ -V to 12-V Common-Mode Range
- High-Input Impedance Allows for 120 Nodes
- LVTTTL I/Os Are 5-V Tolerant
- Adjustable Driver Transition Times for Improved Signal Quality
- Unpowered Node Does Not Disturb the Bus
- Low-Current Standby Mode . . . 200- $\mu$ A Typical
- Thermal Shutdown Protection
- Power-Up/Down Glitch-Free Bus Inputs and Outputs
  - High Input Impedance With Low  $V_{CC}$
  - Monolithic Output During Power Cycling
- Loopback for Diagnostic Functions Available
- DeviceNet Vendor ID #806

<sup>(1)</sup> The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

### SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Military ( $-55^{\circ}\text{C}/125^{\circ}\text{C}$ ) Temperature Range<sup>(1)</sup>
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

<sup>(1)</sup> Additional temperature ranges available - contact factory

### APPLICATIONS

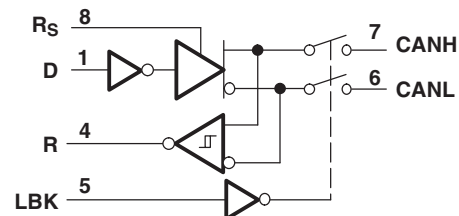
- CAN Data Bus
  - DeviceNet™ Data Buses
  - Smart Distributed Systems (SDS™)
- SAE J1939 Standard Data Bus Interface
- NMEA 2000 Standard Data Bus Interface
- ISO 11783 Standard Data Bus Interface

### DESCRIPTION

The SN65HVD233 is used in applications employing the controller area network (CAN) serial communication physical layer in accordance with the ISO 11898 standard. As a CAN transceiver, it provides transmit and receive capability between the differential CAN bus and a CAN controller, with signaling rates up to 1 Mbps.

Designed for operation in especially harsh environments, the device features cross-wire, overvoltage and loss of ground protection to  $\pm 36$  V, with overtemperature protection and common-mode transient protection of  $\pm 100$  V. This device operates over a  $-7$ -V to 12-V common-mode range with a maximum of 60 nodes on a bus.

FUNCTIONAL BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This device has limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## DESCRIPTION (CONTINUED)

If the common-mode range is restricted to the ISO-11898 Standard range of  $-2\text{ V}$  to  $7\text{ V}$ , up to 120 nodes may be connected on a bus. This transceiver interfaces the single-ended CAN controller with the differential CAN bus found in industrial, building automation, and automotive applications.

The  $R_S$  (pin 8) of the SN65HVD233 provides for three modes of operation: high-speed, slope control, or low-power standby mode. The high-speed mode of operation is selected by connecting  $R_S$  directly to ground, allowing the driver output transistors to switch on and off as fast as possible with no limitation on the rise and fall slope. The rise and fall slope can be adjusted by connecting a resistor to ground at  $R_S$ , since the slope is proportional to the pin's output current. Slope control is implemented with a resistor value of  $10\text{ k}\Omega$  to achieve a slew rate of  $\approx 15\text{ V}/\mu\text{s}$  and a value of  $100\text{ k}\Omega$  to achieve  $\approx 2.0\text{ V}/\mu\text{s}$  slew rate. For more information about slope control, refer to the application information section.

The SN65HVD233 enters a low-current standby mode during which the driver is switched off and the receiver remains active if a high logic level is applied to  $R_S$ . The local protocol controller reverses this low-current standby mode when it needs to transmit to the bus.

A logic high on the loopback LBK (pin 5) of the SN65HVD233 places the bus output and bus input in a high-impedance state. The remaining circuit remains active and available for driver to receiver loopback, self-diagnostic node functions without disturbing the bus.

### AVAILABLE OPTIONS

PART NUMBER	LOW POWER MODE	SLOPE CONTROL	DIAGNOSTIC LOOPBACK	AUTOBAUD LOOPBACK
SN65HVD233	200- $\mu\text{A}$ standby mode	Adjustable	Yes	No

### ORDERING INFORMATION<sup>(1)</sup>

$T_A$	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-55^\circ\text{C}$ to $125^\circ\text{C}$	SOIC – D	Reel of 2500	SN65HVD233MDREP	H233EP

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## POWER DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR <sup>(1)</sup> ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 85°C POWER RATING	T <sub>A</sub> = 125°C POWER RATING
D	Low-K	596.6 mW	5.7 mW/°C	255.7 mW	28.4 mW
D	High-K	1076.9 mW	10.3 mW/°C	461.5 mW	51.3 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

## ABSOLUTE MAXIMUM RATINGS<sup>(1) (2)</sup>

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V <sub>CC</sub>	Supply voltage range	–0.3 to 7	V
	Voltage range at any bus terminal (CANH or CANL)	–36 to 36	V
	Voltage input range, transient pulse, CANH and CANL, through 100 Ω (see Figure 7)	–100 to 100	V
V <sub>I</sub>	Input voltage range, (D, R, R <sub>S</sub> , LBK)	–0.5 to 7	V
I <sub>O</sub>	Receiver output current	–10 to 10	mA
	Electrostatic discharge	Human Body Model <sup>(3)</sup>	CANH, CANL and GND
		Human Body Model <sup>(3)</sup>	All pins
		Charged-Device Mode <sup>(4)</sup>	All pins
		16	kV
		3	kV
		1	kV
	Continuous total power dissipation	See Dissipation Rating Table	
T <sub>J</sub>	Operating junction temperature	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.

(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

## RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V <sub>CC</sub>	Supply voltage	3		3.6	
	Voltage at any bus terminal (separately or common mode)	–7		12	
V <sub>IH</sub>	High-level input voltage		D, LBK	5.5	V
V <sub>IL</sub>	Low-level input voltage		D, LBK	0.8	
V <sub>ID</sub>	Differential input voltage	–6		6	
	Resistance from R <sub>S</sub> to ground	0		100	kΩ
V <sub>I(RS)</sub>	Input Voltage at R <sub>S</sub> for standby	0.75 V <sub>CC</sub>		5.5	V
I <sub>OH</sub>	High-level output current	–50			mA
		–10			
I <sub>OL</sub>	Low-level output current			50	mA
				10	
T <sub>J</sub>	Operating junction temperature			150	°C
T <sub>A</sub>	Operating free-air temperature <sup>(1)</sup>	–55		125	°C

(1) Maximum free-air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

## DRIVER ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
V <sub>O(D)</sub>	Bus output voltage (Dominant)	CANH	D = 0 V, R <sub>S</sub> = 0 V, See <a href="#">Figure 1</a> and <a href="#">Figure 2</a>	2.45	V <sub>CC</sub>	V	
		CANL		0.5	1.25		
V <sub>O</sub>	Bus output voltage (Recessive)	CANH	D = 3 V, R <sub>S</sub> = 0 V, See <a href="#">Figure 1</a> and <a href="#">Figure 2</a>	2.3		V	
		CANL		2.3			
V <sub>OD(D)</sub>	Differential output voltage (Dominant)	D = 0 V, R <sub>S</sub> = 0 V, See <a href="#">Figure 1</a> and <a href="#">Figure 2</a>	1.5	2	3	V	
		D = 0 V, R <sub>S</sub> = 0 V, See <a href="#">Figure 2</a> and <a href="#">Figure 3</a>	1.2	2	3		
V <sub>OD</sub>	Differential output voltage (Recessive)	D = 3 V, R <sub>S</sub> = 0 V, See <a href="#">Figure 1</a> and <a href="#">Figure 2</a>	-120		12	mV	
		D = 3 V, R <sub>S</sub> = 0 V, No load	-0.5		0.05	V	
V <sub>OC(pp)</sub>	Peak-to-peak common-mode output voltage	See <a href="#">Figure 9</a>		1		V	
I <sub>IH</sub>	High-level input current	D, LBK	D = 2 V			μA	
I <sub>IL</sub>	Low-level input current	D, LBK	D = 0.8 V			μA	
I <sub>OS</sub>	Short-circuit output current	V <sub>CANH</sub> = -7 V, CANL Open, See <a href="#">Figure 12</a>	-250			mA	
		V <sub>CANH</sub> = 12 V, CANL Open, See <a href="#">Figure 12</a>			1		
		V <sub>CANL</sub> = -7 V, CANH Open, See <a href="#">Figure 12</a>	-1				
		V <sub>CANL</sub> = 12 V, CANH Open, See <a href="#">Figure 12</a>			250		
C <sub>O</sub>	Output capacitance	See receiver input capacitance					
I <sub>IRs(s)</sub>	R <sub>S</sub> input current for standby	R <sub>S</sub> = 0.75 V <sub>CC</sub>		-10		μA	
I <sub>CC</sub>	Supply current	Standby	R <sub>S</sub> = V <sub>CC</sub> , D = V <sub>CC</sub> , LBK = 0 V		200	600	μA
		Dominant	D = 0 V, No load, LBK = 0 V, R <sub>S</sub> = 0 V			6	mA
		Recessive	D = V <sub>CC</sub> , No load, LBK = 0 V, R <sub>S</sub> = 0 V			6	

(1) All typical values are at 25°C and with a 3.3 V supply.

## DRIVER SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output	R <sub>S</sub> = 0 V, See <a href="#">Figure 4</a>		35	95	ns
		R <sub>S</sub> with 10 kΩ to ground, See <a href="#">Figure 4</a>		70	125	
		R <sub>S</sub> with 100 kΩ to ground, See <a href="#">Figure 4</a>		500	870	
t <sub>PHL</sub>	Propagation delay time, high-to-low-level output	R <sub>S</sub> = 0 V, See <a href="#">Figure 4</a>		70	120	ns
		R <sub>S</sub> with 10 kΩ to ground, See <a href="#">Figure 4</a>		130	180	
		R <sub>S</sub> with 100 kΩ to ground, See <a href="#">Figure 4</a>		870	1200	
t <sub>sk(p)</sub>	Pulse skew ( t <sub>PHL</sub> – t <sub>PLH</sub>  )	R <sub>S</sub> = 0 V, See <a href="#">Figure 4</a>		35		ns
		R <sub>S</sub> with 10 kΩ to ground, See <a href="#">Figure 4</a>		60		
		R <sub>S</sub> with 100 kΩ to ground, See <a href="#">Figure 4</a>		370		
t <sub>r</sub>	Differential output signal rise time	R <sub>S</sub> = 0 V, See <a href="#">Figure 4</a>	20		70	ns
t <sub>f</sub>	Differential output signal fall time		20		70	
t <sub>r</sub>	Differential output signal rise time	R <sub>S</sub> with 10 kΩ to ground, See <a href="#">Figure 4</a>	30		135	ns
t <sub>f</sub>	Differential output signal fall time		30		135	
t <sub>r</sub>	Differential output signal rise time	R <sub>S</sub> with 100 kΩ to ground, See <a href="#">Figure 4</a>	300		1400	ns
t <sub>f</sub>	Differential output signal fall time		300		1400	
t <sub>en(s)</sub>	Enable time from standby to dominant	See <a href="#">Figure 8</a>		0.6	1.5	μs

(1) All typical values are at 25°C and with a 3.3 V supply. Timing parameters are characterized but not production tested.

## RECEIVER ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT		
$V_{IT+}$	Positive-going input threshold voltage <sup>(2)</sup>	LBK = 0 V, See <a href="#">Table 1</a>		750	900	mV		
$V_{IT-}$	Negative-going input threshold voltage <sup>(2)</sup>		500	650				
$V_{hys}$	Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )		100					
$V_{OH}$	High-level output voltage	$I_O = -4$ mA, See <a href="#">Figure 6</a>	2.4			V		
$V_{OL}$	Low-level output voltage	$I_O = 4$ mA, See <a href="#">Figure 6</a>			0.4			
$I_i$	Bus input current	CANH or CANL = 12 V	Other bus pin = 0 V, D = 3 V, LBK = 0 V, $R_S = 0$ V	150	500	$\mu$ A		
		CANH or CANL = 12 V, $V_{CC} = 0$ V		200	600			
		CANH or CANL = -7 V		-610	-150			
		CANH or CANL = -7 V, $V_{CC} = 0$ V		-450	-130			
$C_i$	Input capacitance (CANH or CANL)	Pin-to-ground, $V_i = 0.4 \sin(4E6\pi t) + 0.5V$ , D = 3 V, LBK = 0 V		40		pF		
$C_{iD}$	Differential input capacitance	Pin-to-pin, $V_i = 0.4 \sin(4E6\pi t) + 0.5V$ , D = 3 V, LBK = 0 V		20				
$R_{iD}$	Differential input resistance	D = 3 V, LBK = 0 V	40		100	k $\Omega$		
$R_{iN}$	Input resistance (CANH or CANL)		20		50			
$I_{CC}$	Supply current	Sleep	D = $V_{CC}$ , $R_S = 0$ V or $V_{CC}$		0.05	2	$\mu$ A	
		Standby	$R_S = V_{CC}$ , D = $V_{CC}$ , LBK = 0 V		200	600		
		Dominant	D = 0 V, No load, $R_S = 0$ V, LBK = 0 V				6	mA
		Recessive	D = $V_{CC}$ , No load, $R_S = 0$ V, LBK = 0 V				6	

(1) All typical values are at 25°C and with a 3.3 V supply.

(2) Characterized but not production tested.

## RECEIVER SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level output	See <a href="#">Figure 6</a>		35	60	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output			35	60	
$t_{sk(p)}$	Pulse skew ( $ t_{PHL} - t_{PLH} $ )			7		
$t_r$	Output signal rise time			2	6.5	
$t_f$	Output signal fall time			2	6.5	

(1) All typical values are at 25°C and with a 3.3 V supply. Timing parameters are characterized but not production tested.

## DEVICE SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{(LBK)}$	Loopback delay, driver input to receiver output	HVD233 See <a href="#">Figure 11</a>		7.5	13	ns
$t_{(loop1)}$	Total loop delay, driver input to receiver output, recessive to dominant	$R_S = 0\text{ V}$ , See <a href="#">Figure 10</a>		70	135	ns
		$R_S$ with 10 k $\Omega$ to ground, See <a href="#">Figure 10</a>		105	190	
		$R_S$ with 100 k $\Omega$ to ground, See <a href="#">Figure 10</a>		535	1000	
$t_{(loop2)}$	Total loop delay, driver input to receiver output, dominant to recessive	$R_S = 0\text{ V}$ , See <a href="#">Figure 10</a>		70	135	ns
		$R_S$ with 10 k $\Omega$ to ground, See <a href="#">Figure 10</a>		105	190	
		$R_S$ with 100 k $\Omega$ to ground, See <a href="#">Figure 10</a>		535	1100	

(1) All typical values are at 25°C and with a 3.3 V supply. Timing parameters are characterized but not production tested.

PARAMETER MEASUREMENT INFORMATION

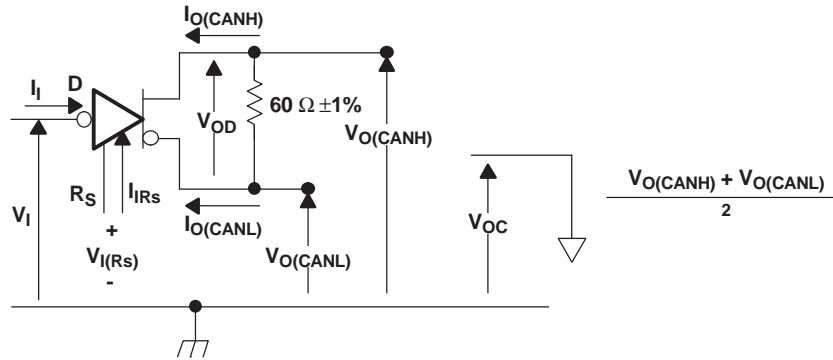


Figure 1. Driver Voltage, Current, and Test Definition

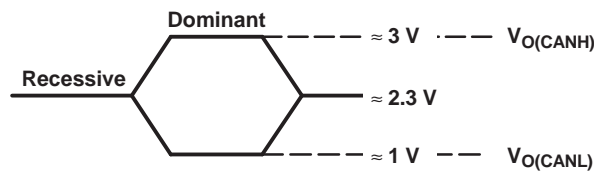


Figure 2. Bus Logic State Voltage Definitions

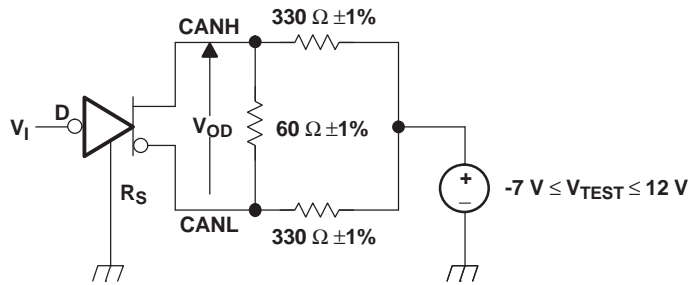
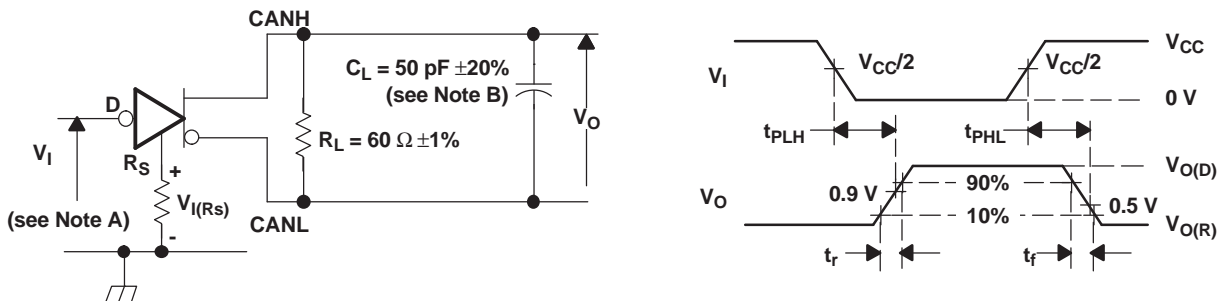


Figure 3. Driver V<sub>OD</sub>



- A. The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) ≤ 125 kHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_0 = 50 \Omega$ .
- B.  $C_L$  includes fixture and instrumentation capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION (continued)

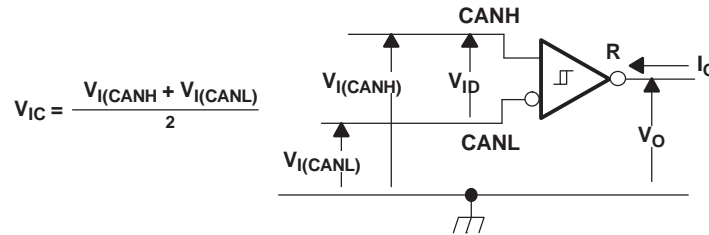
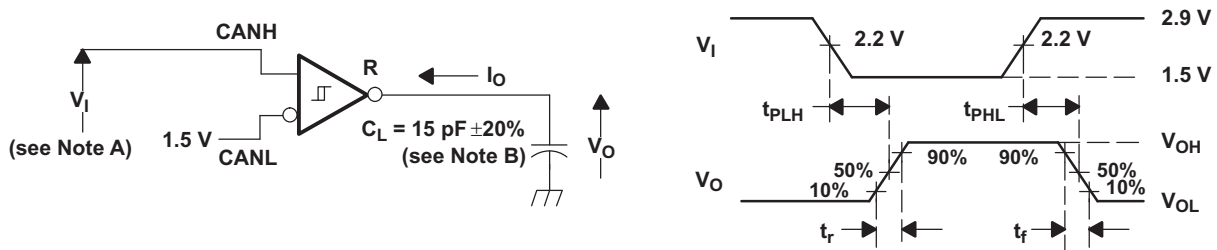


Figure 5. Receiver Voltage and Current Definitions

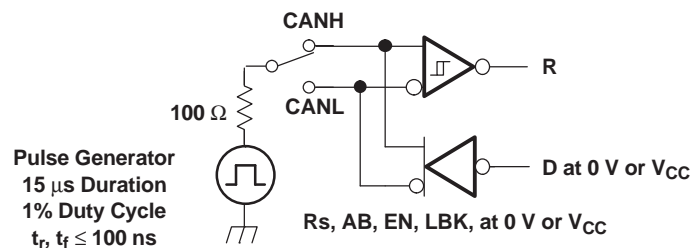


- A. The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) ≤ 125 kHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .
- B.  $C_L$  includes fixture and instrumentation capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms

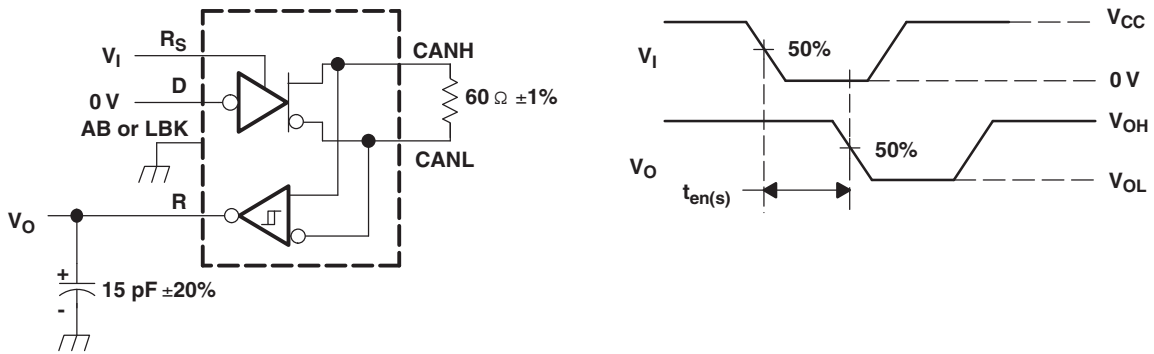
Table 1. Differential Input Voltage Threshold Test

INPUT		OUTPUT		MEASURED
$V_{CANH}$	$V_{CANL}$	R		$ V_{ID} $
-6.1 V	-7 V	L	$V_{OL}$	900 mV
12 V	11.1 V	L		900 mV
-1 V	-7 V	L		6 V
12 V	6 V	L		6 V
-6.5 V	-7 V	H	$V_{OH}$	500 mV
12 V	11.5 V	H		500 mV
-7 V	-1 V	H		6 V
6 V	12 V	H		6 V
Open	Open	H		X



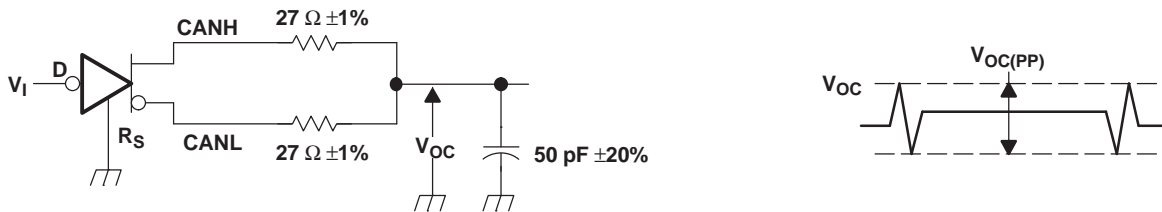
NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 7. Test Circuit, Transient Over Voltage Test



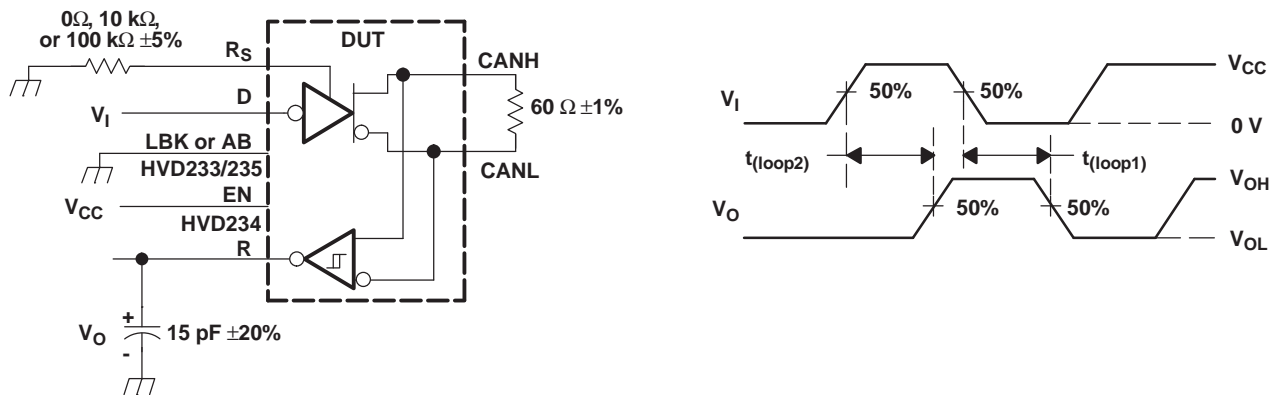
NOTE: All  $V_I$  input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 6$  ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 8.  $t_{en(s)}$  Test Circuit and Voltage Waveforms



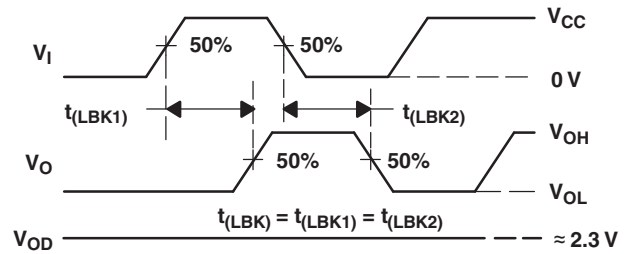
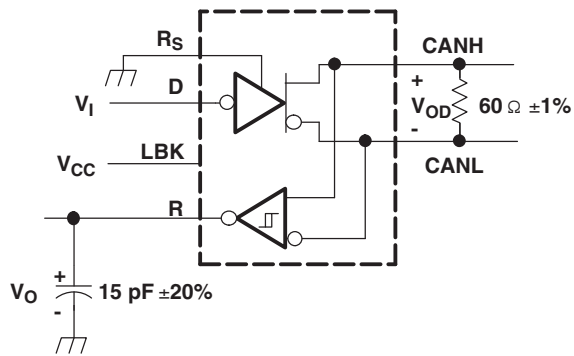
NOTE: All  $V_I$  input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 6$  ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 9.  $V_{OC(pp)}$  Test Circuit and Voltage Waveforms



NOTE: All  $V_I$  input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 6$  ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 10.  $t_{(loop)}$  Test Circuit and Voltage Waveforms



NOTE: All  $V_I$  input pulses are supplied by a generator having the following characteristics:  
 $t_r$  or  $t_f \leq 6$  ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 11.  $t_{(LBK)}$  Test Circuit and Voltage Waveforms

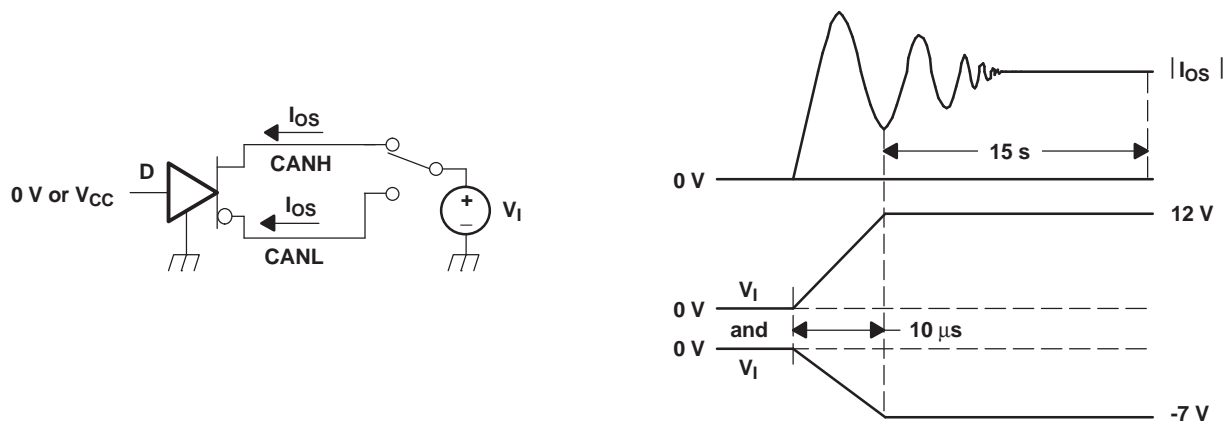
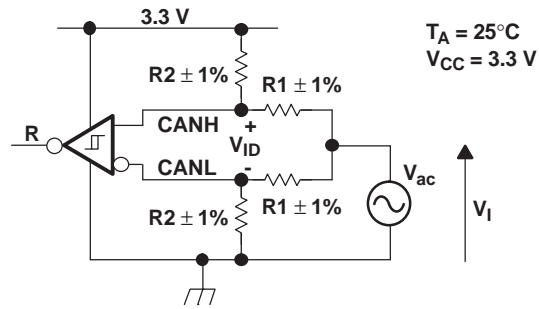


Figure 12.  $I_{OS}$  Test Circuit and Waveforms



The R Output State Does Not Change During Application of the Input Waveform.

$V_{ID}$	R1	R2
500 mV	50 $\Omega$	280 $\Omega$
900 mV	50 $\Omega$	130 $\Omega$

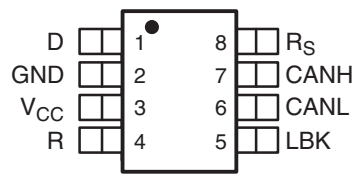


NOTE: All input pulses are supplied by a generator with  $f \leq 1.5\text{ MHz}$ .

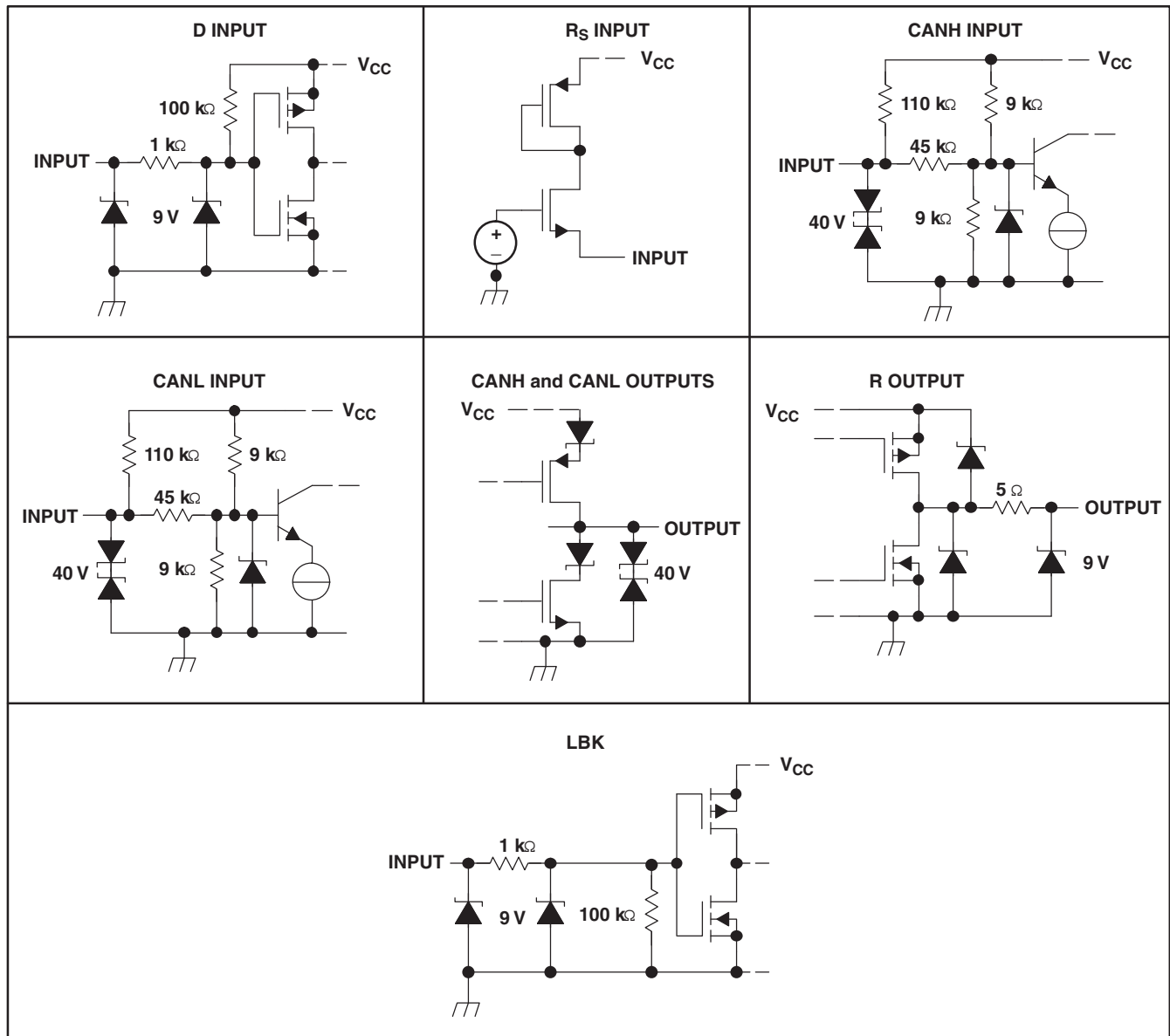
**Figure 13. Common-Mode Voltage Rejection**

DEVICE INFORMATION

SN65HVD233D  
(TOP VIEW)



EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



**Table 2. Thermal Characteristics**

PARAMETERS		TEST CONDITIONS	VALUE	UNIT
$\theta_{JA}$	Junction-to-ambient thermal resistance <sup>(1)</sup>	Low-K <sup>(2)</sup> board, no air flow	185	°C/W
		High-K <sup>(3)</sup> board, no air flow	101	
$\theta_{JB}$	Junction-to-board thermal resistance	High-K <sup>(3)</sup> board, no air flow	82.8	°C/W
$\theta_{JC}$	Junction-to-case thermal resistance		26.5	°C/W
$P_{(AVG)}$	Average power dissipation	$R_L = 60 \Omega$ , $R_S$ at 0 V, input to D a 1-MHz 50% duty cycle square wave $V_{CC}$ at 3.3 V, $T_A = 25^\circ\text{C}$	36.4	mW
$T_{(SD)}$	Thermal shutdown junction temperature		170	°C

- (1) See TI literature number [SZZA003](#) for an explanation of this parameter.  
(2) JESD51-3 low effective thermal conductivity test board for leaded surface mount packages.  
(3) JESD51-7 high effective thermal conductivity test board for leaded surface mount packages.

**FUNCTION TABLES**

DRIVER <sup>(1)</sup>					
INPUTS			OUTPUTS		
D	LBK/AB	$R_s$	CANH	CANL	BUS STATE
X	X	$> 0.75 V_{CC}$	Z	Z	Recessive
L	L or open	$\leq 0.33 V_{CC}$	H	L	Dominant
H or open	X		Z	Z	Recessive
X	H	$\leq 0.33 V_{CC}$	Z	Z	Recessive

- (1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

RECEIVER <sup>(1)</sup>				
INPUTS				OUTPUT
BUS STATE	$V_{ID} = V_{(CANH)} - V_{(CANL)}$	LBK	D	R
Dominant	$V_{ID} \geq 0.9 \text{ V}$	L or open	X	L
Recessive	$V_{ID} \leq 0.5 \text{ V}$ or open	L or open	H or open	H
?	$0.5 \text{ V} < V_{ID} < 0.9 \text{ V}$	L or open	H or open	?
X	X	H	L	L
X	X		H	H

- (1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

TYPICAL CHARACTERISTICS

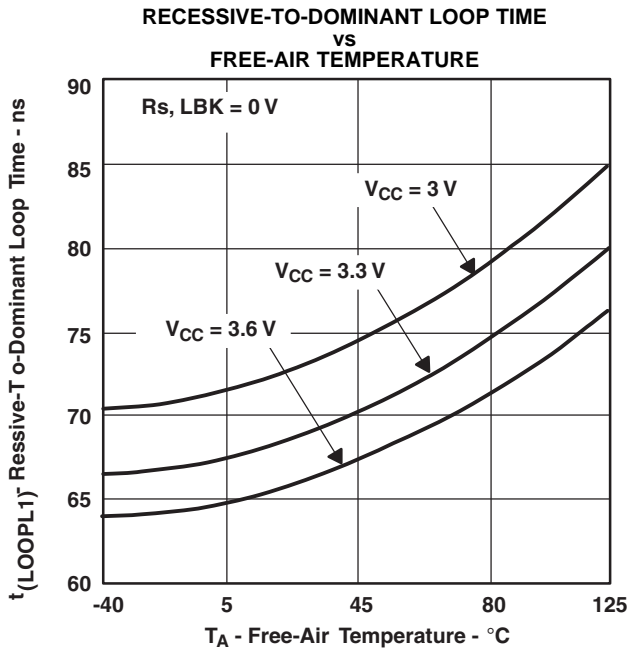


Figure 14.

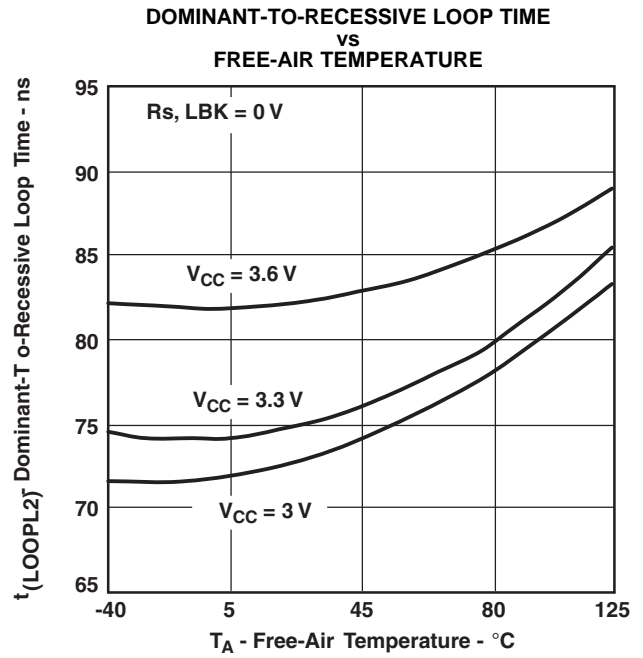


Figure 15.

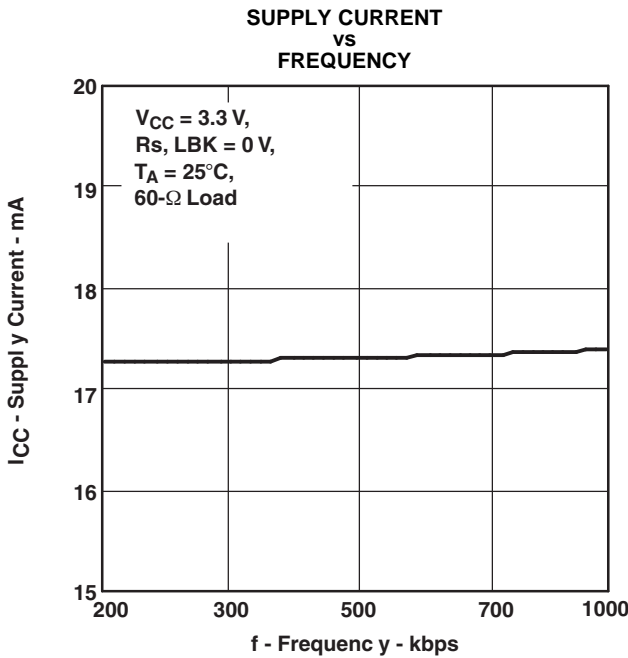


Figure 16.

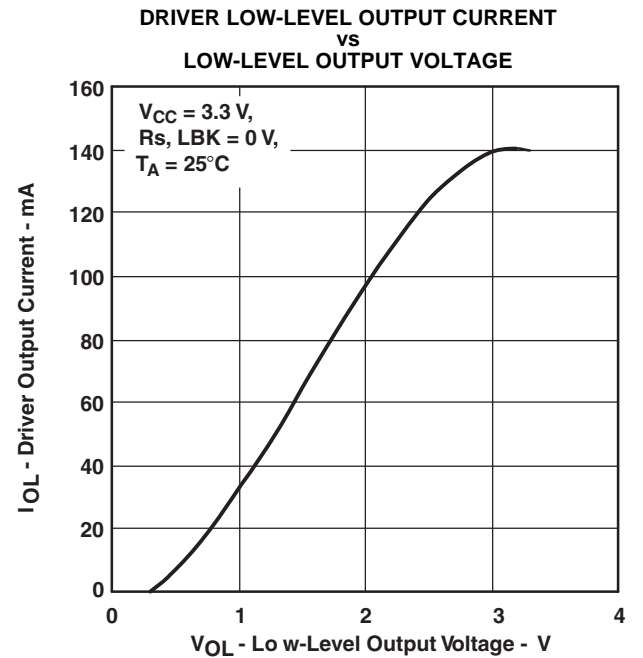


Figure 17.

TYPICAL CHARACTERISTICS (continued)

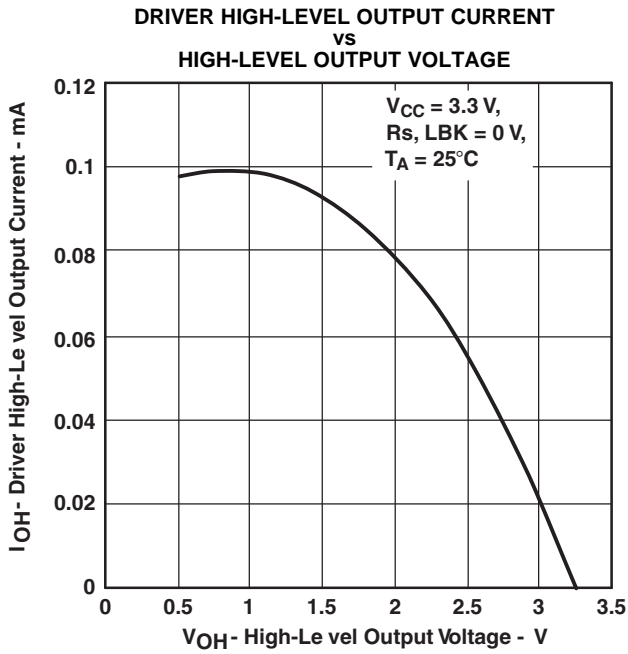


Figure 18.

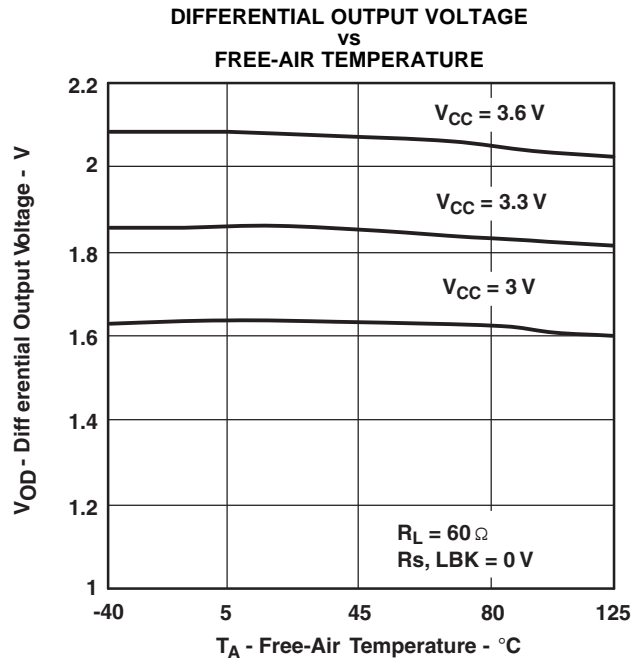


Figure 19.

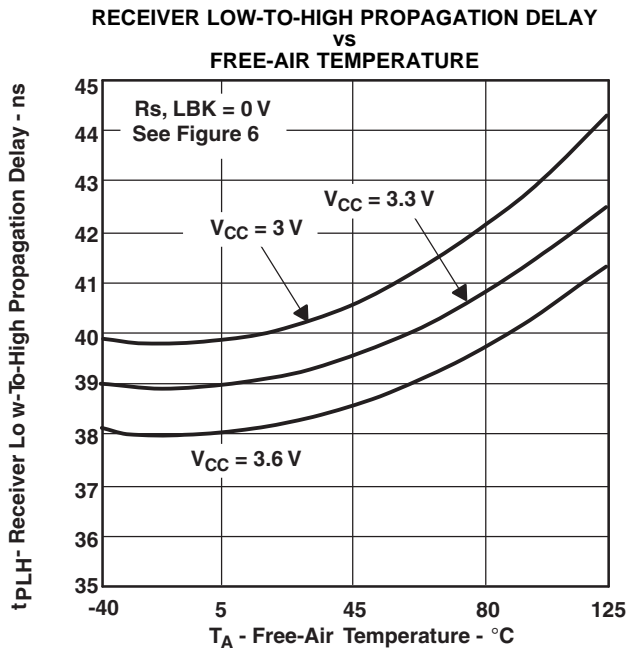


Figure 20.

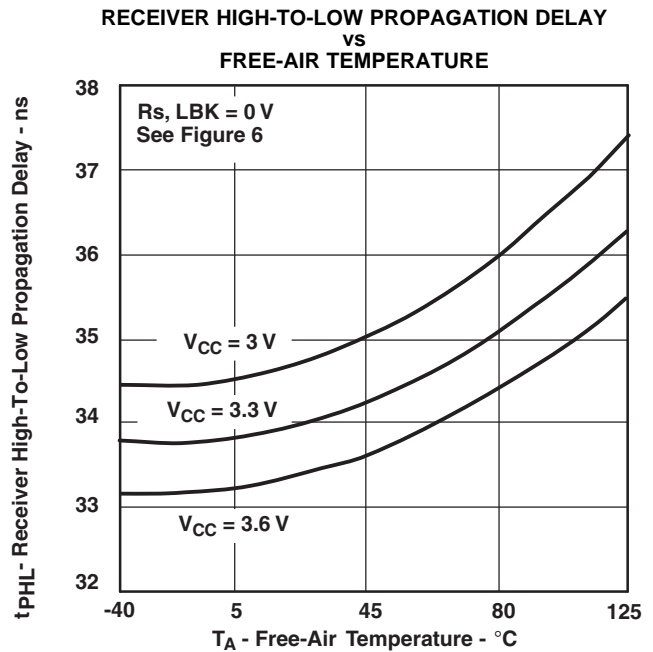


Figure 21.



TYPICAL CHARACTERISTICS (continued)

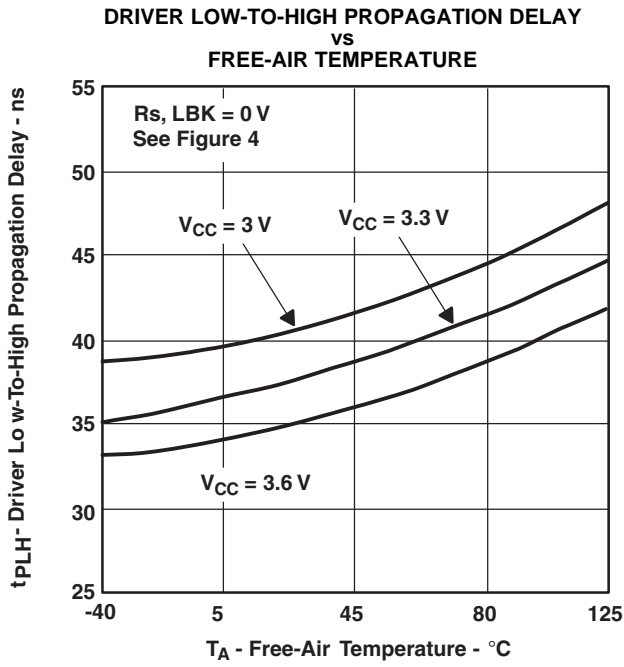


Figure 22.

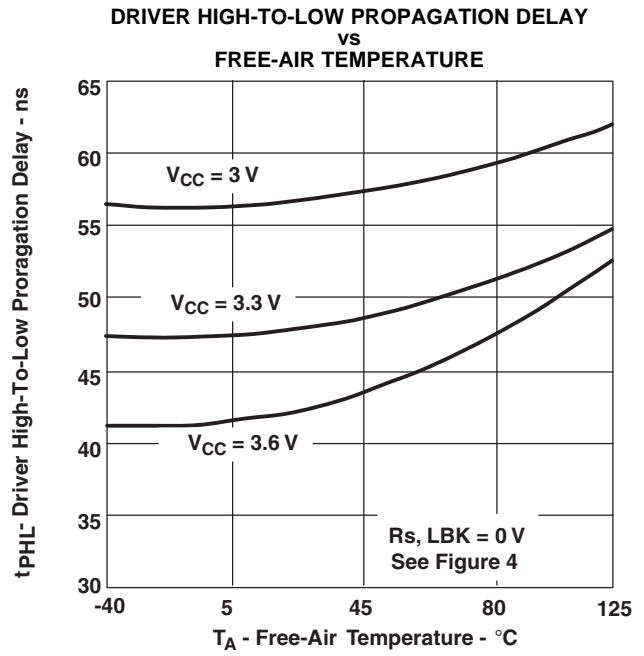


Figure 23.

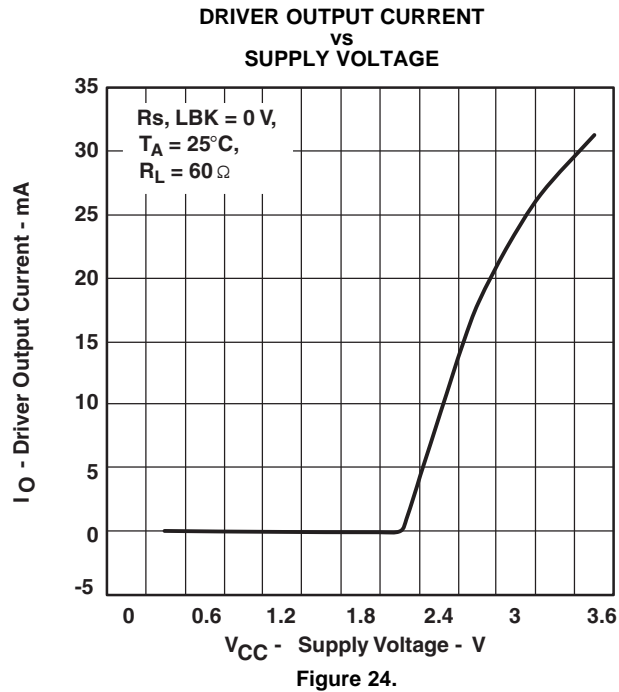


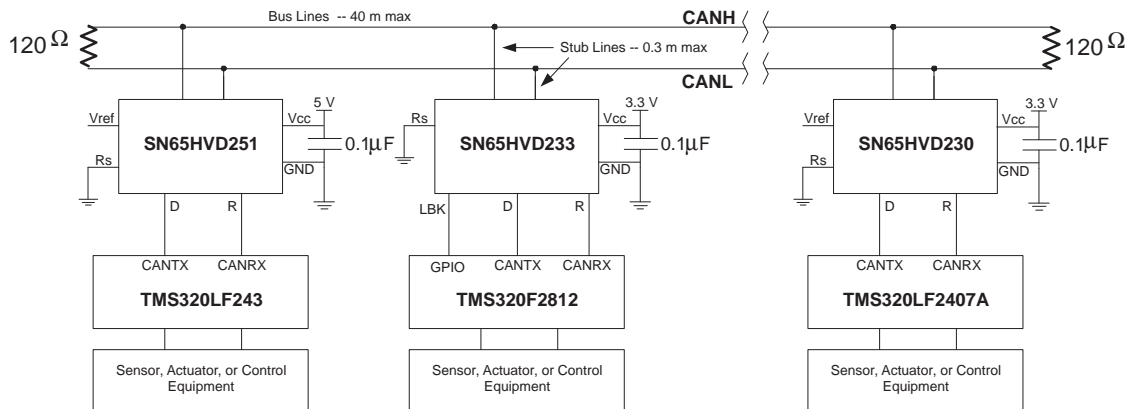
Figure 24.

## APPLICATION INFORMATION

### DIAGNOSTIC LOOPBACK (SN65HVD233)

The loopback function of the SN65HVD233 is enabled with a high-level input to LBK. This forces the driver into a recessive state and redirects the data (D) input at pin 1 to the received-data output (R) at pin 4. This allows the host controller to input and read back a bit sequence to perform diagnostic routines without disturbing the CAN bus. A typical CAN bus application is displayed in [Figure 25](#).

If the LBK pin is not used it may be tied to ground (GND). However, it is pulled low internally (defaults to a low-level input) and may be left open if not in use.



**Figure 25. Typical HVD233 Application**

## ISO 11898 COMPLIANCE OF SN65HVD230 FAMILY OF 3.3-V CAN TRANSCEIVERS

### Introduction

Many users value the low power consumption of operating their CAN transceivers from a 3.3 V supply. However, some are concerned about the interoperability with 5-V supplied transceivers on the same bus. This report analyzes this situation to address those concerns.

### Differential Signal

CAN is a differential bus where complementary signals are sent over two wires and the voltage difference between the two wires defines the logical state of the bus. The differential CAN receiver monitors this voltage difference and outputs the bus state with a single-ended output signal.

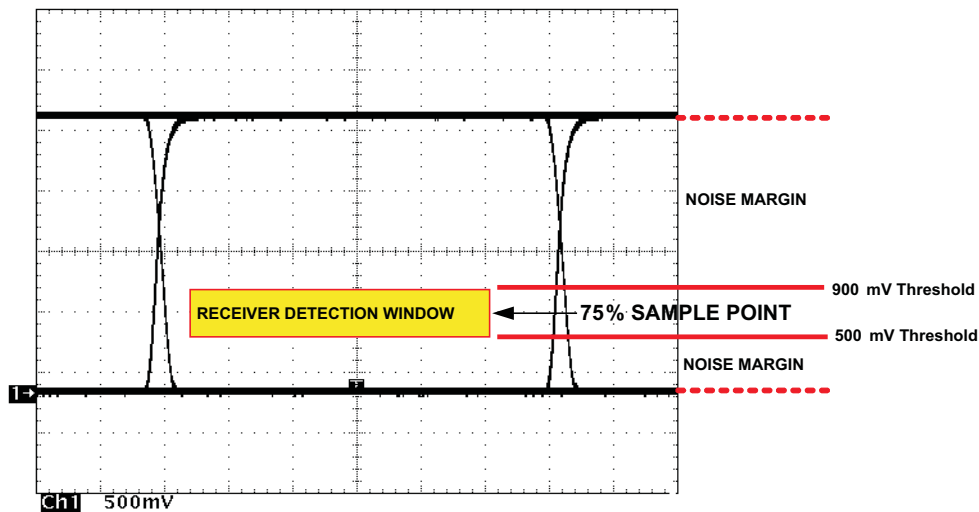


Figure 26. Typical SN65HVD230 Differential Output Voltage Waveform

The CAN driver creates the difference voltage between CANH and CANL in the dominant state. The dominant differential output of the SN65HVD230 is greater than 1.5 V and less than 3 V across a 60-ohm load. The minimum required by ISO 11898 is 1.5 V and maximum is 3 V. These are the same limiting values for 5-V supplied CAN transceivers. The bus termination resistors drive the recessive bus state and not the CAN driver.

A CAN receiver is required to output a recessive state with less than 500 mV and a dominant state with more than 900 mV difference voltage on its bus inputs. The CAN receiver must do this with common-mode input voltages from -2 V to 7 V. The SN65HVD230 family receivers meet these same input specifications as 5-V supplied receivers.

### Common-Mode Signal

A common-mode signal is an average voltage of the two signal wires that the differential receiver rejects. The common-mode signal comes from the CAN driver, ground noise, and coupled bus noise. Obviously, the supply voltage of the CAN transceiver has nothing to do with noise. The SN65HVD230 family driver lowers the common-mode output in a dominant bit by a couple hundred millivolts from that of most 5-V drivers. While this does not fully comply with ISO 11898, this small variation in the driver common-mode output is rejected by differential receivers and does not effect data, signal noise margins or error rates.

### Interoperability of 3.3-V CAN in 5-V CAN Systems

The 3.3-V supplied SN65HVD23x family of CAN transceivers are electrically interchangeable with 5-V CAN transceivers. The differential output is the same. The recessive common-mode output is the same. The dominant common-mode output voltage is a couple hundred millivolts lower than 5-V supplied drivers, while the receivers exhibit identical specifications as 5-V devices.

Electrical interoperability does not assure interchangeability however. Most implementers of CAN buses recognize that ISO 11898 does not sufficiently specify the electrical layer and that strict standard compliance alone does not ensure interchangeability. This comes only with thorough equipment testing.

### BUS CABLE

The ISO-11898 Standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m with a maximum of 30 nodes. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A large number of nodes requires a transceiver with high input impedance such as the SN65HVD233.

The standard specifies the interconnect to be a single twisted-pair cable (shielded or unshielded) with 120-Ω characteristic impedance ( $Z_0$ ). Resistors equal to the characteristic impedance of the line terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections.

### SLOPE CONTROL

The rise and fall slope of the SN65HVD233 driver output can be adjusted by connecting a resistor from  $R_s$  (pin 8) to ground (GND), or to a low-level input voltage as shown in Figure 27.

The slope of the driver output signal is proportional to the pin's output current. This slope control is implemented with an external resistor value of 10 kΩ to achieve a  $\approx 15$  V/μs slew rate, and up to 100 kΩ to achieve a  $\approx 2.0$  V/μs slew rate as displayed in Figure 28. Typical driver output waveforms with slope control are displayed in Figure 29.

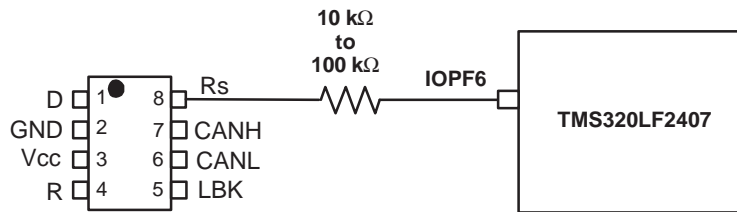


Figure 27. Slope Control/Standby Connection to a DSP

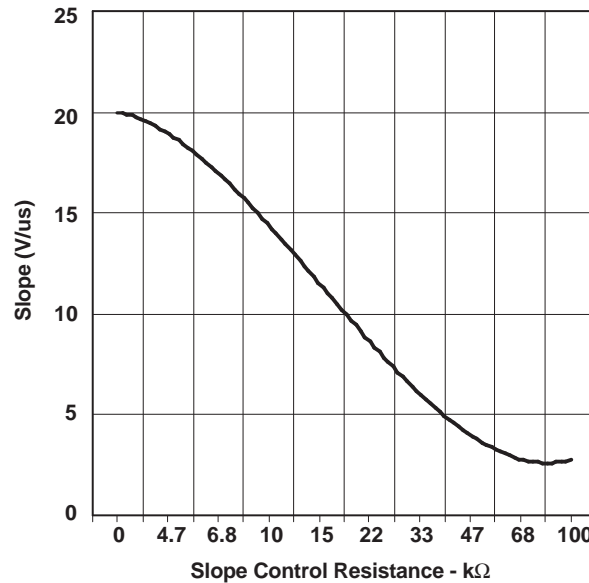


Figure 28. SN65HVD233 Driver Output Signal Slope vs Slope Control Resistance Value

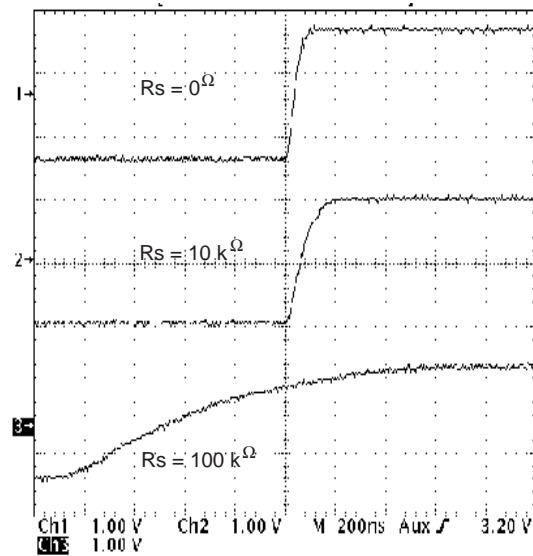


Figure 29. Typical SN65HVD233 250-kbps Output Pulse Waveforms With Slope Control

## STANDBY

If a high-level input ( $> 0.75 V_{CC}$ ) is applied to  $R_s$  (pin 8), the circuit enters a low-current, *listen only* standby mode during which the driver is switched off and the receiver remains active. The local controller can reverse this low-power standby mode when the rising edge of a dominant state (bus differential voltage  $>900$  mV typical) occurs on the bus.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD233MDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	H233EP	<a href="#">Samples</a>
V62/09611-01XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	H233EP	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN65HVD233-EP :**

- Catalog: [SN65HVD233](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD233MDREP	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD233MDREP	SOIC	D	8	2500	340.5	338.1	20.6



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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