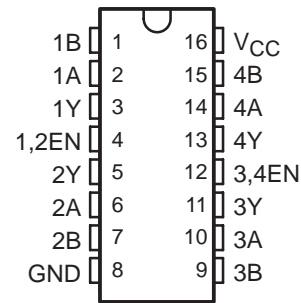


# SN65LBC175, SN75LBC175 QUADRUPLE LOW-POWER DIFFERENTIAL LINE RECEIVERS

SLLS171G – OCTOBER 1993 – REVISED MARCH2009

- Meets or Exceeds the EIA Standards RS-422-A, RS-423-A, RS-485, and CCITT Recommendation V.11
- Designed to Operate With Pulse Durations as Short as 20 ns
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Input Sensitivity . . .  $\pm 200$  mV
- Low-Power Consumption . . . 20 mA Max
- Open-Circuit Fail-Safe Design
- Common-Mode Input Voltage Range of  $-7$  V to 12 V
- Pin Compatible With SN75175 and LTC489

D, DW, OR N PACKAGE  
(TOP VIEW)



## description

The SN65LBC175 and SN75LBC175 are monolithic, quadruple, differential line receivers with 3-state outputs designed to meet the requirements of the EIA standards RS-422-A, RS-423-A, RS-485, and CCITT Recommendation V.11. The devices are optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. The receivers are enabled in pairs, with an active-high enable input. Each differential receiver input features high impedance, hysteresis for increased noise immunity, and sensitivity of  $\pm 200$  mV over a common-mode input voltage range of 12 V to  $-7$  V. The fail-safe design ensures that when the inputs are open-circuited, the outputs are always high. Both devices are designed using the TI proprietary LinBiCMOS™ technology allowing low power consumption, high switching speeds, and robustness.

These devices offer optimum performance when used with the SN75LBC172 or SN75LBC174 quadruple line drivers. The SN65LBC175 is available in the 16-pin DIP (N), small-outline package (D), and the wide small-outline package (DW). The SN75LBC175 is available in the 16-pin DIP (N) and the small-outline package (D).

The SN65LBC175 is characterized over the industrial temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . The SN75LBC175 is characterized for operation over the commercial temperature range of  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

AVAILABLE OPTIONS

PACKAGE	TEMPERATURE RANGE	
	$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$
SOIC	SN75LBC175D	SN65LBC175D
Wide SOIC	—	SN65LBC175DW
PDIP	SN75LBC175N	SN65LBC175N



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



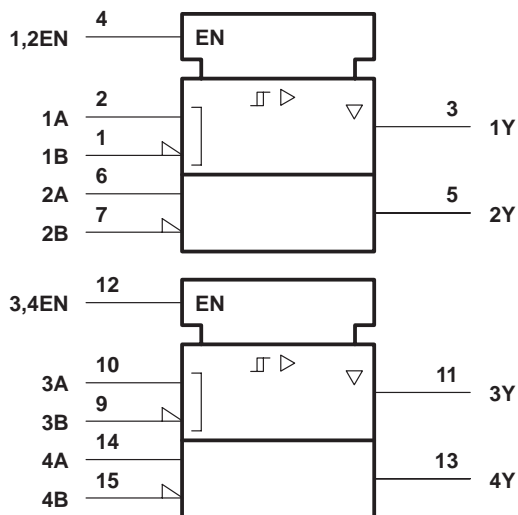
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# SN65LBC175, SN75LBC175 QUADRUPLE LOW-POWER DIFFERENTIAL LINE RECEIVERS

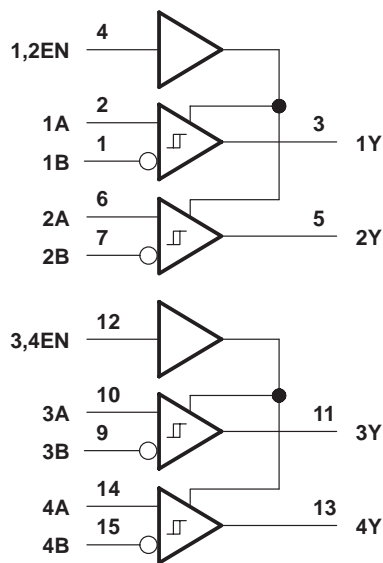
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)

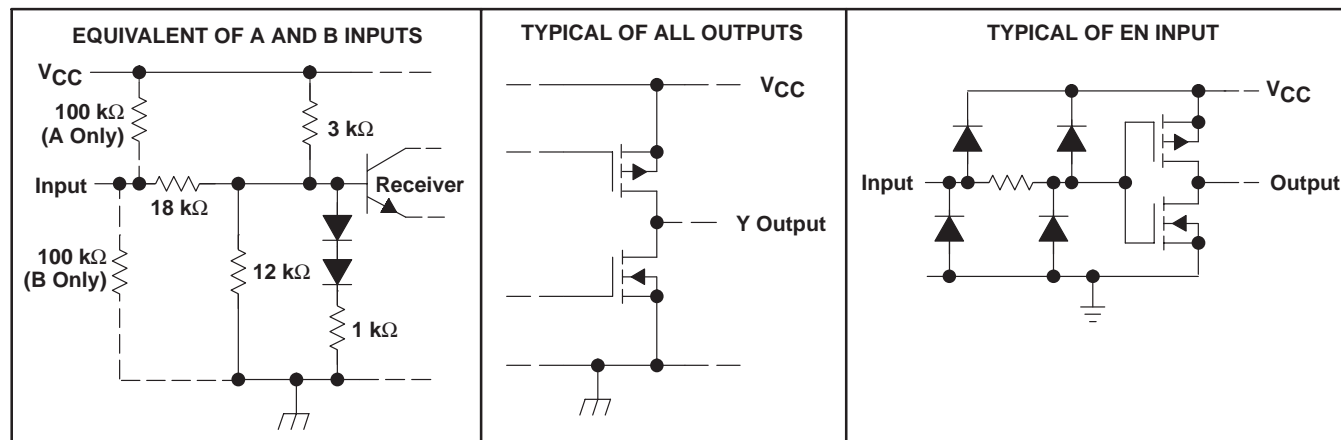


FUNCTION TABLE  
(each receiver)

DIFFERENTIAL INPUTS A-B	ENABLE	OUTPUT Y
$V_{ID} \geq 0.2 \text{ V}$	H	H
$-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$	H	?
$V_{ID} \leq -0.2 \text{ V}$	H	L
X	L	Z
Open circuit	H	H

H = high level, L = low level, X = irrelevant,  
Z = high impedance (off), ? = indeterminate

## schematics of inputs and outputs



# SN65LBC175, SN75LBC175 QUADRUPLE LOW-POWER DIFFERENTIAL LINE RECEIVERS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1)	–0.3 V to 7 V
Input voltage, $V_I$ (A or B inputs)	±25 V
Differential input voltage, $V_{ID}$ (see Note 2)	±25 V
Voltage range at Y, 1/2EN, 3/4EN	–0.3 V to $V_{CC} + 0.5$ V
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$ : SN65LBC175	–40°C to 85°C
SN75LBC175	0°C to 70°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Electrostatic Discharge (ESD): Human Body Model (HBM)	1 kV
Machine Model (MM)	200 V
Charged Device Model (CDM)	1.5 kV

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to GND.  
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D	1100 mW	8.7 mW/°C	709 mW	578 mW
DW	1200 mW	9.6 mW/°C	770 mW	625 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

## recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$		4.75	5	5.25	V
Common-mode input voltage, $V_{IC}$		–7		12	V
Differential input voltage, $V_{ID}$				±6	V
High-level input voltage, $V_{IH}$	EN inputs	2			V
Low-level input voltage, $V_{IL}$				0.8	V
High-level output current, $I_{OH}$				–8	mA
Low-level output current, $I_{OL}$				8	mA
Operating free-air temperature, $T_A$	SN65LBC175	–40		85	°C
	SN75LBC175	0		70	



# SN65LBC175, SN75LBC175 QUADRUPLE LOW-POWER DIFFERENTIAL LINE RECEIVERS

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
$V_{IT+}$	Positive-going input threshold voltage	$I_O = -8$ mA			0.2	V	
$V_{IT-}$	Negative-going input threshold voltage	$I_O = 8$ mA	-0.2			V	
$V_{hys}$	Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )			45		mV	
$V_{IK}$	Enable input clamp voltage	$I_I = -18$ mA		-0.9	-1.5	V	
$V_{OH}$	High-level output voltage	$V_{ID} = 200$ mV, $I_{OH} = -8$ mA	3.5	4.5		V	
$V_{OL}$	Low-level output voltage	$V_{ID} = -200$ mV, $I_{OL} = 8$ mA		0.3	0.5	V	
$I_{OZ}$	High-impedance-state output current	$V_O = 0$ V to $V_{CC}$			$\pm 20$	$\mu$ A	
$I_I$	Bus input current	A or B inputs	$V_{IH} = 12$ V, $V_{CC} = 5$ V, Other inputs at 0 V		0.7	1	mA
			$V_{IH} = 12$ V, $V_{CC} = 0$ V, Other inputs at 0 V		0.8	1	
			$V_{IH} = -7$ V, $V_{CC} = 5$ V, Other inputs at 0 V		-0.5	-0.8	
			$V_{IH} = -7$ V, $V_{CC} = 0$ V, Other inputs at 0 V		-0.4	-0.8	
$I_{IH}$	High-level enable input current	$V_{IH} = 5$ V			$\pm 20$	$\mu$ A	
$I_{IL}$	Low-level enable input current	$V_{IL} = 0$ V			-20	$\mu$ A	
$I_{OS}$	Short-circuit output current	$V_O = 0$		-80	-120	mA	
$I_{CC}$	Supply current	Outputs enabled, $I_O = 0$ , $V_{ID} = 5$ V		11	20	mA	
		Outputs disabled		0.9	1.4		

† All typical values are at  $V_{CC} = 5$  V and  $T_A = 25^\circ\text{C}$ .

switching characteristics,  $V_{CC} = 5$  V,  $C_L = 15$  pF,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{PHL}$	Propagation delay time, high- to low-level output	$V_{ID} = -1.5$ V to 1.5 V,	11	22	30	ns
$t_{PLH}$	Propagation delay time, low- to high-level output	See Figure 1	11	22	30	ns
$t_{PZH}$	Output enable time to high level	See Figure 2		17	30	ns
$t_{PZL}$	Output enable time to low level	See Figure 3		18	30	ns
$t_{PHZ}$	Output disable time from high level	See Figure 2		30	40	ns
$t_{PLZ}$	Output disable time from low level	See Figure 3		23	30	ns
$t_{sk(p)}$	Pulse skew ( $ t_{PHL} - t_{PLH} $ )	See Figure 2		4	6	ns
$t_t$	Transition time	See Figure 1		3	10	ns

# SN65LBC175, SN75LBC175 QUADRUPLE LOW-POWER DIFFERENTIAL LINE RECEIVERS

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## PARAMETER MEASUREMENT INFORMATION

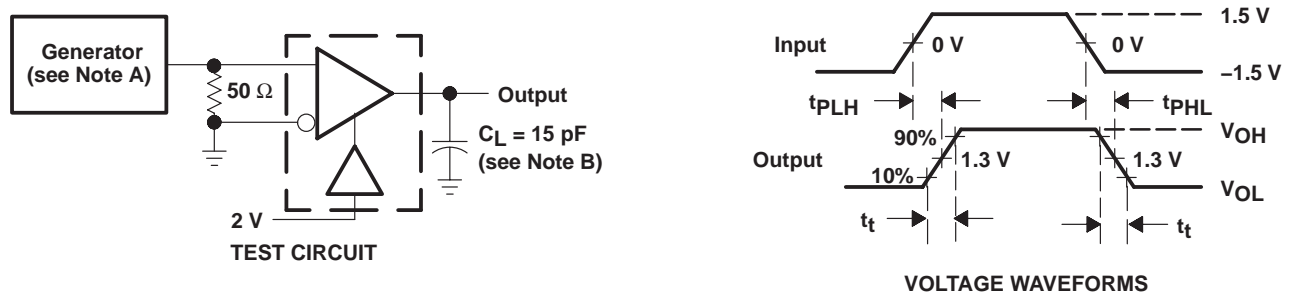
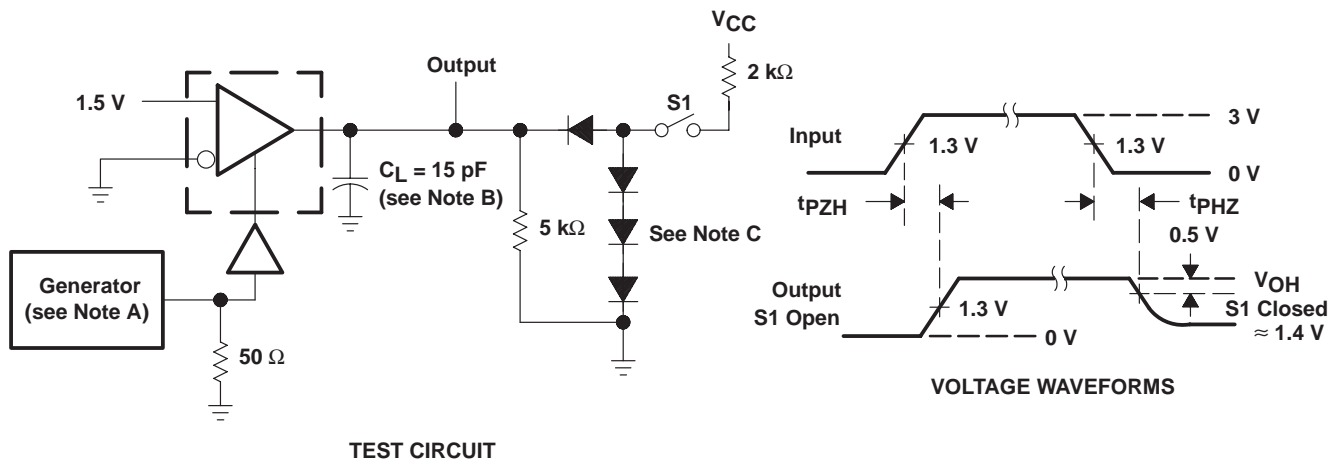


Figure 1.  $t_{pLH}$  and  $t_{pHL}$  Test Circuit and Voltage Waveforms



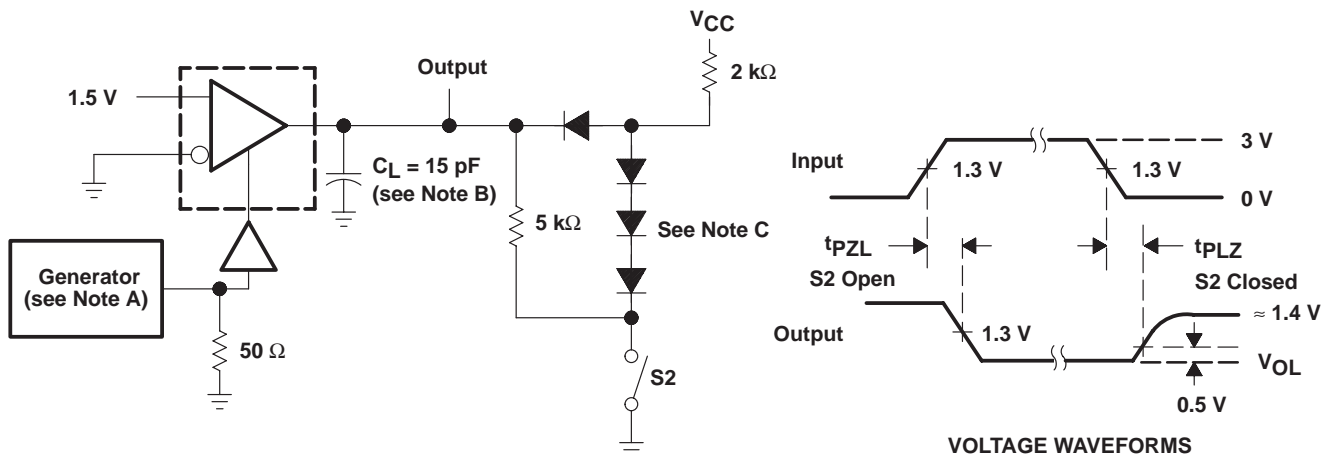
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.  
 C. All diodes are 1N916 or equivalent.

Figure 2.  $t_{pHZ}$  and  $t_{pZH}$  Test Circuit and Voltage Waveforms

# SN65LBC175, SN75LBC175 QUADRUPLE LOW-POWER DIFFERENTIAL LINE RECEIVERS

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## PARAMETER MEASUREMENT INFORMATION



### TEST CIRCUIT

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.  
 C. All diodes are 1N916 or equivalent.

Figure 3.  $t_{pZL}$  and  $t_{PLZ}$  Test Circuit and Voltage Waveforms

## TYPICAL CHARACTERISTICS

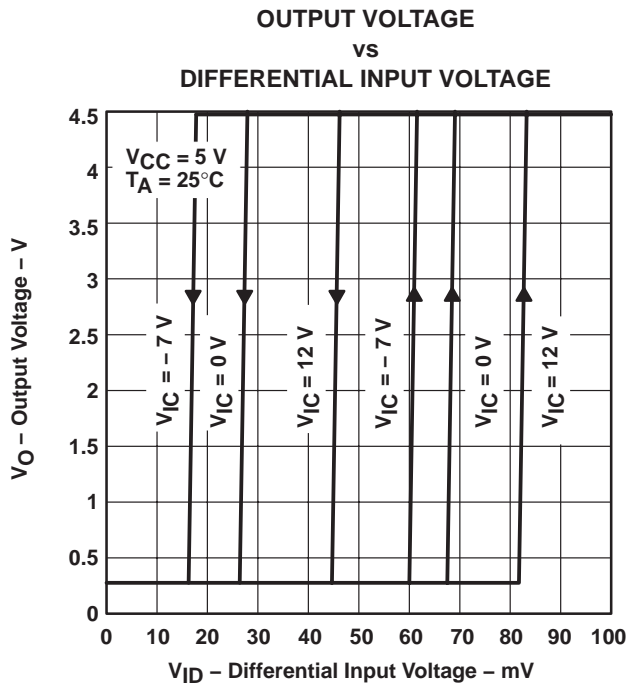


Figure 4

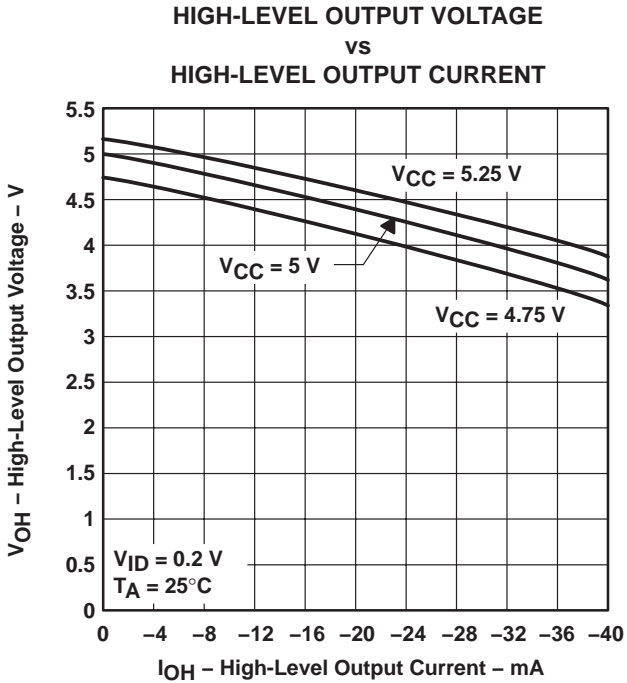


Figure 5

# SN65LBC175, SN75LBC175 QUADRUPLE LOW-POWER DIFFERENTIAL LINE RECEIVERS

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## TYPICAL CHARACTERISTICS

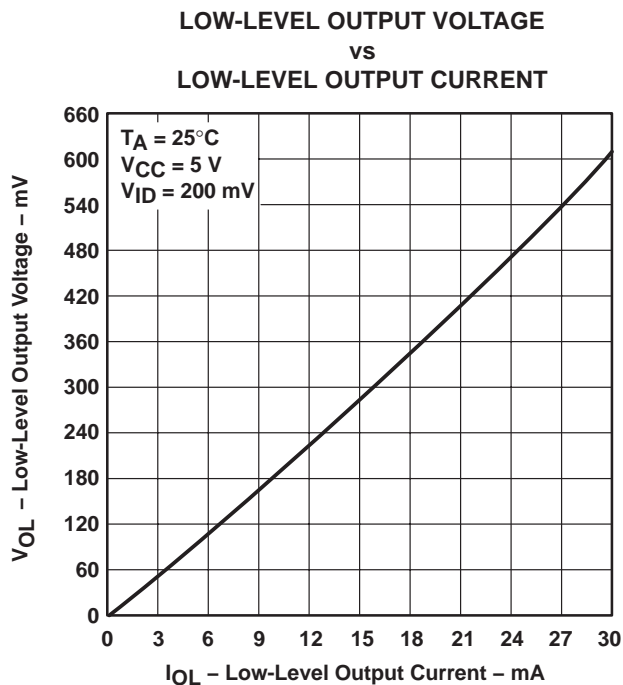


Figure 6

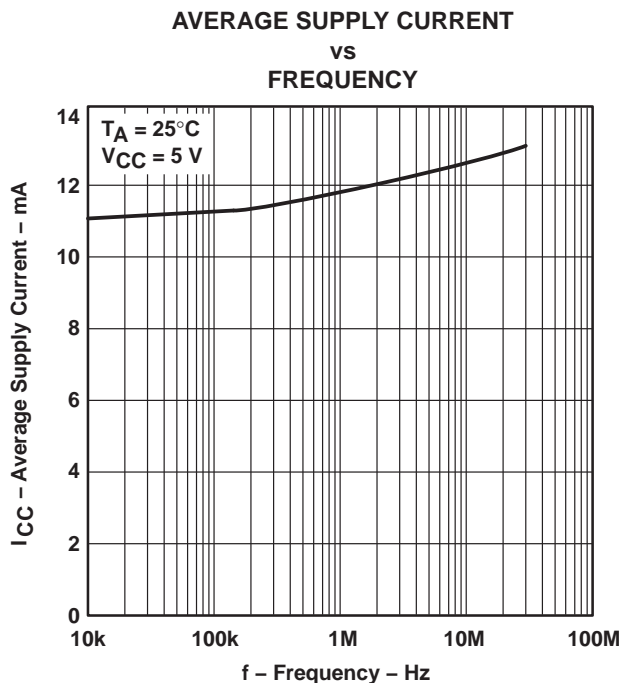


Figure 7

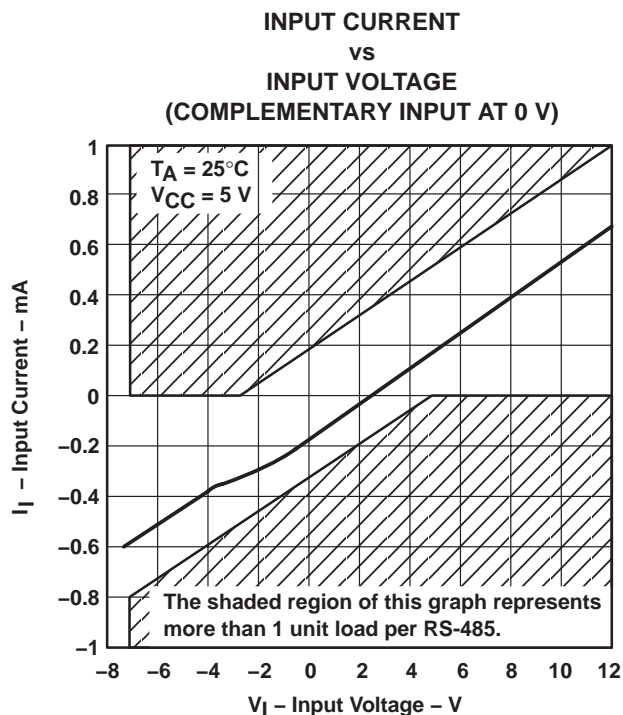


Figure 8

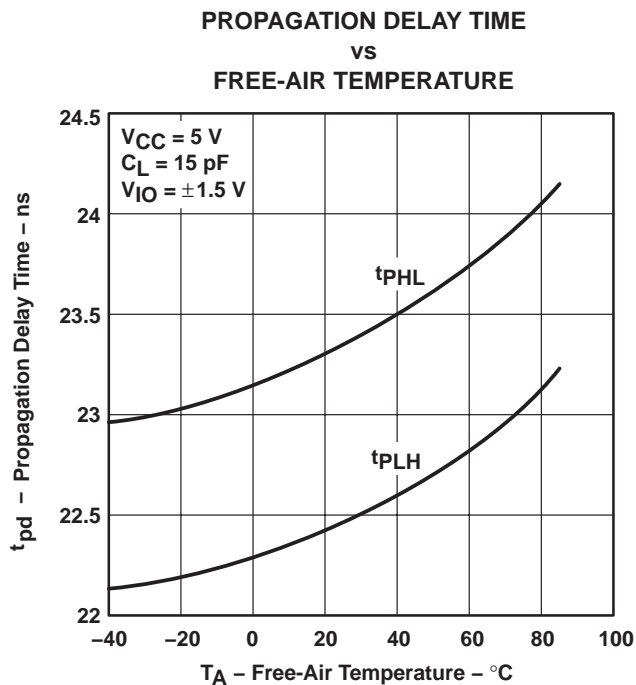


Figure 9

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC175D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC175	<a href="#">Samples</a>
SN65LBC175DG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC175	<a href="#">Samples</a>
SN65LBC175DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC175	<a href="#">Samples</a>
SN65LBC175DRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC175	<a href="#">Samples</a>
SN65LBC175DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC175	<a href="#">Samples</a>
SN65LBC175DWG4	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC175	<a href="#">Samples</a>
SN65LBC175DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC175	<a href="#">Samples</a>
SN65LBC175N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN65LBC175N	<a href="#">Samples</a>
SN75LBC175D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LBC175	<a href="#">Samples</a>
SN75LBC175DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LBC175	<a href="#">Samples</a>
SN75LBC175N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75LBC175N	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN75LBC175 :**

- Military : [SN55LBC175](#)

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC175DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LBC175DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
SN75LBC175DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC175DR	SOIC	D	16	2500	340.5	336.1	32.0
SN65LBC175DWR	SOIC	DW	16	2000	350.0	350.0	43.0
SN75LBC175DR	SOIC	D	16	2500	340.5	336.1	32.0

## GENERIC PACKAGE VIEW

**DW 16**

**SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A



# DW0016A

# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

### NOTES:

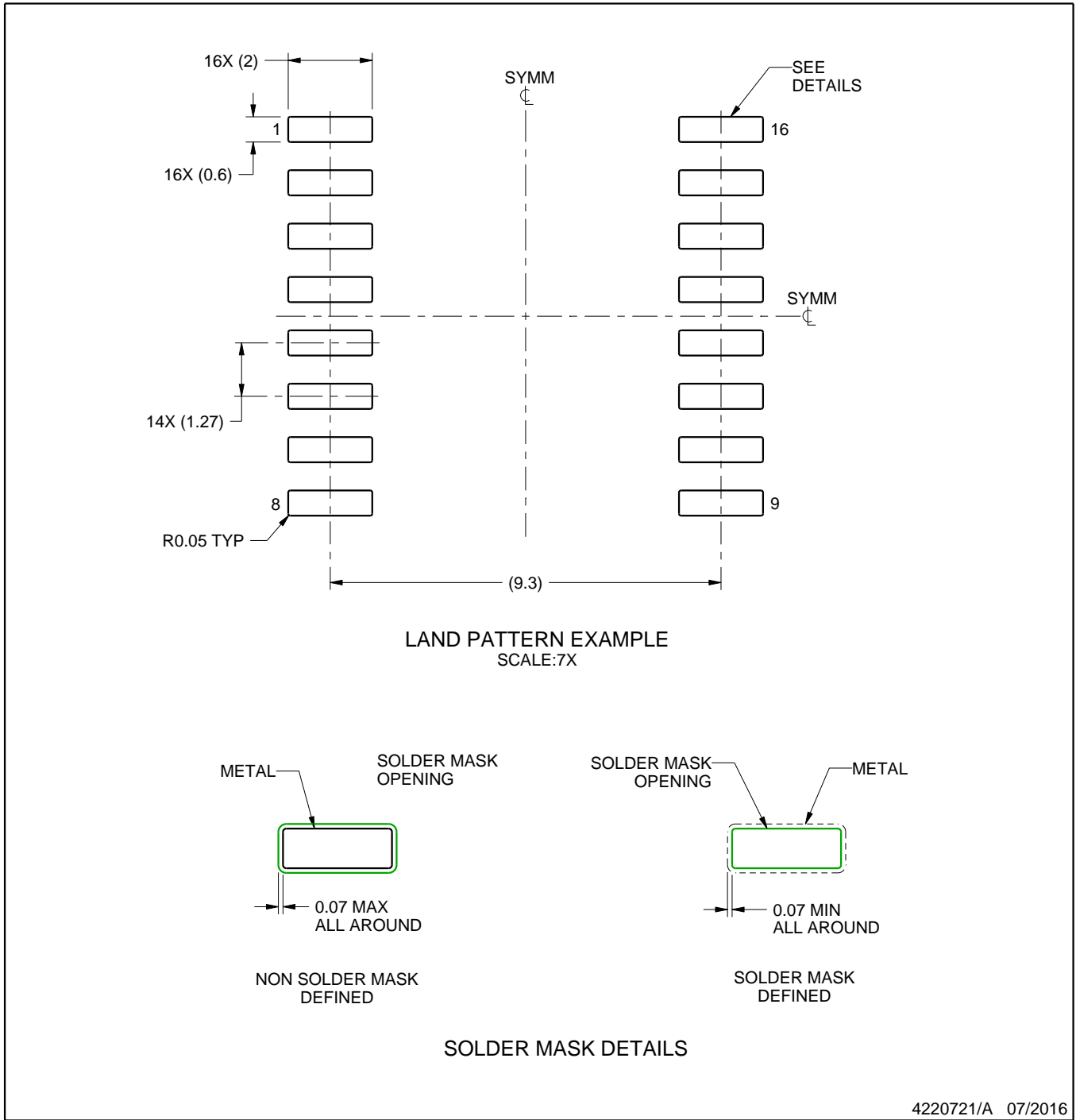
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211283-4/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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