# PROGRAMMABLE 27-BIT PARALLEL-TO-SERIAL RECEIVER

## FEATURES

- **FlatLink 3G Serial Interface Technology**
- **Compatible With FlatLink™ 3G Transmitters Such as SN65LVDS307**
- **Supports Video Interfaces up to 24-Bit RGB Data and 3 Control Bits Received Over Two Differential Data Lines**
- **SubLVDS Differential Voltage Levels**
- **Up to 810-Mbps Data Throughput**
- **Three Operating Modes to Conserve Power**
  - **Active mode VGA 60 fps: 17 mW**
  - **Typical Shutdown: 0.7 μW**
  - **Typical Standby Mode: 67 μW Typical**
- **ESD Rating > 4 kV (HBM)**
- **Pixel-Clock Range of 8 MHz–30 MHz**
- **Failsafe on all CMOS Inputs**
- **4-mm × 4-mm MicroStar Junior™μBGA® Package With 0,5-mm Ball Pitch**
- **Very Low EMI**

## APPLICATIONS

- **Small Low-Emission Interface Between Graphics Controller and LCD Display**
- **Mobile Phones and Smart Phones**
- **Portable Multimedia Players**

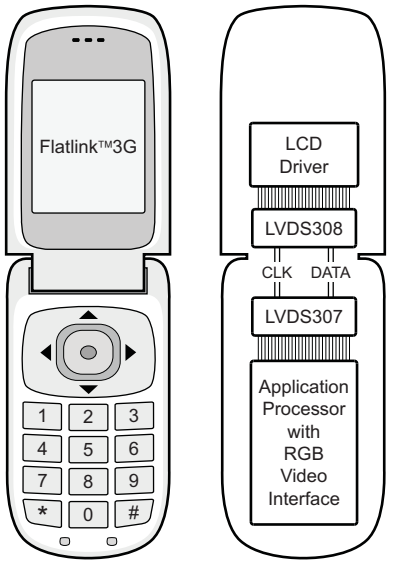
## DESCRIPTION

The SN65LVDS308 receiver deserializes FlatLink 3G-compliant serial input data to 27 parallel data outputs. The SN65LVDS308 receiver contains one shift register to load 30 bits from two serial inputs and latches the 24 pixel bits and 3 control bits out to the parallel CMOS outputs after checking the parity bit. If a parity error is detected, the data output bus disregards the newly received pixel. Instead, the last data word is held on the output bus for another clock cycle.

The serial data and clock are received via sub-low-voltage differential signalling (SubLVDS) lines. The SN65LVDS308 supports three operating power modes (shutdown, standby, and active) to conserve power.

When receiving, the PLL locks to the incoming clock, CLK, and generates an internal high-speed clock at the line rate of the data lines. The data is serially loaded into a shift register using the internal high-speed clock. The deserialized data is presented on the parallel output bus with a recreation of the pixel clock, PCLK, generated from the internal high-speed clock. If no input CLK signal is present, the output bus is held static with PCLK and DE held low, while all other parallel outputs are pulled high.

The F/S control input selects between a slow CMOS bus output rise time for best EMI and power consumption and a fast CMOS output for increased speed or higher-load designs.

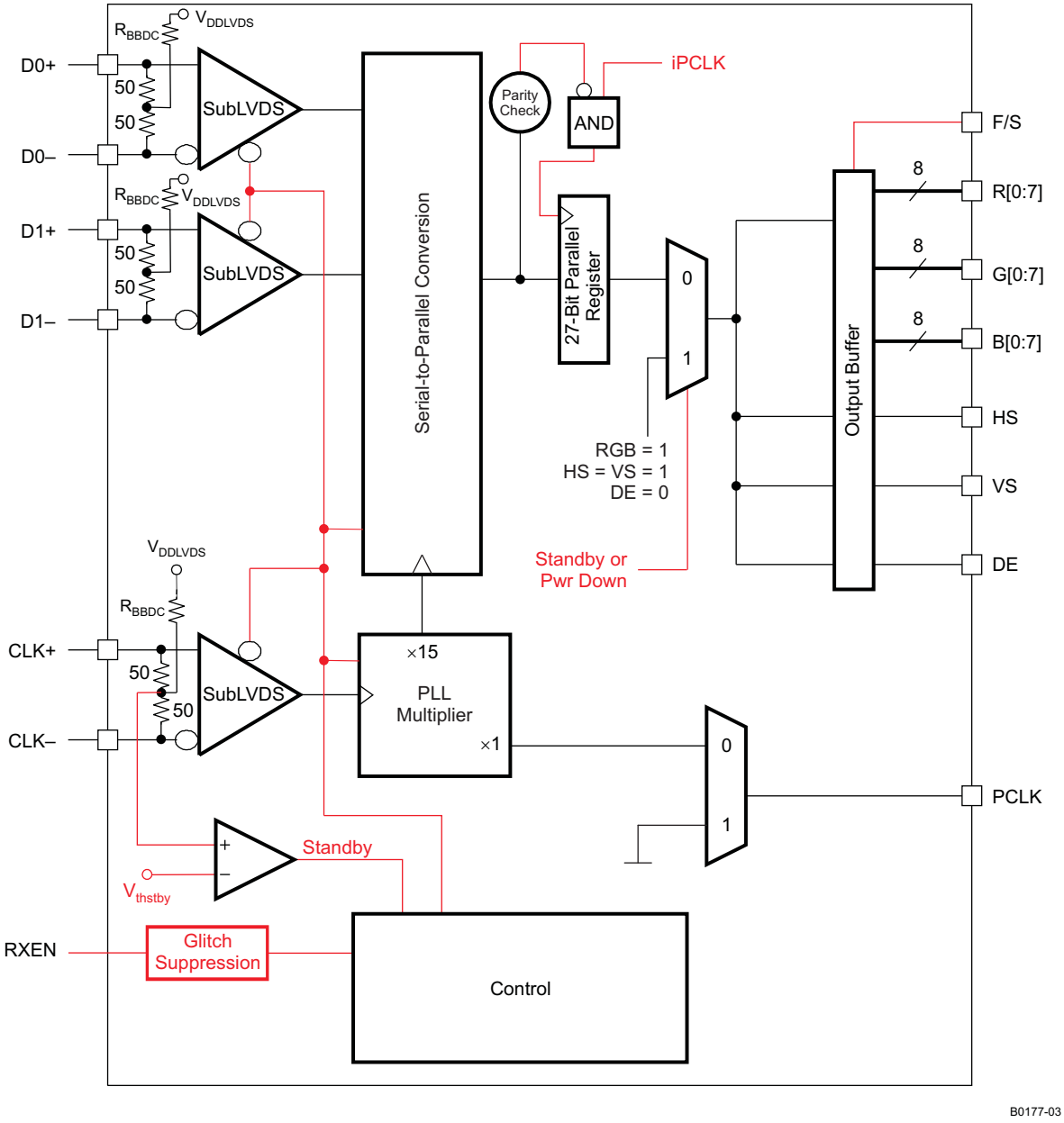


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## DESCRIPTION (CONTINUED)

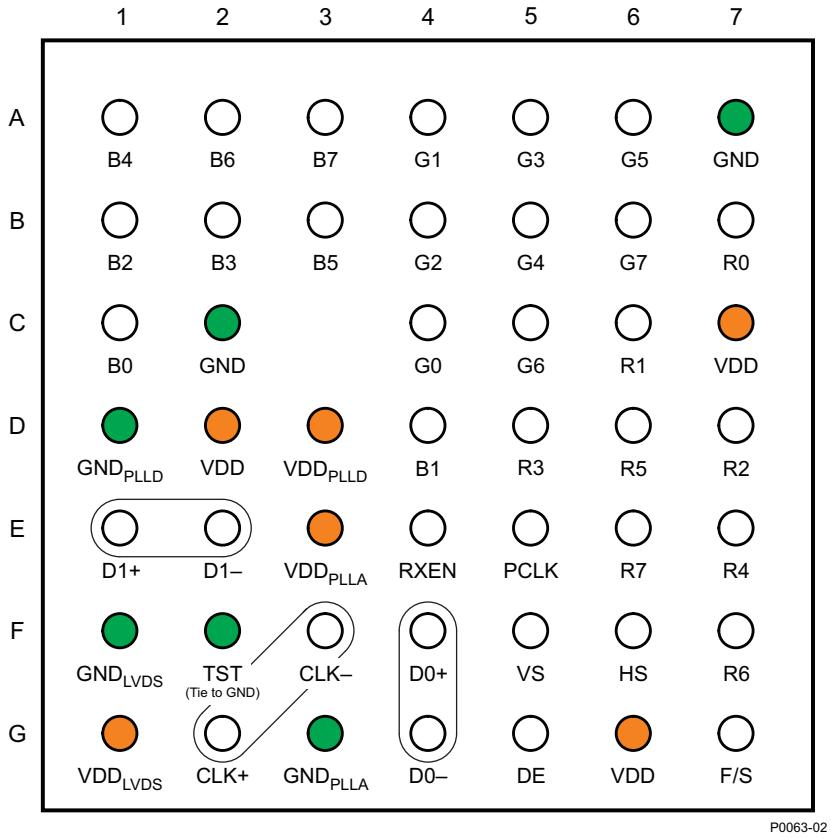
The RXEN input can be used to put the SN65LVDS308 in a shutdown mode. The SN65LVDS308 enters an active standby mode if the common-mode voltage of the CLK input becomes shifted to $VDD_{LVDS}$ (e.g., the transmitter releases the CLK output into high-impedance). This minimizes power consumption without the need of switching an external control pin. The SN65LVDS308 is characterized for operation over ambient air temperatures of –40°C to 85°C. All CMOS and SubLVDS signals are 2-V tolerant with VDD = 0 V. This feature allows powering up I/Os before VDD is stabilized.

### FUNCTIONAL BLOCK DIAGRAM



## PINOUT – TOP VIEW

**ZQC PACKAGE**
**(TOP VIEW)**

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## PINOUT – TOP VIEW (continued)

### Table 1. Numeric Terminal List

| TERMINAL | SIGNAL | TERMINAL | SIGNAL | TERMINAL | SIGNAL | TERMINAL | SIGNAL |
|---|---|---|---|---|---|---|---|
| **A1** | B4 | **B7** | R0 | **D6** | R5 | **F5** | VS |
| **A2** | B6 | **C1** | B0 | **D7** | R2 | **F6** | HS |
| **A3** | B7 | **C2** | GND | **E1** | D1+ | **F7** | R6 |
| **A4** | G1 | **C3** | – | **E2** | D1– | **G1** | $VDD_{LVDS}$ |
| **A5** | G3 | **C4** | G0 | **E3** | $VDD_{PLLA}$ | **G2** | CLK+ |
| **A6** | G5 | **C5** | G6 | **E4** | RXEN | **G3** | $GND_{PLLA}$ |
| **A7** | GND | **C6** | R1 | **E5** | PCLK | **G4** | D0– |
| **B1** | B2 | **C7** | VDD | **E6** | R7 | **G5** | DE |
| **B2** | B3 | **D1** | $GND_{PLLD}$ | **E7** | R4 | **G6** | VDD |
| **B3** | B5 | **D2** | VDD | **F1** | $GND_{LVDS}$ | **G7** | F/S |
| **B4** | G2 | **D3** | $VDD_{PLLD}$ | **F2** | TST | | |
| **B5** | G4 | **D4** | B1 | **F3** | CLK– | | |
| **B6** | G7 | **D5** | R3 | **F4** | D0+ | | |

**Table 2. TERMINAL FUNCTIONS**

| NAME | I/O | DESCRIPTION |
|---|---|---|
| D0+, D0– | SubLVDS in | SubLVDS data link |
| D1+, D1– | | SubLVDS data link |
| CLK+, CLK– | | SubLVDS input pixel clock; polarity is fixed. |
| R0–R7 | CMOS out | Red-pixel data (8) |
| G0–G7 | | Green-pixel data (8) |
| B0–B7 | | Blue-pixel data (8) |
| HS | | Horizontal sync |
| VS | | Vertical sync |
| DE | | Data enable |
| PCLK | | Output pixel clock (rising clock polarity) |
| RXEN | CMOS in | Disables the CMOS Drivers and Turns Off the PLL, putting device in shutdown mode<br>1 – Receiver enabled<br>0 – Receiver disabled (shutdown)<br>Note: The RXEN input incorporates glitch suppression logic to avoid unwanted switching. The input must be pulled low for longer than 10 µs continuously to force the receiver to enter shutdown. The input must be pulled high for at least 10 µs continuously to activate the receiver. An input pulse shorter than 5 µs is interpreted as a glitch and becomes ignored. At power up, the receiver is enabled immediately if RXEN = H and disabled if RXEN = L. |
| F/S | | CMOS bus rise time select<br>1 – fast-output rise time<br>0 – slow-output rise time |
| TST | | Test – this input is used for TI internal test purposes only and must be tied permanently to VSS. |
| VDD | Power supply | Supply voltage |
| GND | | Supply ground |
| $VDD_{LVDS}$ | | SubLVDS I/O supply voltage |
| $GND_{LVDS}$ | | SubLVDS ground |
| $VDD_{PLLA}$ | | PLL analog supply voltage |
| $GND_{PLLA}$ | | PLL analog GND |
| $VDD_{PLLD}$ | | PLL digital supply voltage |
| $GND_{PLLD}$ | | PLL digital GND |

## FUNCTIONAL DESCRIPTION

The SN65LVDS308 receives payload data over two SubLVDS data pairs, D0 and D1. The PLL locks to the SubLVDS clock input and internally multiplies the clock by a factor of 15. The internal high-speed clock is used to shift in the data payload on D0 and D1 and to deserialize 15 bits of data from each pair. Figure 1 illustrates the timing and the mapping of the data payload into the 30-bit frame. The internal high-speed clock is divided by a factor of 15 to recreate the pixel clock, and the data payload with pixel clock is presented on the output bus. The reserved bits and parity bit are not output.

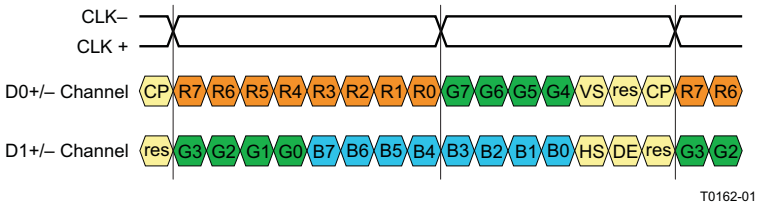



**Figure 1. Data and Clock Input**

## POWER-DOWN MODES

The SN65LVDS308 receiver has two power-down modes to facilitate efficient power management.

### Shutdown Mode

A low input signal on the RXEN pin puts the SN65LVDS308 into shutdown mode. This turns off most of the receiver circuitry, including the SubLVDS receivers, PLL, and deserializers. The SubLVDS differential-input resistance remains 100 Ω, and any input signal is ignored. All outputs hold a static output pattern:

R[0:7] = G[0:7] = B[0:7] = VS = HS = high; DE = PCLK = low.

The current draw in shutdown mode is nearly zero if the SubLVDS inputs are left open or pulled high.

### Standby Mode

The SN65LVDS308 enters the standby mode when the SN65LVDS308 is not in shutdown mode but the clock-input common-mode voltage on the SubLVDS clock input is above 0.9 × $VDD_{LVDS}$. The CLK input incorporates pullup circuitry. This circuit shifts the SubLVDS clock-input common-mode voltage to $VDD_{LVDS}$ in the absence of an input signal. All circuitry except the SubLVDS clock-input standby monitor is shut down. The SN65LVDS308 also enters the standby mode when the input clock frequency on the CLK input is less than 500 kHz. The SubLVDS input resistance remains 100 Ω, and any input signal on data inputs D0 and D1 is ignored. All outputs hold a static output pattern:

R[0:7] = G[0:7] = B[0:7] = VS = HS = high; DE = PCLK = low.

The current draw in standby mode is very low.

## ACTIVE MODES

A high input signal on RXEN combined with a CLK input signal switching faster than 3 MHz and $V_{ICM}$ smaller than 0.9 VDD forces the SN65LVDS308 into the active mode. Current consumption in the active mode depends on operating frequency and the number of data transitions in the data payload. CLK-input frequencies between 3 MHz and 8 MHz activate the device, but proper PLL functionality is not assured.

### Acquire Mode (PLL Approaches Lock)

When the SN65LVDS308 is enabled and a SubLVDS clock input is present, the PLL pursues lock to the input clock. While the PLL pursues lock, the output data bus holds a static output pattern:

R[0:7] = G[0:7] = B[0:7] = VS = HS = high; DE = PCLK = low.

## FUNCTIONAL DESCRIPTION (continued)

For proper device operation, the pixel clock frequency must fall within the valid $f_{PCLK}$ range specified under recommended operating conditions. If the pixel clock frequency is larger than 3 MHz but smaller than $f_{PCLK(min)}$, the SN65LVDS308 PLL is enabled. Under such conditions, it is possible for the PLL to lock temporarily to the pixel clock, causing the PLL monitor to release the device into active receive mode. If this happens, the PLL may or may not be properly locked to the pixel clock input, potentially causing data errors, frequency oscillation, and PLL deadlock (loss of VCO oscillation).

### Receive Mode

After the PLL achieves lock the device enters the normal receive mode. The output data bus presents the deserialized data. The PCLK output pin outputs the recovered pixel clock.

### *PARITY ERROR DETECTION AND HANDLING*

The SN65LVDS308 receiver performs error checking on the basis of a parity bit that is transmitted across the SubLVDS interface from the transmitting device. Once the SN65LVDS308 detects the presence of the clock and the PLL has locked onto PCLK, then the parity is checked. Parity-error detection ensures detection of all single-bit errors in one pixel and 50% of all multibit errors.

The parity bit covers the 27-bit data payload consisting of 24 bits of pixel data plus VS, HS, and DE. Odd-parity bit signalling is used. If the sum of the 27 data bits and the parity bit is an odd number, the receive data are assumed to be valid. If the sum equals an even number, parity error is declared.

If a parity error is detected, then the data on that PCLK cycle is not output. Instead, the last valid data from a previous PCLK cycle is repeated on the output bus. This is to prevent any bit error that occurs on the LVDS link from causing perturbations in VS, HS, or DE that might be visually disruptive to a display.

The reserved bits are not covered in the parity calculations.

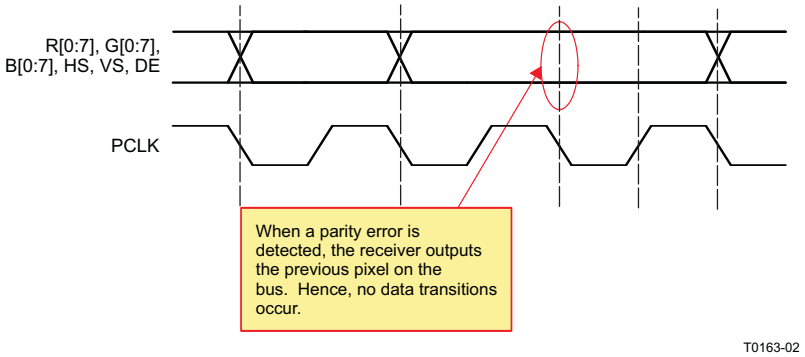



**Figure 2. Output Response When Parity Error Is Detected**

## FUNCTIONAL DESCRIPTION (continued)

### STATUS-DETECT AND OPERATING-MODES FLOW DIAGRAM

The SN65LVDS308 switches between the power saving and active modes in the following way:

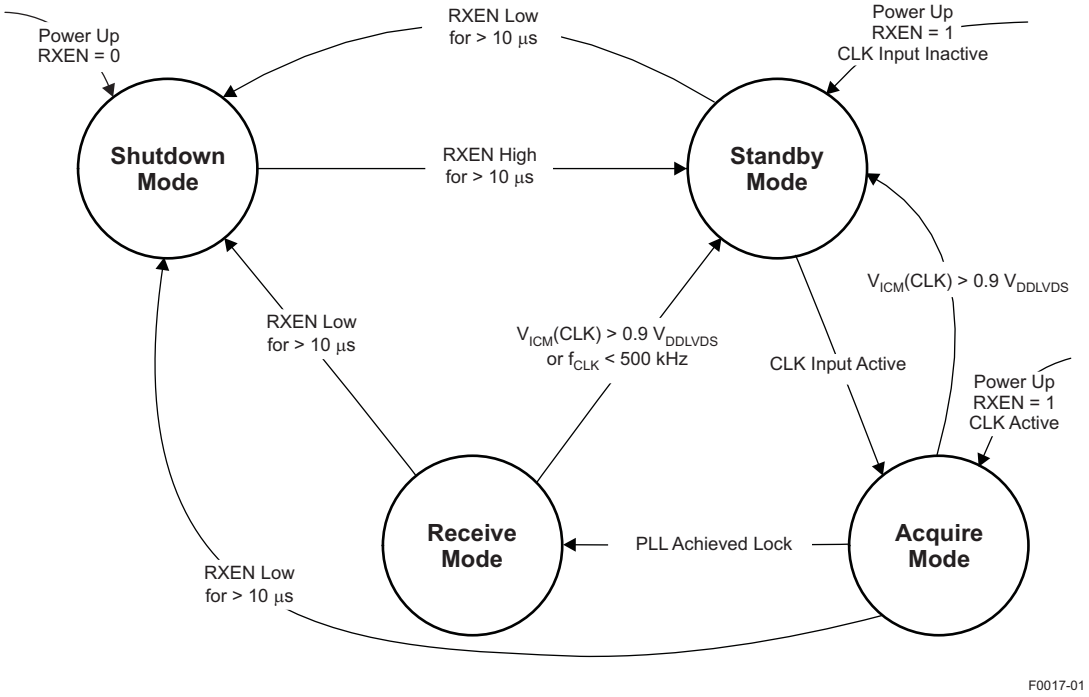



**Figure 3. Operating Modes Flow Diagram**

**Table 3. Status Detect and Operating Modes Descriptions**

| MODE | CHARACTERISTICS | CONDITIONS |
|---|---|---|
| Shutdown mode | Least amount of power consumption (most circuitry turned off); all outputs held static:<br>R[0:7] = G[0:7] = B[0:7] = VS = HS = high; DE = PCLK = low | RXEN is set low for longer than 10 µs. (1)(2) |
| Standby mode | Low power consumption (standby monitor circuit active; PLL is shut down to conserve power);<br>All outputs held static:<br>R[0:7] = G[0:7] = B[0:7] = VS = HS = high;<br>DE = PCLK = low | RXEN is high for longer than 10 µs and both CLK inputs are common-mode, $V_{ICM(CLK)}$ is above $0.9 \times VDD_{LVDS}$, or CLK inputs are floating (2) |
| Acquire mode | PLL pursues lock; all outputs held static:<br>R[0:7] = G[0:7] = B[0:7] = VS = HS = high; DE = PCLK = low | RXEN is high; CLK input monitor detected clock input common mode and woke up receiver from standby mode. |
| Receive mode | Data transfer (normal operation);<br>receiver deserializes data and provides data on parallel output | RXEN is high and PLL is locked to incoming clock. |

(1) In shutdown mode, all SN65LVDS308 internal switching circuits (e.g., PLL, serializer, etc.) are turned off to minimize power consumption. The input stage of any input pin remains active.

(2) Leaving inputs unconnected can cause random noise to toggle the input stage and potentially harm the device. All CMOS inputs must be tied to a valid logic level, $V_{IL}$ or $V_{IH}$, during shutdown or standby mode. Exceptions are the SubLVDS inputs CLK and Dx, which can be left unconnected while not in use.

**Table 4. Operating Mode Transitions**

| MODE TRANSITION | USE CASE | TRANSITION SPECIFICS |
|---|---|---|
| Shutdown → standby | Drive RXEN high to enable receiver. | 1. RXEN high > 10 µs<br>2. Receiver enters standby mode.<br>a. R[0:7] = G[0:7] = B[0:7] = VS = HS remain high and DE = PCLK low<br>b. Receiver activates clock input monitor. |
| Standby → acquire | Transmitter activity detected | 1. CLK input monitor detects clock input activity.<br>2. Outputs remain static.<br>3. PLL circuit is enabled. |
| Acquire → receive | Link is ready to receive data. | 1. PLL is active and approaches lock.<br>2. PLL achieves lock within $t_{wakeup}$.<br>3. First data word is recovered.<br>4. Parallel output bus turns on switching from a static output pattern to output the first valid data word. |
| Receive → standby | Transmitter requested to enter standby mode by input common-mode voltage $V_{ICM}$ > 0.9 $VDD_{LVDS}$ (e.g., transmitter output clock enters high-impedance state) | 1. Receiver disables outputs within $t_{sleep}$.<br>2. RX input monitor detects $V_{ICM}$ > 0.9 $VDD_{LVDS}$.<br>3. R[0:7] = G[0:7] = B[0:7] = VS = HS transition to high and DE = PCLK to low on next falling PLL clock edge.<br>4. PLL shuts down.<br>5. Clock activity input monitor remains active. |
| Receive/standby → shutdown | Turn off receiver. | 1. RXEN pulled low for > $t_{pwrdn}$.<br>2. Receiver switches all outputs to high-impedance state.<br>3. Most IC circuitry is shut down for least power consumption. |

## ABSOLUTE MAXIMUM RATINGS(1)

| | | VALUE | UNIT |
|---|---|---|---|
| Supply voltage range, VDD(2), $VDD_{PLLA}$, $VDD_{PLLD}$, $VDD_{LVDS}$ | | –0.3 to 2.175 | V |
| Voltage range at any input or output terminal | When $VDD_x$ > 0 V | –0.5 to 2.175 | V |
| | When $VDD_x$ ≤ 0 V | –0.5 to VDD + 2.175 | |
| Electrostatic discharge | Human body model(3) (all pins) | ±4 | kV |
| | Charged-device model(4) (all pins) | ±1500 | V |
| | Machine model(5) (all pins) | ±200 | |
| Continuous power dissipation | | See Dissipation Ratings Table | |
| Ouput current, $I_O$ | | ±5 | mA |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND terminals.
(3) In accordance with JEDEC Standard 22, Test Method A114-B
(4) In accordance with JEDEC Standard 22, Test Method C101
(5) In accordance with JEDEC Standard 22, Test Method A115-A

## DISSIPATION RATINGS

| PACKAGE | CIRCUIT BOARD MODEL | $T_A$ < 25°C | DERATING FACTOR(1) ABOVE $T_A$ = 25°C | $T_A$ = 85°C POWER RATING |
|---|---|---|---|---|
| ZQC | Low-K(2) | 496 mW | 6.21 mW/°C | 124 mW |

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) In accordance with the low-K thermal metric definitions of EIA/JESD51-2.

## DEVICE POWER DISSIPATION

| PARAMETER | | TEST CONDITIONS | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $P_D$ | Device power dissipation | $VDD_x$ = 1.8 V, $T_A$ = 25°C, all outputs terminated with 10 pF, $f_{CLK}$ at 8 MHz | 11.5 | | mW |
| | | $VDD_x$ = 1.95 V, $T_A$ = –40°C, all outputs terminated with 10 pF, $f_{CLK}$ at 30 MHz | | 72.2 | |

## RECOMMENDED OPERATING CONDITIONS(1)

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{DD}$<br>$V_{DD_{PLLA}}$<br>$V_{DD_{PLLD}}$<br>$V_{DD_{LVDS}}$ | Supply voltages | | 1.65 | 1.8 | 1.95 | V |
| $V_{DD_{n(PP)}}$ | Supply voltage noise magnitude | Test setup shown in Figure 5; f(noise) = 1Hz to 2 GHz | | | 100 | mV |
| | | f(noise) = 1Hz to 1MHz | | | 100 | |
| | | f(noise) > 1MHz | | | 40 | |
| $T_A$ | Operating free-air temperature | | –40 | | 85 | °C |
| **CLK+ and CLK–** | | | | | | |
| $f_{CLK\pm}$ | Input pixel clock frequency | See Figure 1 | 8 | | 30 | MHz |
| | | Standby mode(2), see Figure 14 | | | 500 | kHz |
| $t_{DUTCLK}$ | CLK input duty cycle | | 35 | | 65 | % |
| **D0+, D0–, D1+, D1–, CLK+, and CLK–** | | | | | | |
| $\|V_{ID}\|$ | Magnitude of differential input voltage | $\|V_{D0+} - V_{D0-}\|$, $\|V_{D1+} - V_{D1-}\|$, $\|V_{CLK+} - V_{CLK-}\|$ during normal operation | 70 | | 200 | mV |
| $V_{ICM}$ | Input voltage common mode range | Receive or acquire mode | 0.6 | | 1.2 | V |
| | | Standby mode | 0.9 $V_{DD_{LVDS}}$ | | | |
| $\Delta V_{ICM}$ | Input voltage common mode variation among all SubLVDS inputs | $V_{ICM(n)} - V_{ICM(m)}$ with n = D0, D1, or CLK and m = D0, D1, or CLK | –100 | | 100 | mV |
| $\Delta V_{ID}$ | Differential input voltage amplitude variation among all SubLVDS inputs | $V_{ID(n)} - V_{ID(m)}$ with n = D0, D1, or CLK and m = D0, D1, or CLK | –10 | | 10 | % |
| $t_{r/f}$ | Input rise and fall times | RXEN at VDD; see Figure 8 | | | 800 | ps |
| $\Delta t_{r/f}$ | Input rise or fall time mismatch among all SubLVDS inputs | $t_{r(n)} - t_{r(m)}$ and $t_{f(n)} - t_{f(m)}$ with n = D0, D1, or CLK and m = D0, D1, or CLK | –100 | | 100 | ps |
| **RXEN, F/S** | | | | | | |
| $V_{ICMOSH}$ | High-level input voltage | | 0.7 VDD | | VDD | V |
| $V_{ICMOSL}$ | Low-level input voltage | | 0 | | 0.3 VDD | V |
| $t_{inRXEN}$ | RXEN input pulse duration | | 10 | | | µs |
| **R[7:0], G[7:0], B[7:0], VS, HS, PCLK** | | | | | | |
| $C_L$ | Output load capacitance | | | 10 | | pF |

(1) Unused single-ended inputs must be held high or low to prevent them from floating.
(2) PCLK input frequencies lower than 500 kHz force the SN65LVDS308 into standby mode. Input frequencies between 500 kHz and 3 MHz may or may not activate the SN65LVDS308. Input frequencies beyond 3 MHz activate the SN65LVDS308. Input frequencies between 500 kHz and 4 MHz are not recommended, and can cause PLL malfunction.

## DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ | RMS supply current | Alternating 1010 test pattern (see **Table 8*****); all CMOS outputs terminated with 10 pF; F/S and RXEN at VDD; $V_{IH}$ = VDD, $V_{IL}$ = 0 V; VDD = $V_{DD_{PLLA}}$ = $V_{DD_{PLLD}}$ = $V_{DD_{LVDS}}$ | $f_{PCLK}$ = 8 MHz | | 14.3 | 19.4 | mA |
| | | | $f_{PCLK}$ = 22 MHz | | 25 | 33 | |
| | | | $f_{PCLK}$ = 30 MHz | | 26.8 | 37 | |
| | | Typical power test pattern (see Table 6); $V_{ID}$ = 70 mV, all CMOS outputs terminated with 10 pF; F/S at GND and RXEN at VDD; $V_{IH}$ = VDD, $V_{IL}$ = 0 V; VDD = $V_{DD_{PLLA}}$ = $V_{DD_{PLLD}}$ = $V_{DD_{LVDS}}$ | $f_{PCLK}$ = 8 MHz | | 6.4 | | mA |
| | | | $f_{PCLK}$ = 22 MHz | | 13.7 | | |
| | | | $f_{PCLK}$ = 30 MHz | | 18.3 | | |
| | | CLK and Dx inputs are left open; all control inputs held static high or low; All CMOS outputs terminated with 10 pF; $V_{IH}$ = VDD, $V_{IL}$ = 0 V; VDD = $V_{DD_{PLLA}}$ = $V_{DD_{PLLD}}$ = $V_{DD_{LVDS}}$ | Standby mode; RXEN = $V_{IH}$ | | 15 | 100 | µA |
| | | | Shutdown mode; RXEN = $V_{IL}$ | | 0.4 | 10 | |

(1) All typical values are at 25°C and with 1.8-V supply, unless otherwise noted.

## INPUT ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| **D0+, D0–, D1+, D1–, CLK+, and CLK–** | | | | | | |
| $V_{thstby}$ | Input voltage common mode threshold to switch between receive/acquire mode and standby mode | RXEN at VDD | 1.3 | | 0.9 $VDD_{LVDS}$ | V |
| $V_{THL}$ | Low-level differential input voltage threshold | $V_{D0+} - V_{D0-}$, $V_{D1+} - V_{D1-}$, $V_{CLK+} - V_{CLK-}$ | –40 | | | mV |
| $V_{THH}$ | High-level differential input voltage threshold | | | | 40 | mV |
| $I_{I+}$, $I_{I-}$ | Input leakage current | VDD = 1.95 V; $V_{I+} = V_{I-}$; $V_I$ = 0.4 V or $V_I$ = 1.5 V | | | 75 | µA |
| $I_{IOFF}$ | Power-off input current | VDD = GND; $V_I$ = 1.5 V | | | –75 | µA |
| $R_{ID}$ | Differential input termination resistor value | | 78 | 100 | 122 | Ω |
| $C_{IN}$ | Input capacitance | Measured between input terminal and GND | | 1 | | pF |
| $\Delta C_{IN}$ | Input capacitance variation | Within one signal pair | | | 0.2 | pF |
| | | Between all signals | | | 1 | |
| $R_{BBDC}$ | Pullup resistor for standby detection | | 21 | 30 | 39 | kΩ |
| **RXEN, F/S** | | | | | | |
| $V_{IK}$ | Input clamp voltage | $I_I$ = –18 mA, VDD = VDD(min) | | | –1.2 | V |
| $I_{ICMOS}$ | Input current(2) | 0 V ≤ VDD ≤ 1.95 V; $V_I$ = GND or $V_I$ = 1.95 V | | | 100 | nA |
| $C_{IN}$ | Input capacitance | | | 2 | | pF |
| $I_{IH}$ | High-level input current | $V_{IN}$ = 0.7 VDD | –200 | | 200 | nA |
| $I_{IL}$ | Low-level input current | $V_{IN}$ = 0.3 VDD | –200 | | 200 | |
| $V_{IH}$ | High-level input voltage | | 0.7 VDD | | VDD | V |
| $V_{IL}$ | Low-level input voltage | | 0 | | 0.3 VDD | |

(1) All typical values are at 25°C and with 1.8-V supply unless otherwise noted.
(2) Do not leave any CMOS input unconnected or floating to minimize leakage currents. Every input must be connected to a valid logic level, $V_{IH}$ or $V_{OL}$, while power is supplied to VDD.

## OUTPUT ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **R[0:7], G[0:7], B[0:7], VS, HS, PCLK** | | | | | | |
| $V_{OH}$ | High-level output current | F/S = L, $I_{OH}$ = –500 µA | 0.8 VDD | | VDD | V |
| | | F/S = H, $I_{OH}$ = –2 mA | | | | |
| $V_{OL}$ | Low-level output current | F/S = L, $I_{OL}$ = 500 µA | | 0 | 0.2 VDD | V |
| | | F/S = H, $I_{OL}$ = 2 mA | | | | |
| $I_{OH}$ | High-level output current | F/S = L | –500 | | | µA |
| | | F/S = H | –2000 | | | |
| $I_{OL}$ | Low-level output current | F/S = L | | | 500 | µA |
| | | F/S = H | | | 2000 | |

## SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **D0+, D0–, D1+, D1–, CLK+, and CLK–** | | | | | | | |
| $t_{r/f}$ | Input rise and fall times | RXEN at VDD; see Figure 8 | | | | 800 | ps |
| $\Delta t_{r/f}$ | Input rise or fall time mismatch between all SubLVDS inputs | $t_r(n) - t_r(m)$ and $t_f(n) - t_f(m)$ with n = D0, D1, or CLK and m = D0, D1, or CLK | | –100 | | 100 | ps |
| **R[7:0], G[7:0], B[7:0], VS, HS, PCLK** | | | | | | | |
| $t_{r/f}$ | Rise and fall time 20%–80% of VDD (2) | $C_L$ = 10 pF(3); see Figure 7 | F/S = L | 4 | | 8 | ns |
| | | | F/S = H | 1 | | 2 | |
| $t_{OUTP}$ | PCLK output duty cycle | | | 48% | 53% | 59% | |
| $t_{OSK}$ | Output skew between PCLK and R[0:7], G[0:7], B[0:7], HS, VS, and DE | See Figure 7. | | –500 | | 500 | ps |
| **INPUT-TO-OUTPUT RESPONSE TIME** | | | | | | | |
| $t_{PD(L)}$ | Propagation delay time from CLK+ input to PCLK output | RXEN at VDD, $V_{IH}$ = VDD, $V_{IL}$ = GND, $C_L$ = 10 pF, see Figure 12 | | 1.4/$f_{PCLK}$ | 1.9/$f_{PCLK}$ | 2.5/$f_{PCLK}$ | s |
| $t_{GS}$ | RXEN glitch suppression pulse width(4) | $V_{IH}$ = VDD, $V_{IL}$ = GND, RXEN toggles between $V_{IL}$ and $V_{IH}$; see Figure 13 and Figure 14. | | | | 3.8 | µs |
| $t_{pwrup}$ | Enable time from power down (↑RXEN) | Time from RXEN pulled high to data outputs enabled and transmit valid data; see Figure 14. | | | | 2 | ms |
| $t_{pwrdn}$ | Disable time from active mode (↓RXEN) | RXEN is pulled low during receive mode; time measurement until all outputs held static: R[0:7] = G[0:7] = B[0:7] = VS = HS = high, DE = PCLK = low and PLL is shut down; see Figure 14. | | | | 11 | µs |
| $t_{wakeup}$ | Enable time from standby (↑↓CLK) | RXEN at VDD; device is in standby; time measurement from CLK input start of switching until PCLK and data outputs enabled and transmitting valid data; see Figure 15. | | | | 2 | ms |
| $t_{sleep}$ | Disable time from active mode (CLK transitions to high-impedance) | RXEN at VDD; device is receiving data; time measurement from CLK input signal stops (input open or input common mode $V_{ICM}$ exceeds threshold voltage $V_{thstby}$) until all outputs held static: R[0:7] = G[0:7] = B[0:7] = VS = HS = high; DE = PCLK = low and PLL is shut down; see Figure 15. | | | | 3 | µs |
| $f_{BW}$ | PLL bandwidth(5) | Tested from CLK input to PCLK output; $f_{PCLK}$ = 22 MHz | | 0.087 $f_{PCLK}$ | | | MHz |

(1) All typical values are at 25°C and with 1.8-V supply, unless otherwise noted.
(2) $t_{r/f}$ depends on the F/S setting and the capacitive load connected to each output. Some application information of how to calculate $t_{r/f}$ based on the output load and how to estimate the timing budget to interconnect to an LCD driver are provided in the application section near the end of this data sheet.
(3) The output rise and fall times are optimized for an output load of 10 pF. The rise and fall times can be adjusted by changing the output load capacitance.
(4) The RXEN input incorporates glitch-suppression logic to disregard short input pulses. $t_{GS}$ is the duration of either a high-to-low or low-to-high transition that is suppressed.
(5) When using the SN65LVDS308 receiver in conjunction with the SN65LVDS307 transmitter in one link, the PLL bandwidth of the SN65LVDS308 receiver always exceeds the bandwidth of the SN65LVDS307 transmit PLL. This ensures stable PLL tracking under all operating conditions and maximizes the receiver skew margin.

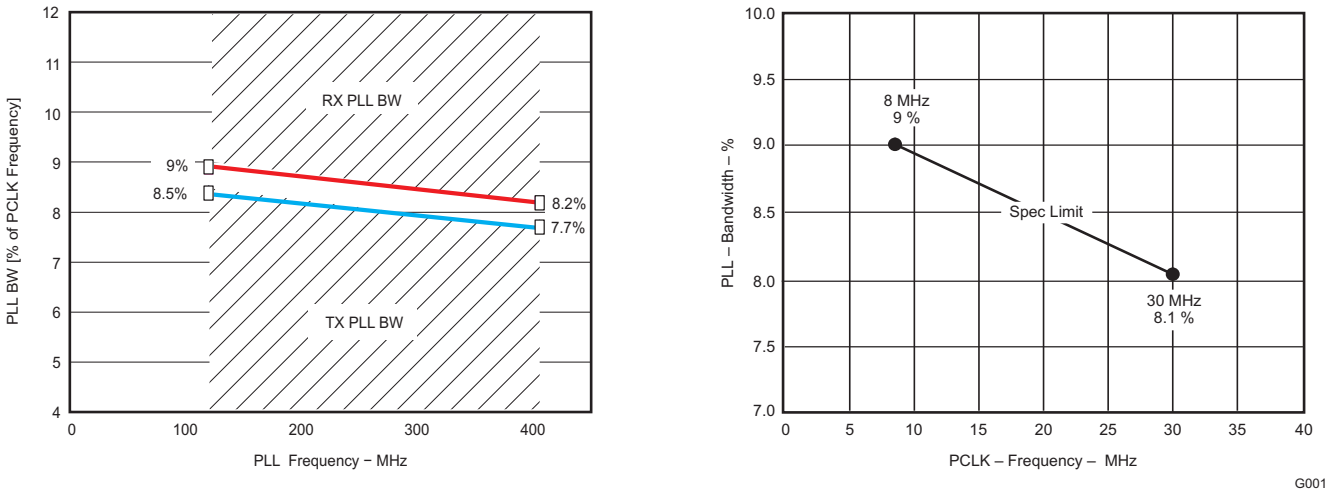



**Figure 4. SN65LVDS308 PLL Bandwidth (Also Showing the SN65LVDS307 PLL Bandwidth)**

## TIMING CHARACTERISTICS

| PARAMETER | | TEST CONDITIONS | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{RSKMx}$ (1)(2) | Receiver input skew margin; See (3) and Figure 30 | x = 0..14, $f_{PCLK}$ =30 MHz RXEN at VDD, $V_{IH}$ = VDD, $V_{IL}$ = GND, $R_L$ = 100 Ω, test setup as in Figure 6, test pattern as in Table 9 | $f_{CLK}$ = 30 MHz (4) | 630 | | ps |
| | | | $f_{CLK}$ = 8 MHz to 30 MHz (5) | $\frac{1}{2 \bullet 15 \bullet f_{CLK}} - 480\,ps$ | | |

(1) Receiver input skew margin ($t_{RSKM}$) is the timing margin available for transmitter output pulse position ($t_{PPOS}$), interconnect skew, and interconnect inter-symbol interference. $t_{RSKM}$ represents the remainder of the serial bit time not taken up by the receiver strobe uncertainty. $t_{RSKM}$ assumes a bit error rate better than $10^{-12}$.
(2) $t_{RSKM}$ is inversely proportional to the internal setup and hold time uncertainty, ISI and duty cycle distortion from the front end receiver, the skew missmatch between CLK and data D0 and D1, as well as the PLL cycle-to-cycle jitter.
(3) This includes the receiver internal setup and hold time uncertainty, all PLL-related high-frequency random and deterministic jitter components that impact the jitter budget, ISI and duty cycle distortion from the front-end receiver, and the skew between CLK and data D0 and D1; the pulse position minimum/maximum variation is given with a bit error rate target of $10^{-12}$; measurements of the total jitter are taken over $>10^{12}$ samples.
(4) The minimum and maximum limits are based on statistical analysis of the device performance over process, voltage, and temperature ranges.
(5) These minimum and maximum limits are simulated only.

## PARAMETER MEASUREMENT INFORMATION

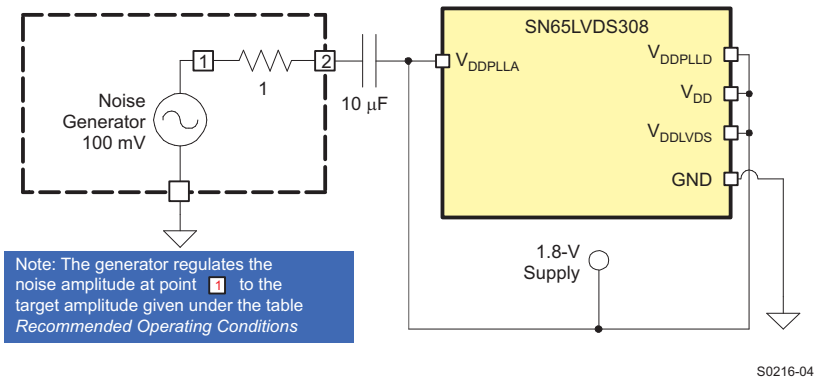
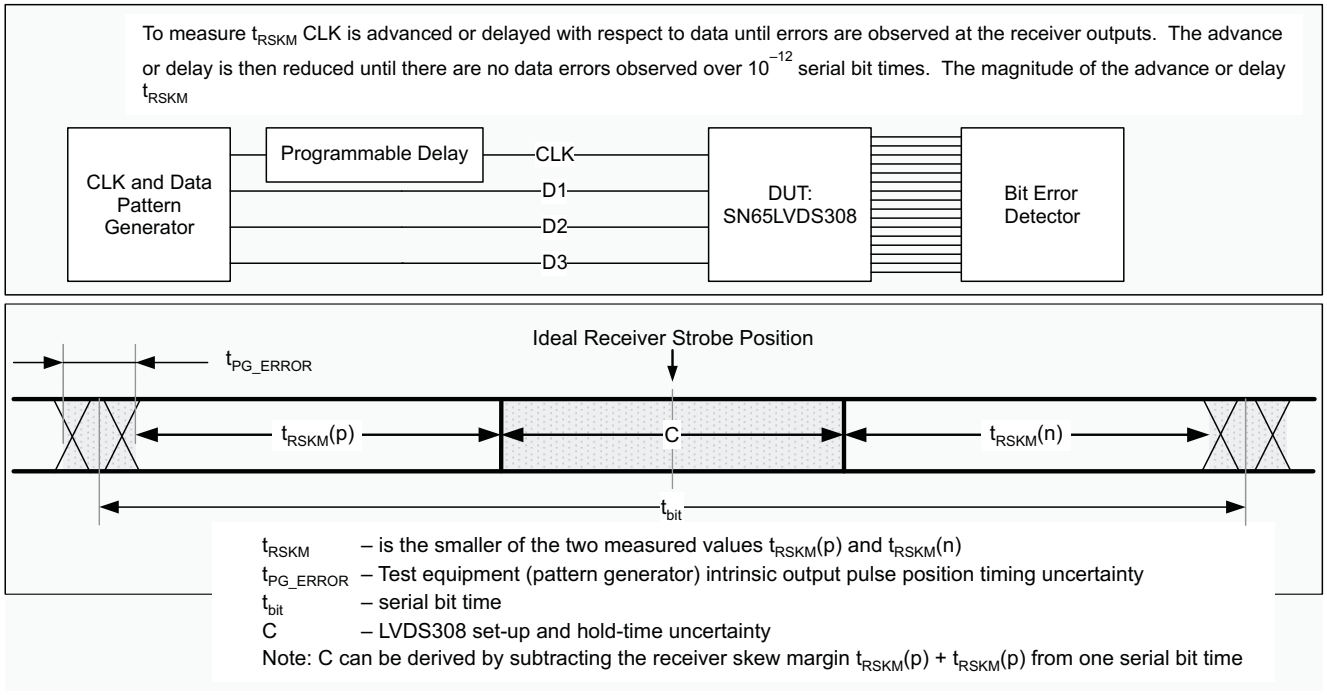


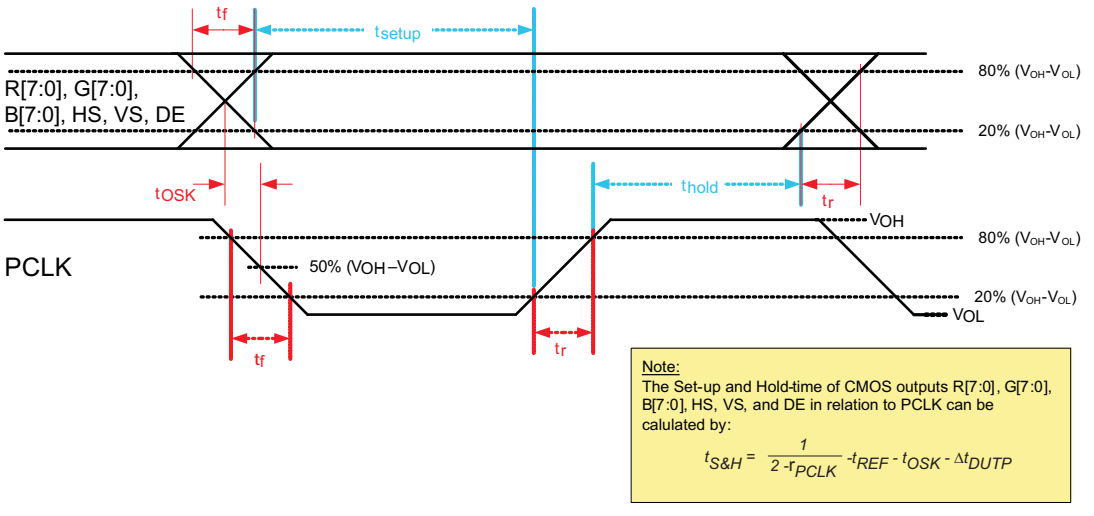

**Figure 5. Power-Supply Noise Test Setup**

## PARAMETER MEASUREMENT INFORMATION (continued)




T0164-03

**Figure 6. Receiver Jitter-Budget Test Setup**




T0256-01

**Figure 7. Output Rise/Fall, Setup/Hold Time**

## PARAMETER MEASUREMENT INFORMATION (continued)

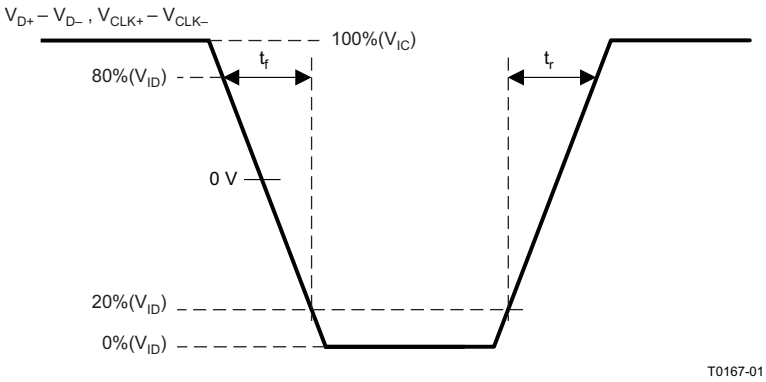



**Figure 8. SubLVDS Differential Input Rise and Fall Time Defintion**

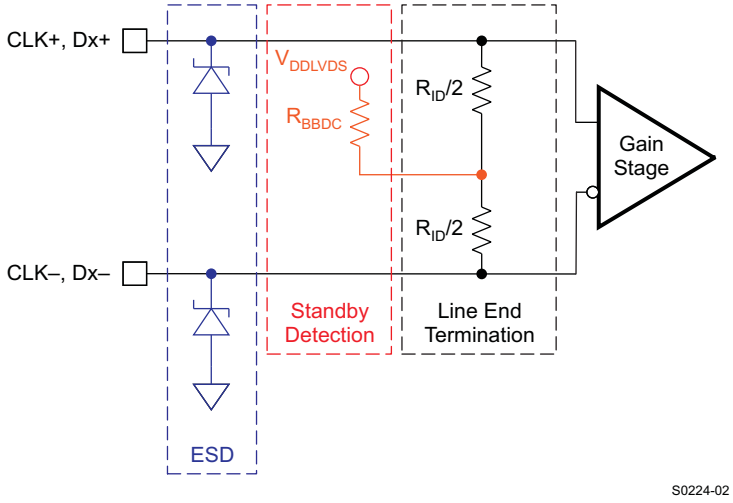



**Figure 9. Equivalent Input Circuit Design**

## PARAMETER MEASUREMENT INFORMATION (continued)

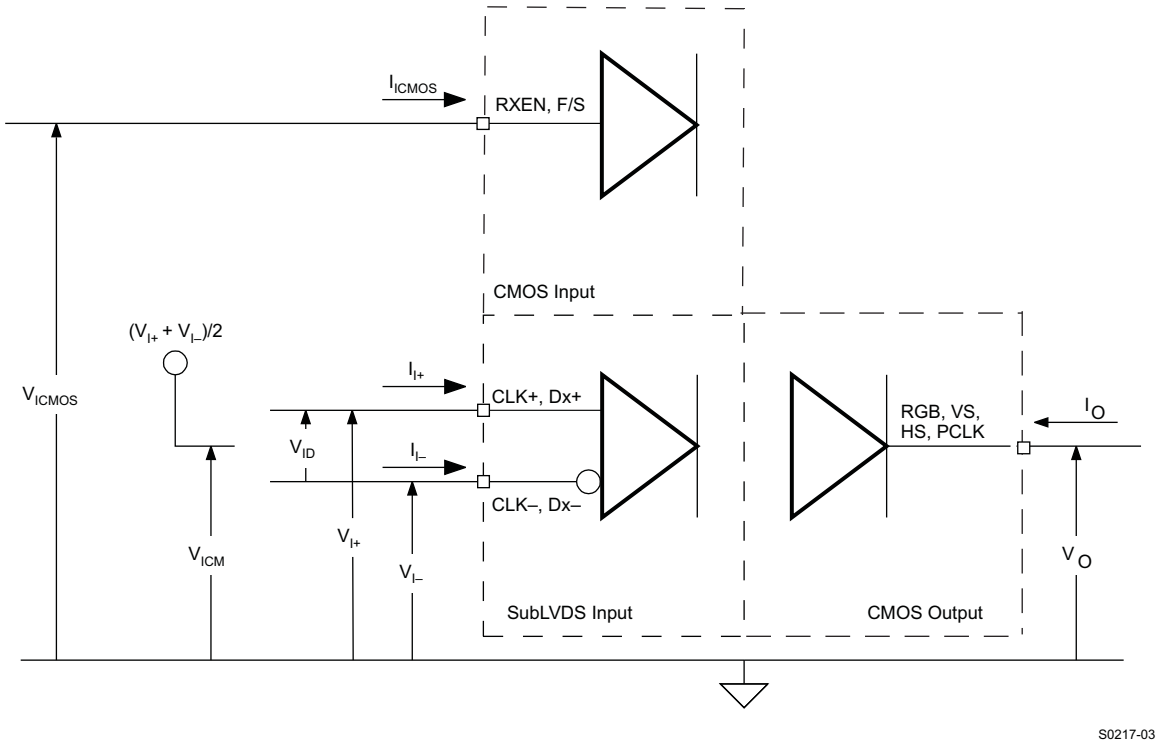



**Figure 10. I/O Voltage and Current Definition**

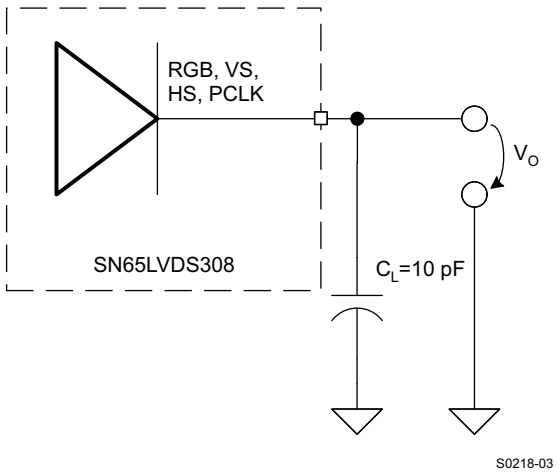



**Figure 11. CMOS Output Test Circuit, Signal, and Timing Definition**

## PARAMETER MEASUREMENT INFORMATION (continued)

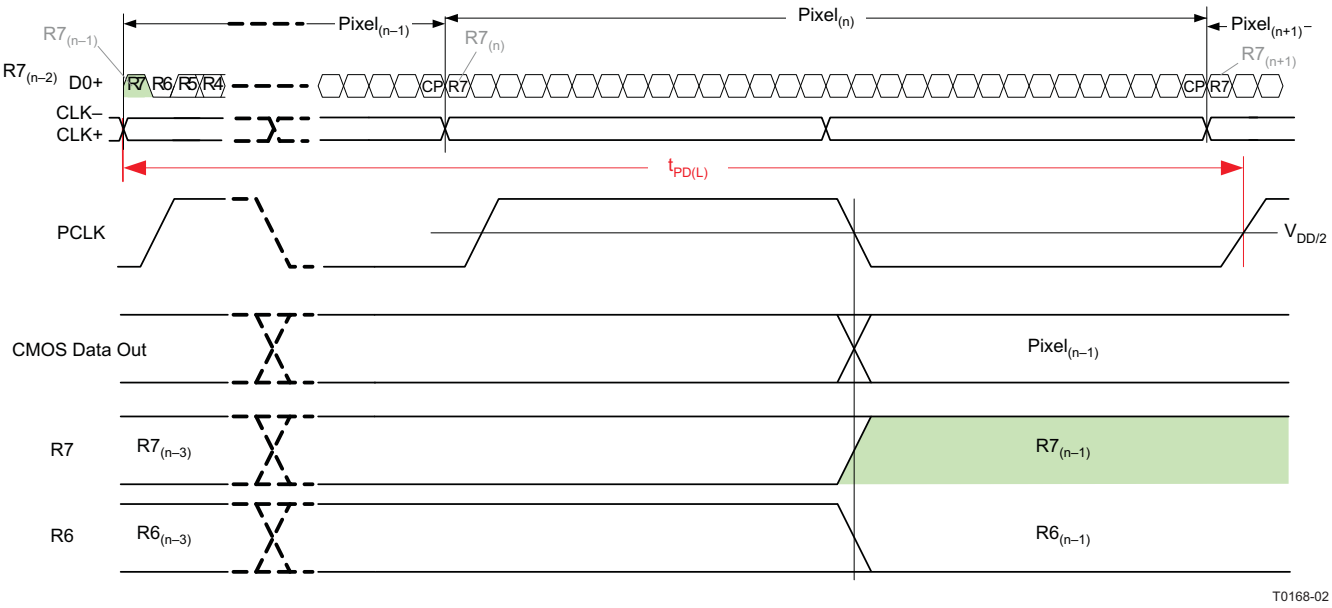



**Figure 12. Propagation Delay, Input to Output**

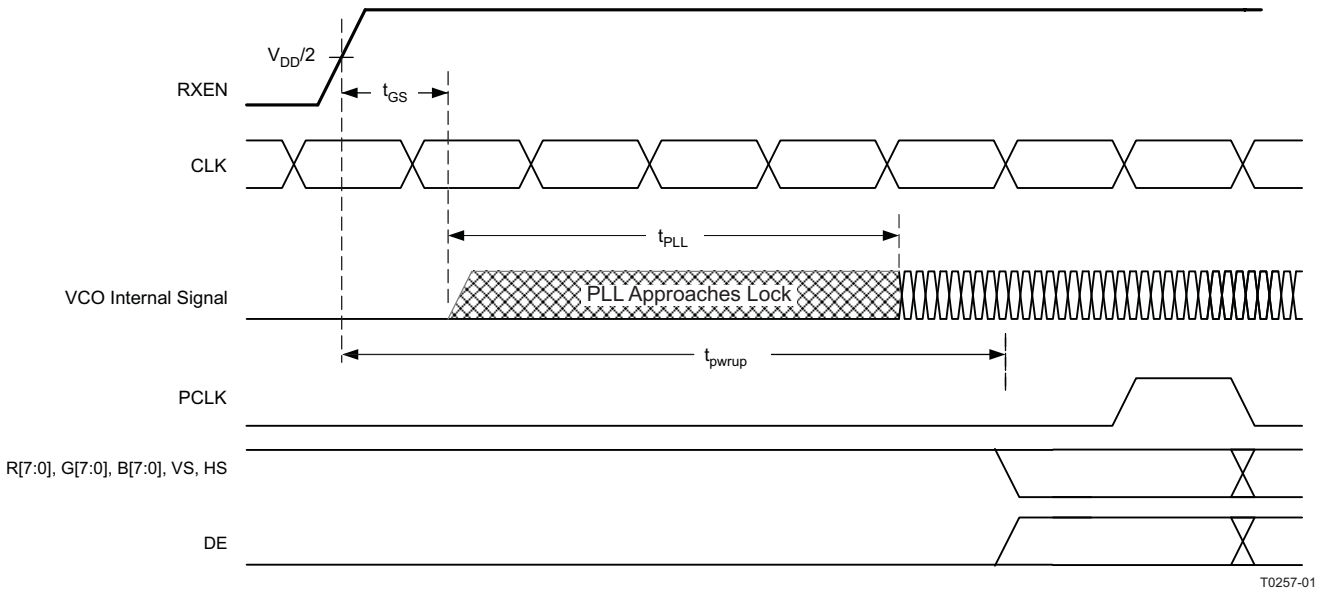



**Figure 13. Receiver Phase-Locked Loop Set TIme and Receiver Enable Time**

## PARAMETER MEASUREMENT INFORMATION (continued)

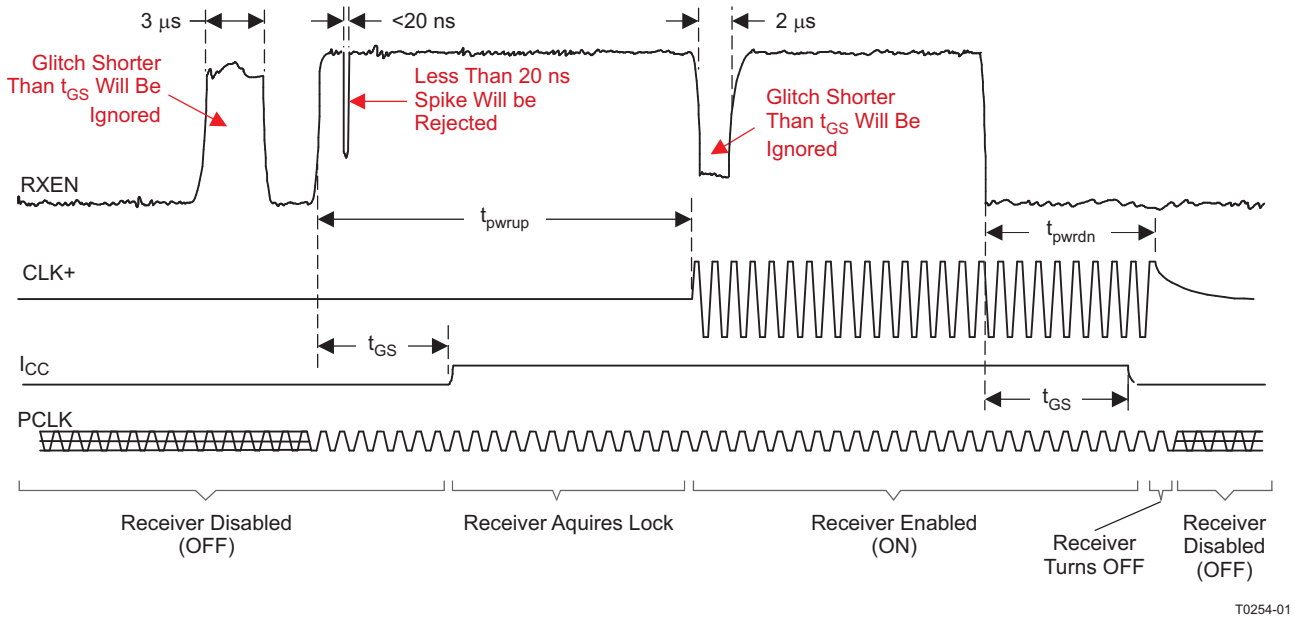



**Figure 14. Receiver Enable/Disable Glitch Suppression Time**

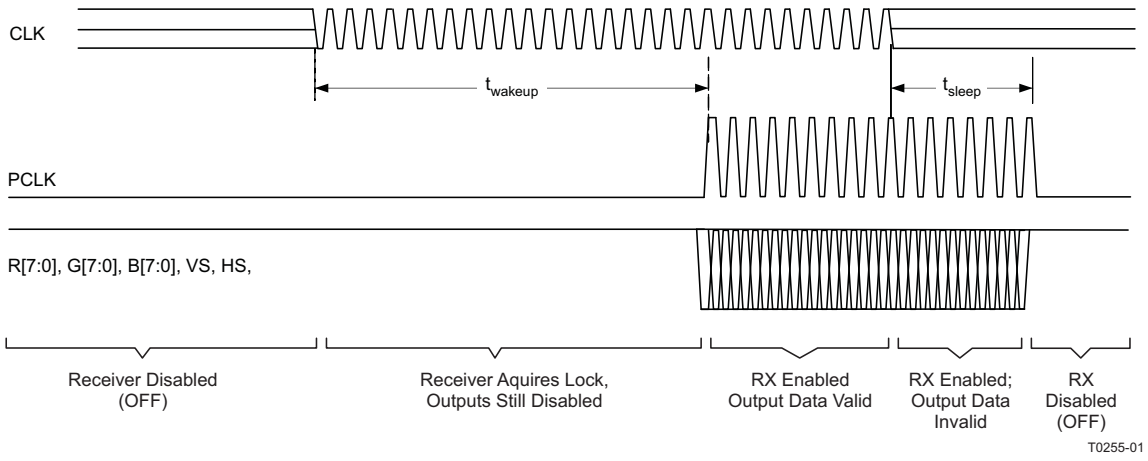



**Figure 15. Standby Detection**

## PARAMETER MEASUREMENT INFORMATION (continued)

### POWER CONSUMPTION TESTS

Table 5 shows an example test pattern word.

**Table 5. Example Test Pattern Word**

| WORD | R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE |
|---|---|
| 1 | 0x7C3E1E7 |

| 7 | | | | C | | | | 3 | | | | E | | | | 1 | | | | E | | | | 7 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 | G7 | G6 | G5 | G4 | G3 | G2 | G1 | G0 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 0 | VS | HS | DE |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |

### TYPICAL IC POWER-CONSUMPTION TEST PATTERN

Typical power-consumption test patterns consist of eight 30-bit transmit words. The pattern repeats itself throughout the entire measurement. It is assumed that every possible transmit code on RGB inputs has the same probability to occur during typical device operation.

**Table 6. Typical IC Power-Consumption Test Pattern**

| WORD | TEST PATTERN:<br>R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE |
|---|---|
| 1 | 0x0000001 |
| 2 | 0x03F03F1 |
| 3 | 0xBFFBFF1 |
| 4 | 0x1D71D71 |
| 5 | 0x4C74C71 |
| 6 | 0xC45C451 |
| 7 | 0xA3aA3A5 |
| 8 | 0x5555553 |

## MAXIMUM POWER-CONSUMPTION TEST PATTERN

The maximum (or worst-case) power consumption of the SN65LVDS308 is tested using the two different test patterns shown in Table 7. Test patterns consist of eight 30-bit transmit words. The pattern repeats itself throughout the entire measurement. It is assumed that every possible transmit code on the RGB inputs has the same probability to occur during typical device operation.

**Table 7. Worst-Case Power-Consumption Test Pattern 1**

| WORD | TEST PATTERN: R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE |
|---|---|
| 1 | 0x0000000 |
| 2 | 0xFFFFFF7 |

**Table 8. Worst-Case Power-Consumption Test Pattern 2**

| WORD | TEST PATTERN: R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE |
|---|---|
| 1 | 0x0000000 |
| 2 | 0xFFFFFF7 |

## OUTPUT SKEW PULSE POSITION and JITTER PERFORMANCE

The following test pattern is used to measure the output skew pulse position and the jitter performance of the SN65LVDS308. The jitter test pattern stresses the interconnect, particularly to test for ISI, using very long run-lengths of consecutive bits, and incorporating very high and low data rates, maximizing switching noise. The pattern is self-repeating for the duration of the test.

**Table 9. Transmit Jitter Test Pattern**

| WORD | TEST PATTERN:<br>R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE |
|---|---|
| 1 | 0x0000001 |
| 2 | 0x000FFF3 |
| 3 | 0x8008001 |
| 4 | 0x0030037 |
| 5 | 0xE00E001 |
| 6 | 0x00FF001 |
| 7 | 0x007E001 |
| 8 | 0x003C001 |
| 9 | 0x0018001 |
| 10 | 0x1C7E381 |
| 11 | 0x3333331 |
| 12 | 0x555AAA5 |
| 13 | 0x6DBDB61 |
| 14 | 0x7777771 |
| 15 | 0x555AAA3 |
| 16 | 0xAAAAAA5 |
| 17 | 0x5555553 |
| 18 | 0xAAA5555 |
| 19 | 0x8888881 |
| 20 | 0x9242491 |
| 21 | 0xAAA5571 |
| 22 | 0xCCCCCC1 |
| 23 | 0xE3E1C71 |
| 24 | 0xFFE7FF1 |
| 25 | 0xFFC3FF1 |
| 26 | 0xFF81FF1 |
| 27 | 0xFE00FF1 |
| 28 | 0x1FF1FF1 |
| 29 | 0xFFCFFC3 |
| 30 | 0x7FF7FF1 |
| 31 | 0xFFF0007 |
| 32 | 0xFFFFFF1 |

## TYPICAL CHARACTERISTIC CURVES

Some of the plots in this section show more than one curve representing various device pin relationships. Taken together, they represent a working range for the tested parameter.

**SUPPLY CURRENT vs TEMPERATURE**

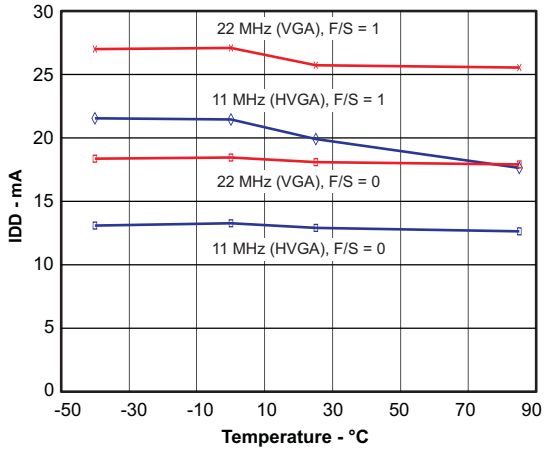



**Figure 16.**

**QUIESCENT SUPPLY CURRENT vs TEMPERATURE**

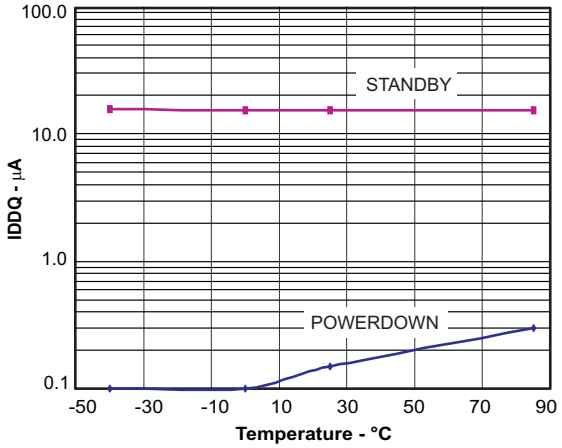



**Figure 17.**

**SUPPLY CURRENT vs FREQUENCY**

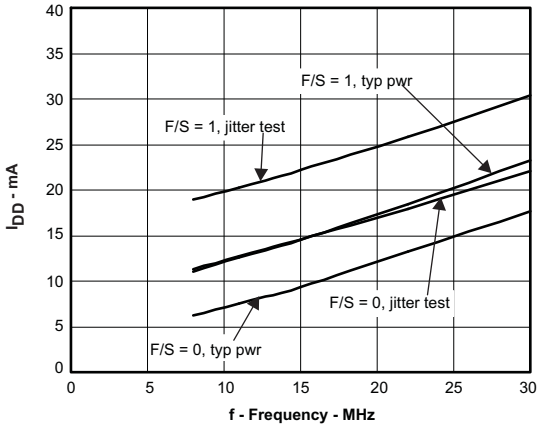



**Figure 18.**

**RECEIVER STROBE POSITION vs TEMPERATURE**

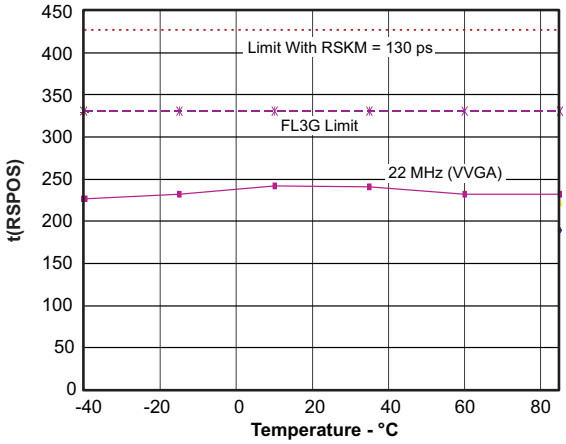



**Figure 19.**

## TYPICAL CHARACTERISTIC CURVES (continued)

### PLL BANDWIDTH

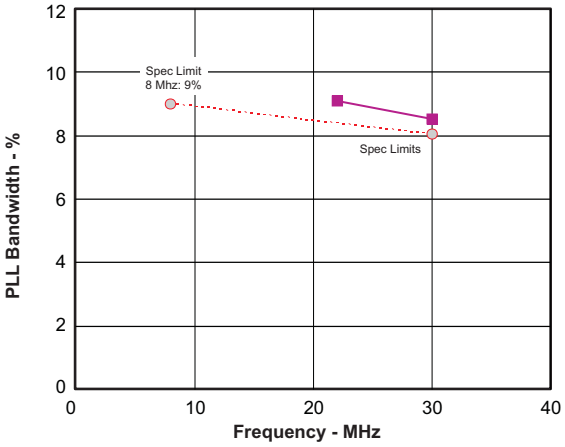



Figure 20.

### PCLK CYCLE-TO-CYCLE OUTPUT JITTER

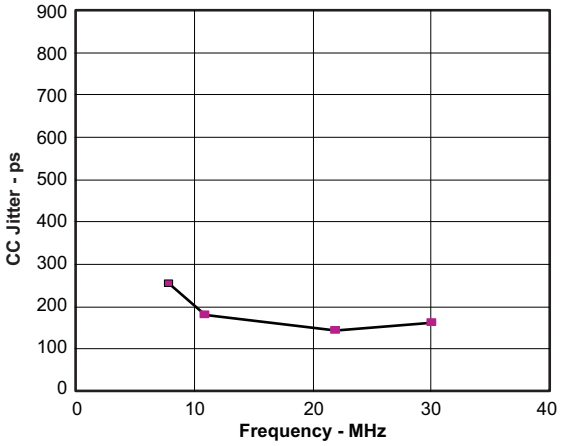



Figure 21.

### RSKM vs BIT RATE

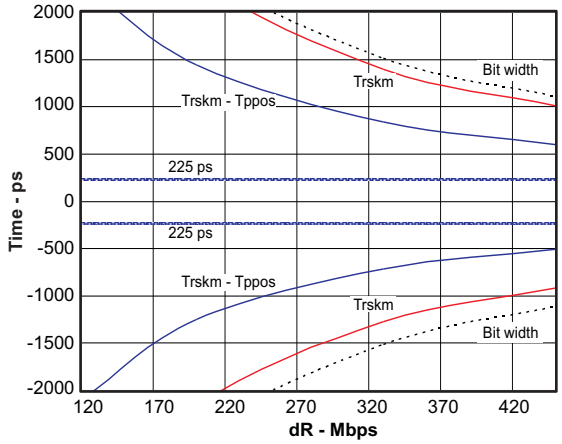



Figure 22.

### VGA OUTPUT WAVEFORM

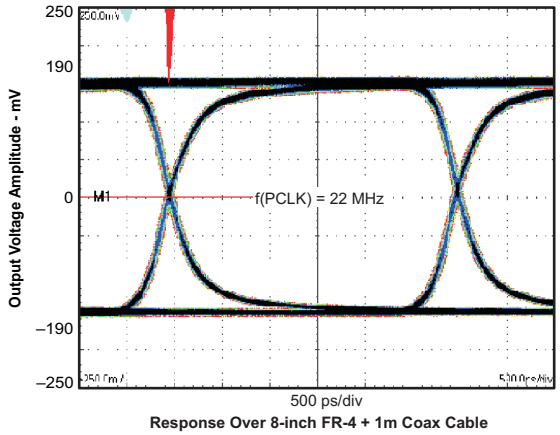



Figure 23.

### VGA OUTPUT WAVEFORM

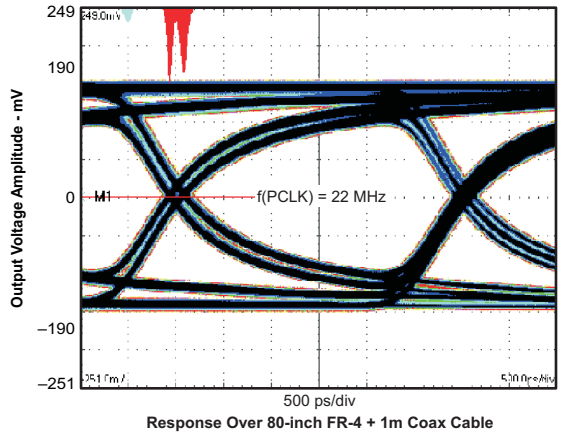



Figure 24.

### INPUT COMMON-MODE NOISE REJECTION vs FREQUENCY

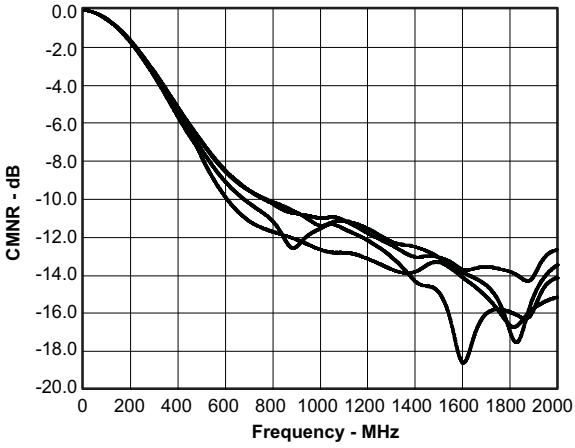



Figure 25.

## TYPICAL CHARACTERISTIC CURVES (continued)

INPUT RETURN LOSS

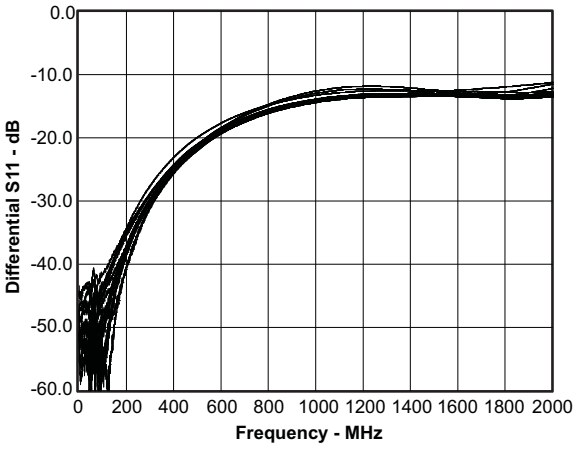



Figure 26.

INPUT DIFFERENTIAL CROSSTALK vs FREQUENCY

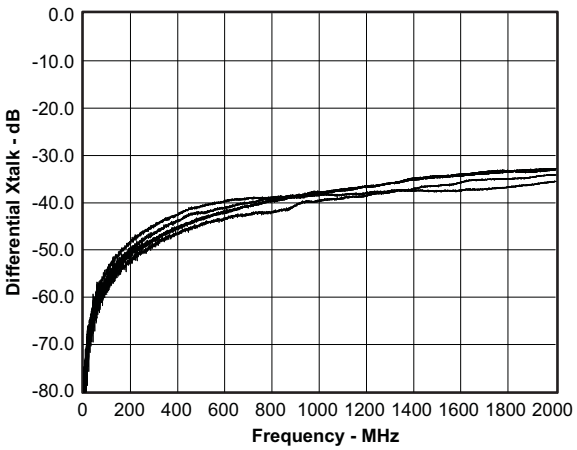



Figure 27.

# APPLICATION INFORMATION

## PREVENTING INCREASED LEAKAGE CURRENTS IN CONTROL INPUTS

A floating (left open) CMOS input allows leakage currents to flow from VDD to GND. Do not leave any CMOS input unconnected or floating. Every input must be connected to a valid logic level, $V_{IH}$ or $V_{IL}$, while power is supplied to VDD. This also minimizes the power consumption of standby and power-down modes.

## POWER-SUPPLY DESIGN RECOMMENDATION

For a multilayer PCB, it is recommended to keep one common GND layer underneath the device and connect all ground terminals directly to this plane.

## SN65LVDS308 DECOUPLING RECOMMENDATION

The SN65LVDS308 was designed to operate reliably in a constricted environment with other digital switching ICs. In cell phone designs, the SN65LVDS308 often shares a power supply with various other ICs. The SN65LVDS308 can operate with power-supply noise as specified in the *Recommended Operating Conditions*. To minimize the power-supply noise floor, provide good decoupling near the SN65LVDS308 power pins. The use of four ceramic capacitors (two 0.01-µF and two 0.1-µF) provides good performance. At the very least, it is recommended to install one 0.1-µF and one 0.01-µF capacitor near the SN65LVDS308. To avoid large current loops and trace inductance, the trace length between the decoupling capacitors and IC power input pins must be minimized. Placing the capacitor underneath the SN65LVDS308 on the bottom of the PCB is often a good choice.

## VGA APPLICATION

Figure 28 shows a possible implementation of a standard 640 × 480 VGA display. The SN65LVDS307 interfaces to the SN65LVDS308, which is the corresponding receiver device, to deserialize the data and drive the display driver. The pixel clock rate of 22 MHz assumes ~10% blanking overhead and 60-Hz display refresh rate. The application assumes 24-bit color resolution. Also shown is how the application processor provides a power-down (reset) signal for both the serializer and the display driver. The signal count over the flexible printed circuit board (FPC) could be further decreased by using the standby detection feature of the SN65LVDS307 and SN65LVDS308 and pulling RXEN high.

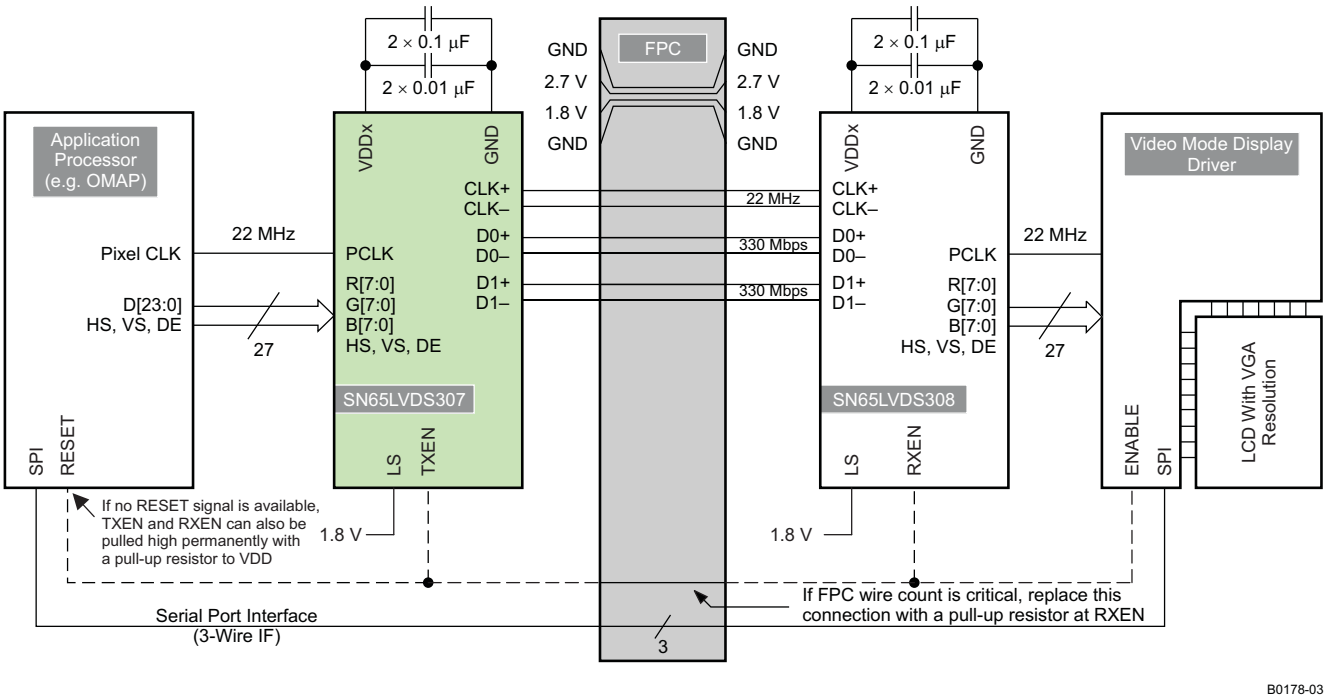



**Figure 28. Typical VGA Display Application**

## APPLICATION INFORMATION (continued)

### TYPICAL APPLICATION FREQUENCIES

The SN65LVDS308 supports pixel clock frequencies from 8 MHz to 30 MHz over two data pairs. Table 10 provides a few typical display resolution examples and shows the number of data pairs necessary to connect the SN65LVDS308 with the display. The blanking overhead is assumed to be 20%. Often, blanking overhead is smaller, resulting in a lower data rate. Furthermore, the examples in the table assumes a display frame refresh rate of 60 Hz. The actual refresh rate may differ, depending on the application-processor clock implementation.

**Table 10. Typical Application Data Rates and Serial Pair Usage**

| Display Screen Resolution | Visible Pixel Count | Blanking Overhead | Display Refresh Rate [Hz] | Pixel Clock Frequency [MHz] | Data Rate on D0 and D1 [Mbps] |
|---|---|---|---|---|---|
| 240 × 320 (QVGA) | 76,800 | 20% | 90 | 8.3 | 124 |
| 640 × 200 | 128,000 | | 60 | 9.2 | 138 |
| 352 × 416 (CIF+) | 146,432 | | | 10.5 | 158 |
| 352 × 440 | 154,880 | | | 11.2 | 167 |
| 320 × 480 (HVGA) | 153,600 | | | 11.1 | 166 |
| 800 × 250 | 200,000 | | | 14.4 | 216 |
| 640 x 320 | 204,800 | | | 14.7 | 221 |
| 640 × 480 (VGA) | 307,200 | | 30 | 11.1 | 166 |
| 640 × 480 (VGA) | 307,200 | | 60 | 22.1 | 332 |
| 1024 × 320 | 327,680 | | | 23.6 | 354 |
| 854 × 480 (WVGA) | 409,920 | | | 29.5 | 443 |
| 800 × 600 (SVGA) | 480,000 | | 30 | 17.3 | 259 |
| 1024 × 768 (XGA) | 786,432 | | | 28.3 | 425 |

## CALCULATION EXAMPLE: HVGA DISPLAY

The following calculation shows an example for a half-VGA display with the following parameters:

| | |
|---|---|
| Display resolution: | 480 × 320 |
| Frame refresh rate: | 58.4 Hz |
| Vertical visible pixels: | 320 lines |
| Vertical front porch: | 10 lines |
| Vertical sync: | 5 lines |
| Vertical back porch: | 3 lines |
| Horizontal visible pixels: | 480 columns |
| Horizontal front porch: | 20 columns |
| Horizontal sync: | 5 columns |
| Horizontal back porch: | 3 columns |

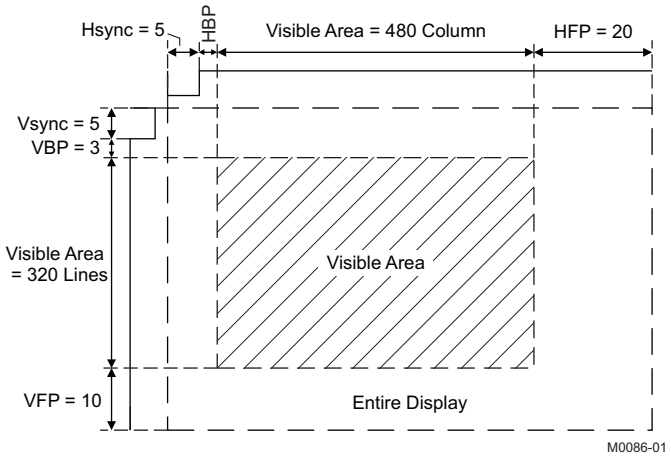



**Figure 29. HVGA Display**

*Calculation of the total number of pixels and blanking overhead:*

| | |
|---|---|
| Visible area pixel count: | 480 × 320 = 153,600 pixels |
| Total frame pixel count: | (320 + 10 + 5 + 3) × (480 + 20 + 5 + 3) = 171,704 pixels |
| Blanking overhead: | (171,704 – 153,600) ÷ 153,600 ≈ 11.8% |

*The application requires the following serial-link parameters:*

| | |
|---|---|
| Pixel clock frequency: | 171,704 × 58.4 Hz = 10 MHz |
| Serial data rate: | 10 MHz × 15 bits/channel = 150 Mbps |

## HOW TO DETERMINE INTERCONNECT SKEW AND JITTER BUDGET

Designing a reliable data link requires examining the interconnect skew and jitter budget. The sum of all transmitter, PCB, connector, FPC, and receiver uncertainties must be smaller than the available serial bit time. The highest pixel clock frequency defines the available serial bit time. The transmitter timing uncertainty is defined by $t_{PPOS}$ in the transmitter data sheet. For a bit-error-rate target of $\leq 10^{-12}$, the measurement duration for $t_{PPOS}$ is $\geq 10^{12}$. The SN65LVDS308 receiver can tolerate a maximum timing uncertainty defined by $t_{RSKM}$. The interconnect budget is calculated by:

$$t_{interconnect} = t_{RSKM} - t_{PPOS}$$

**Example:**

$f_{PCLK}$(max) = 23 MHz (VGA display resolution, 60 Hz)

Transmission mode: 2-ChM; $t_{PPOS}$(SN65LVDS307) = 330 ps

Target bit error rate: $10^{-12}$

$t_{RSKM}$(SN65LVDS308) = $1/(2 \times 15 \times f_{PCLK}) - 480$ ps = 969 ps

The interconnect budget for cable skew and ISI must be smaller than:

$$t_{interconnect} = t_{RSKM} - t_{PPOS} = 639 \text{ ps}$$

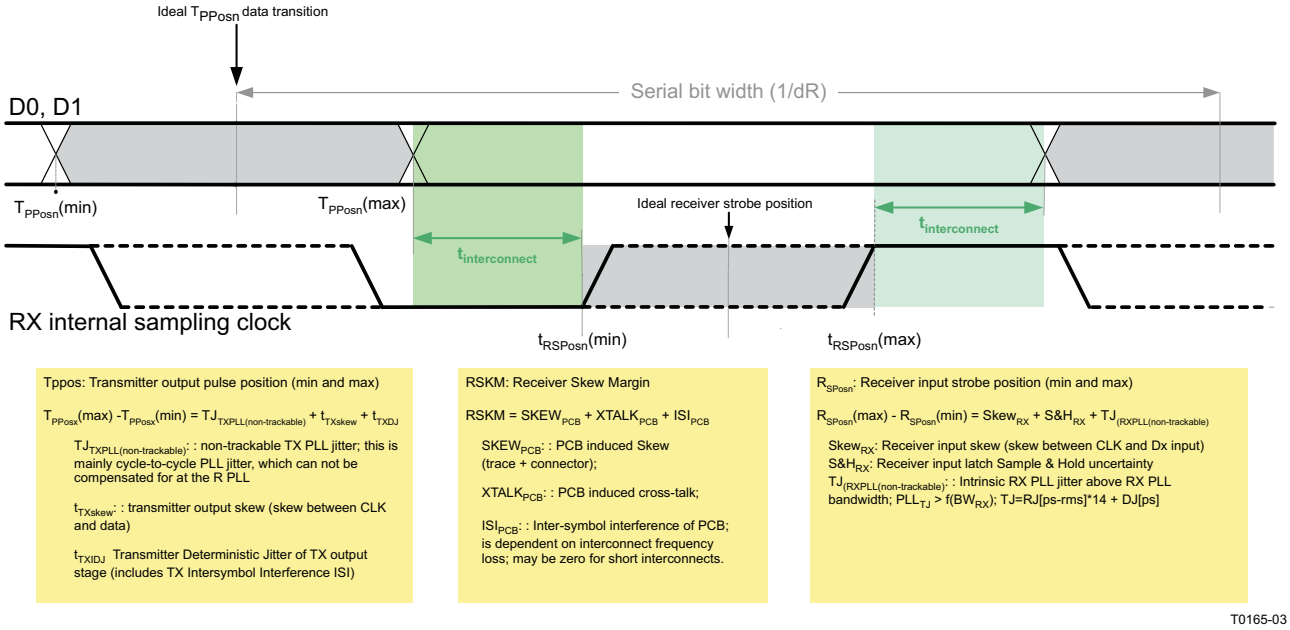



**Figure 30. Jitter Budget**

## F/S-PIN SETTING AND CONNECTING THE SN65LVDS308 TO AN LCD DRIVER

**NOTE:**

**Receiver PLL tracking:** To maximize the design margin for the interconnect, good RX PLL tracking of the TX PLL is important. FlatLink3G requires the RX PLL to have a bandwidth higher than the bandwidth of the TX PLL. The SN65LVDS308 PLL design is optimized to track the SN65LVDS307 PLL particularly well, thus providing a very large receiver skew margin. A FlatLink3G-compliant link must provide at least ±225 ppm of receiver skew margin for the interconnect.

It is important to understand the tradeoff between power consumption, EMI, and maximum speed when selecting the F/S signal. It is beneficial to choose the slowest rise time possible to minimize EMI and power consumption. Unfortunately, a slower rise time also reduces the timing margin left for the LCD driver. Hence, it is necessary to calculate the timing margin to select the correct F/S pin setting.

The output rise time depends on the output driver strength and the output load. An LCD driver typical capacitive load is assumed with ~10 pF. The higher the capacitive load, the slower is the rise time. Rise time of the SN65LVDS308 is measured as the time duration it takes the output voltage to rise from 20% of VDD to 80% of VDD, and fall time is defined as the time for the output voltage to transition from 80% of VDD down to 20% of VDD.

The rise time of the output stage is fixed and does not adjust to the pixel frequency. Only setting F/S changes the output rise time. Due to the short bit time at very fast pixel clock speeds and the real capacitive load of the display driver, the output amplitude might not reach VDD and GND saturation fully. To ensure sufficient signal swing and verify the design margin, it becomes necessary to determine that the output amplitude under any circumstance reaches the display driver's input stage logic threshold (usually 30% and 70% of VDD).

Figure 31 shows a worst-case rise time simulation assuming an LCD driver load of 16 pF at VGA display resolution. PCLK is the fastest-switching output. With F/S set to GND (Figure 31-b), the PCLK output voltage amplitude is significantly reduced. The voltage amplitude of the output data RGB[7:0], VS, HS, and DE shows less amplitude attenuation because these outputs carry random data patterns and toggle at half of the PCLK frequency or less. It is necessary to determine the timing margin between the SN65LVDS308 output and LCD driver input.

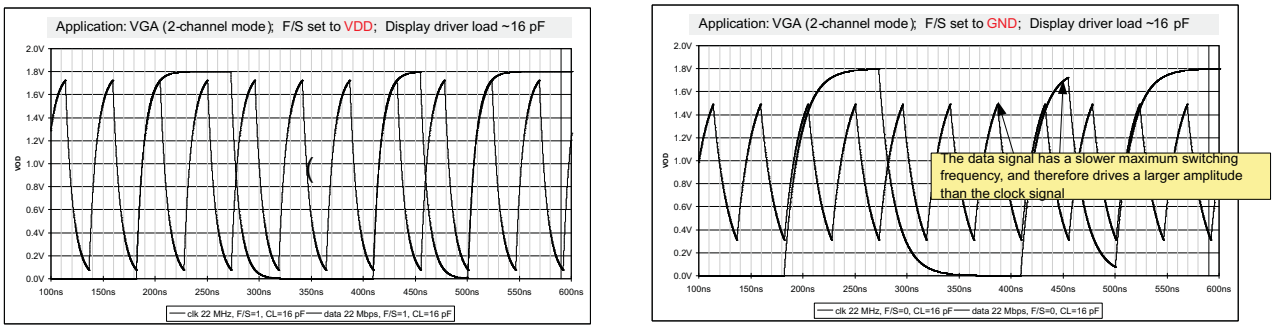



**Figure 31. Output Amplitude as a Function of Output Toggling Frequency, Capacitive Load, and F/S Setting**

## HOW TO DETERMINE THE LCD DRIVER TIMING MARGIN

To determine the timing margin, it is necessary to specify the frequency of operation, identify the setup and hold times of the LCD driver, and specify the output load of the SN65LVDS308 as a combination of the LCD driver input parasitics plus any capacitance caused by the connecting PCB trace. Furthermore, the setting of pin F/S and the SN65LVDS308 output skew impact the margin. The total remaining design margin calculates as follows:

$$t_{DM} = \frac{1}{2 \times f_{PCLK}} - t_{DUTP(max\_error)} - \frac{t_{rise(max)} \times C_{LOAD}}{10\ pF} - \left|t_{OSK}\right| \quad (3)$$

where:

$t_{DM}$ – Design margin
$f_{PCLK}$ – Pixel clock frequency
$t_{DUTP(max\_error)}$ – maximum duty cycle error
$t_{rise(max)}$ – maximum rise or fall time; see $t_{r/f}$ under switching characteristics
$C_{LOAD}$ – parasitic capacitance (sum of LCD driver input parasitics + connecting PCB trace)
$t_{skew}$ – clock to data output skew of the SN65LVDS308

### Example:

At a pixel clock frequency of 11 MHz (HVGA), and an assumed LCD driver load of 15 pF, the remaining timing margin is:

$$t_{DUTP(max\_error)} = \frac{\left|t_{DUTP}(max) - 50\right|}{100\%} \times t_{PCLK} = \frac{5\%}{100\%} \times \frac{1}{11\ MHz} = 4.5\ ns$$

$$t_{DM} = \frac{1}{2 \times 11\ MHz} - 4.5ns - \frac{16ns_{(F/S = GND)} \times 15pF}{10\ pF} - 500\ ps = 16\ ns$$

As long as the setup and hold times of the LCD driver are each less than 16 ns, the timing budget is met sufficiently.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65LVDS308ZQCR | ACTIVE | BGA MICROSTAR JUNIOR | ZQC | 48 | 2500 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 85 | LVDS308 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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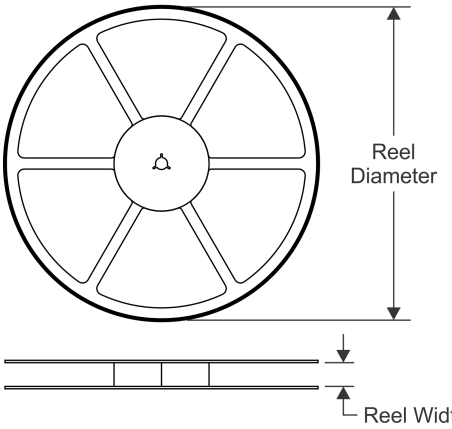
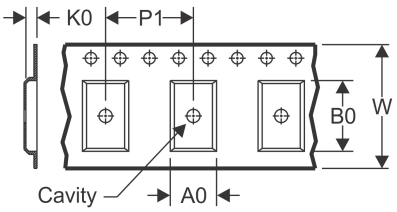
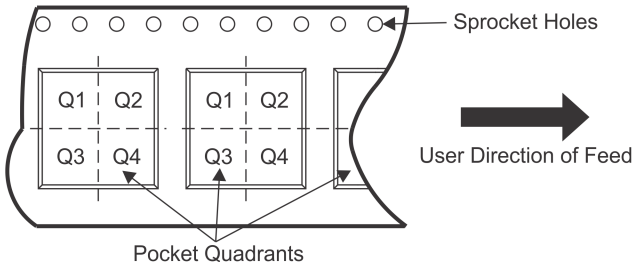



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

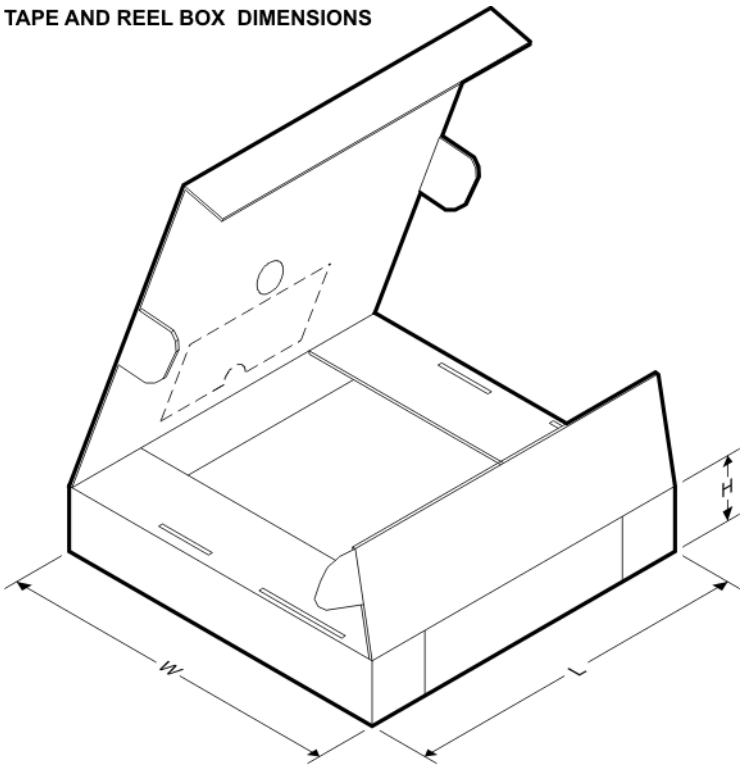
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65LVDS308ZQCR | BGA MICROSTAR JUNIOR | ZQC | 48 | 2500 | 330.0 | 12.4 | 4.3 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |

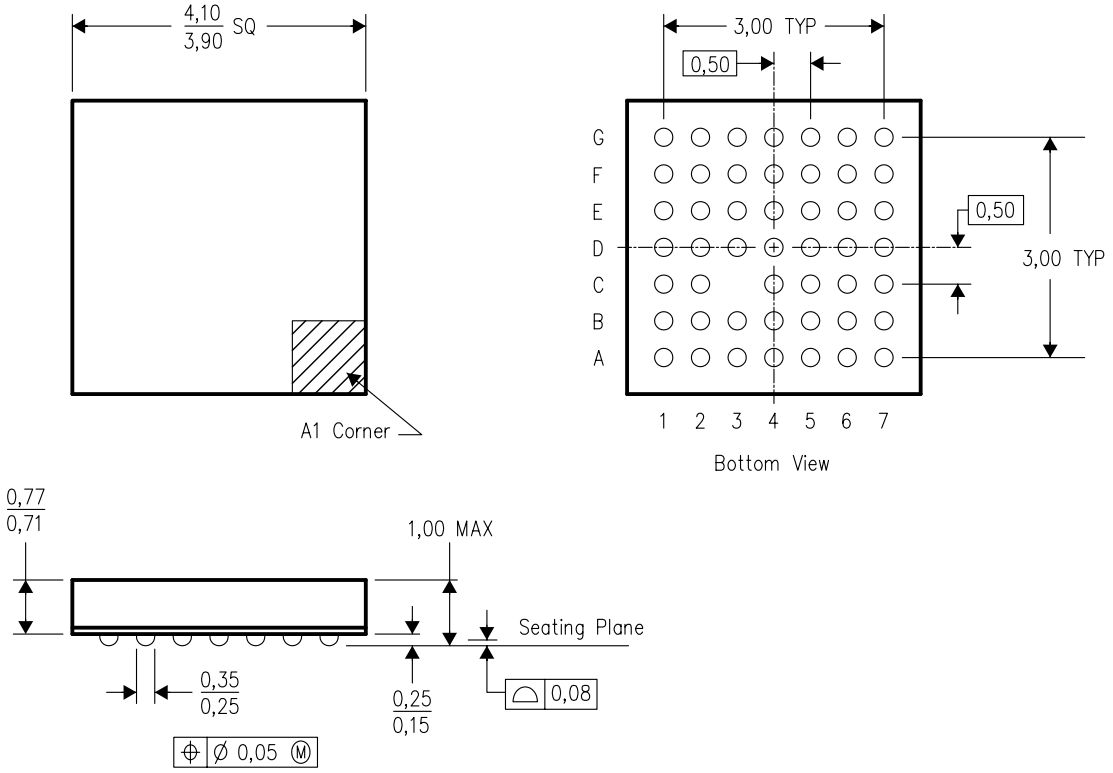
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN65LVDS308ZQCR | BGA MICROSTAR JUNIOR | ZQC | 48 | 2500 | 336.6 | 336.6 | 28.6 |

## ZQC (S–PBGA–N48) PLASTIC BALL GRID ARRAY




4204659/A 09/02

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration
D. Falls within JEDEC MO–225
E. This package is lead–free.

MicroStar Junior is a trademark of Texas Instruments.

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