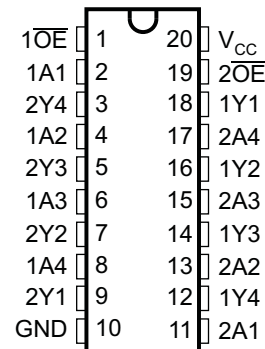


FEATURES

- **Controlled Baseline**
– One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree ⁽¹⁾**
- **State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Typical V_{OLP} (Output Ground Bounce) <1 V at $V_{CC} = 5 V, T_A = 25^\circ C$**
- **High-Drive Outputs (–24-mA I_{OH} , 48-mA I_{OL})**
- **Packaged in Shrink Small-Outline (DB) Package**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

DB PACKAGE
(TOP VIEW)



DESCRIPTION

This octal buffer and line driver is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the SN54ABT240, SN74ABT240A, SN54ABT241, and SN74ABT241A, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable (\overline{OE}) inputs, and complementary OE and \overline{OE} inputs.

The SN74ABT244A is organized as two 4-bit buffers/line drivers with separate \overline{OE} inputs. When \overline{OE} is low, the device passes noninverted data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT244 is characterized for operation over the full military temperature range of –55°C to 125°C.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SSOP – DB	Tape and reel	SN74ABT244AMDBREP	ABT244AMEP

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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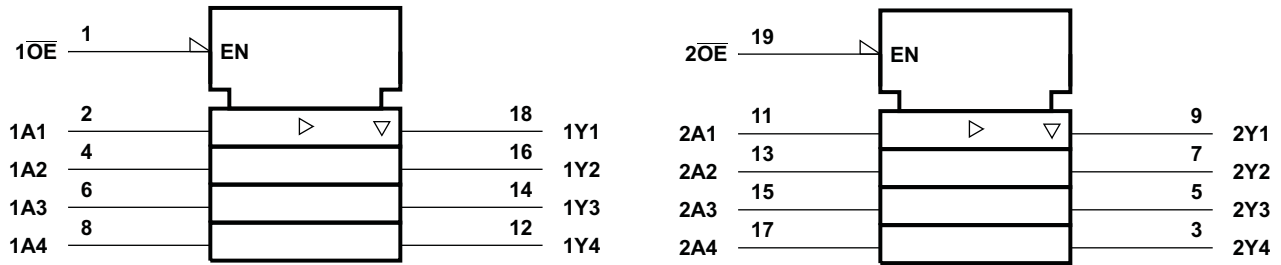
SN74ABT244A-EP OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SGBS312A—JULY 2006—REVISED JULY 2006

**FUNCTION TABLE
(EACH BUFFER)**

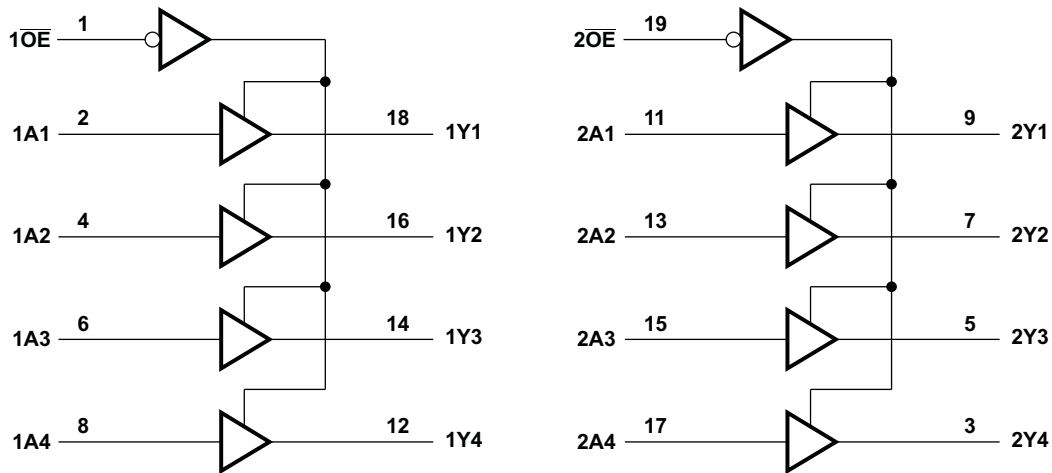
INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

LOGIC SYMBOL⁽¹⁾



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	–0.5	7	V
V _I	Input voltage range ⁽²⁾	–0.5	7	V
V _O	Voltage range applied to any output in the high or power-off state	–0.5	5.5	V
I _O	Current into any output in the low state		96	mA
I _{IK}	Input clamp current	V _I < 0	–18	mA
I _{OK}	Output clamp current	V _O < 0	–50	mA
θ _{JA}	Package thermal impedance ⁽³⁾		115	°C/W
T _{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	4.5	5.5	V
V _{IH}	High-level input voltage	2		V
V _{IL}	Low-level input voltage		0.8	V
V _I	Input voltage	0	V _{CC}	V
I _{OH}	High-level output current		–24	mA
I _{OL}	Low-level output current		48	mA
Δt/Δv	Input transition rise or fall rate		5	ns/V
	Outputs enabled			
T _A	Operating free-air temperature	–55	125	°C

- (1) Unused inputs must be held high or low to prevent them from floating.

SN74ABT244A-EP

OCTAL BUFFER/DRIVER

WITH 3-STATE OUTPUTS

SGBS312A—JULY 2006—REVISED JULY 2006

Electrical Characteristics⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP ⁽²⁾	MAX			
V _{IK}	V _{CC} = 4.5 V,	I _I = -18 mA	-1.2				-1.2	V
V _{OH}	V _{CC} = 4.5 V,	I _{OH} = -3 mA	2.5			2.5		V
	V _{CC} = 5 V,	I _{OH} = -3 mA	3			3		
	V _{CC} = 4.5 V,	I _{OH} = -24 mA	2			2		
V _{OL}	V _{CC} = 4.5 V,	I _{OL} = 48 mA	0.55			0.55		V
V _{hys}			100					mV
I _I	V _{CC} = 5.5 V,	V _I = V _{CC} or GND	±1			±1		μA
I _{OZH}	V _{CC} = 5.5 V,	V _O = 2.7 V	10			10		μA
I _{OZL}	V _{CC} = 5.5 V,	V _O = 0.5 V	-10			-10		μA
I _{off}	V _{CC} = 0,	V _I or V _O ≤ 5.5 V	±100					μA
I _{CEX}	V _{CC} = 5.5 V,	Outputs high	50			50		μA
I _O ⁽³⁾	V _{CC} = 5.5 V,	V _O = 2.5 V	-50	-100	-180	-50	-180	mA
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND		Outputs high		1	250	250	μA
			Outputs low		24	30	30	mA
			Outputs disabled		0.5	250	250	μA
ΔI _{CC} ⁽⁴⁾	Data inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	Outputs enabled		1.5	1.5	mA	
			Outputs disabled		0.05	0.05		
	Control inputs				1.5	1.5		
C _i	V _I = 2.5 V or 0.5 V		3.5				pF	
C _o	V _O = 2.5 V or 0.5 V		7.5				pF	

(1) On products compliant to MIL-PRF-38535, this parameter does not apply.

(2) All typical values are at V_{CC} = 5 V.

(3) Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

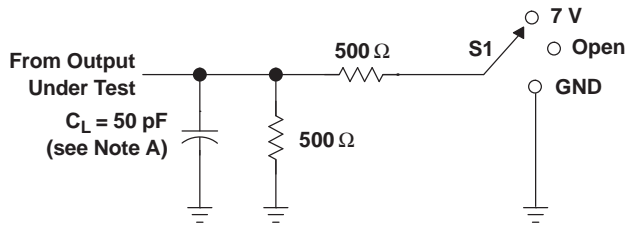
Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted)

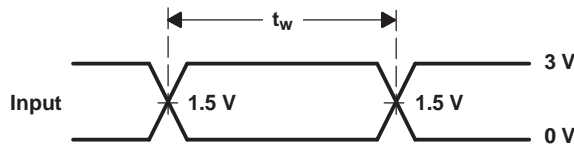
(see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	A	Y	1	2.6	4.1	1	5.3	ns
t _{PHL}			1	2.9	4.2	1	5	
t _{PZH}	\overline{OE}	Y	1.1	3.1	4.6	0.8	5.7	ns
t _{PZL}			2.1	4.1	5.6	1.2	7.9	
t _{PHZ}	\overline{OE}	Y	2.1	4.1	5.6	1.2	7.6	ns
t _{PLZ}			1.5	3.7	5.6	1	7.9	

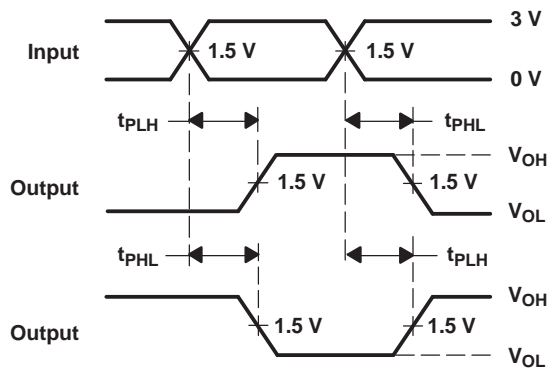
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

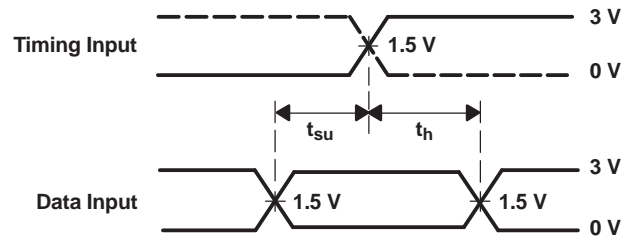


VOLTAGE WAVEFORMS
PULSE DURATION

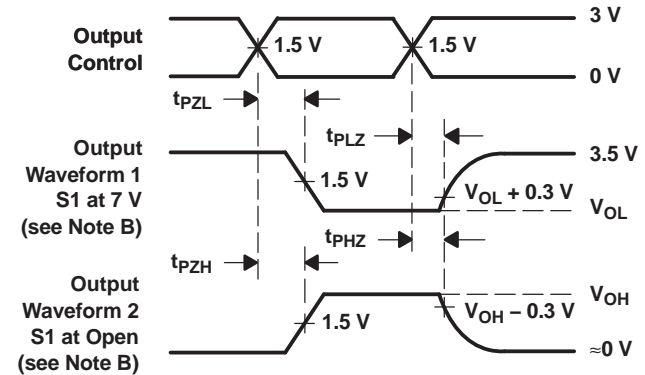


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74ABT244AMDBREP	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/06667-01XE	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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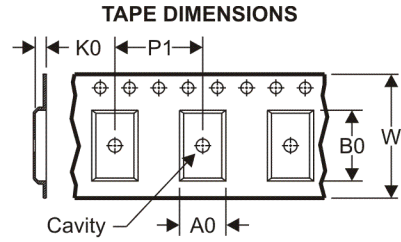
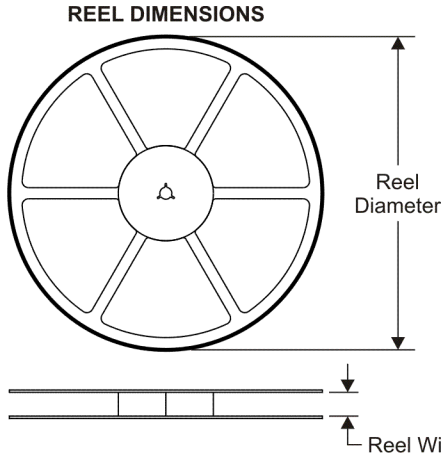
OTHER QUALIFIED VERSIONS OF SN74ABT244A-EP :

- Catalog: [SN74ABT244A](#)

NOTE: Qualified Version Definitions:

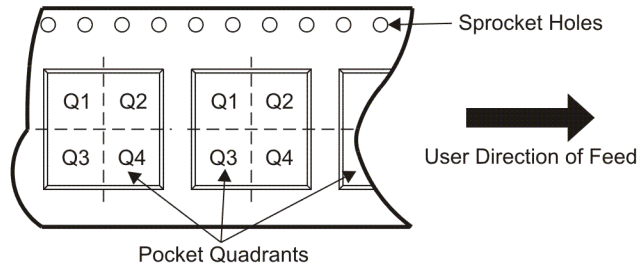
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT244AMDBREP	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT244AMDBREP	SSOP	DB	20	2000	346.0	346.0	33.0

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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