# SN74AC74-EP
# DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

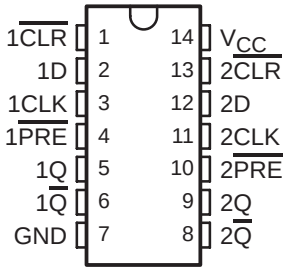
SCAS721 − OCTOBER 2003

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of −55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- **2-V to 6-V $V_{CC}$ Operation**
- **Inputs Accept Voltages to 6 V**
- **Max $t_{pd}$ of 10 ns at 5 V**

**D PACKAGE**
**(TOP VIEW)**




## description/ordering information

The SN74AC74 is a dual positive-edge-triggered D-type flip-flop.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) input sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at D can be changed without affecting the levels at the outputs.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE‡ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −55°C to 125°C | SOIC − D | Tape and reel | SN74AC74MDREP | SAC74MEP |

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{PRE}$ | $\overline{CLR}$ | CLK | D | Q | $\overline{Q}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H§ | H§ |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | $Q_0$ | $\overline{Q}_0$ |

§ This configuration is nonstable; that is, it does not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

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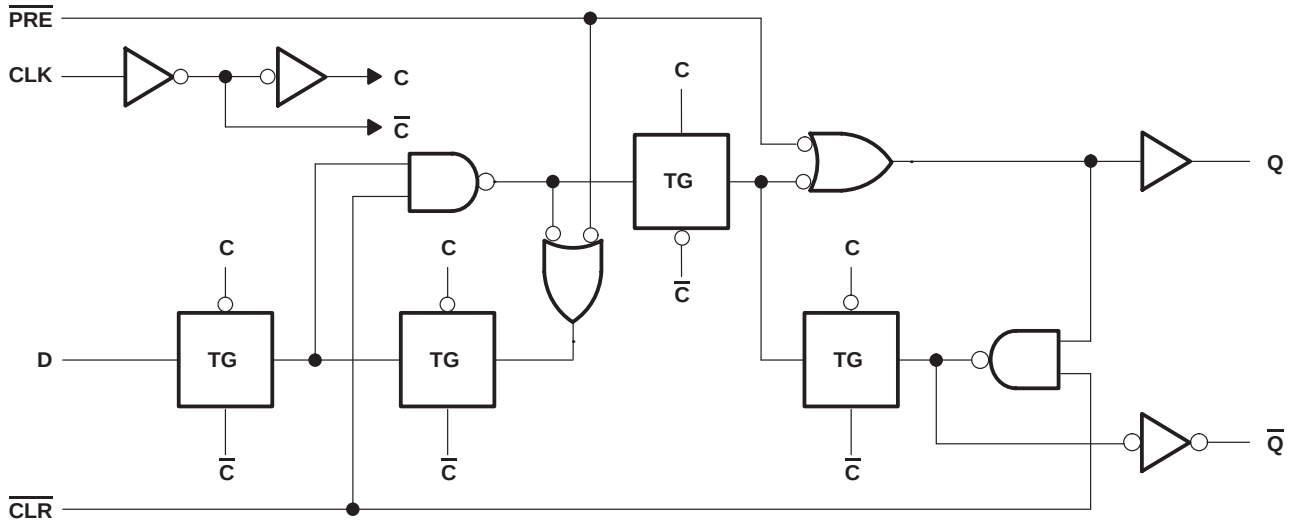
### logic diagram, each flip-flop (positive logic)




### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | −0.5 V to 7 V |
| Input voltage range, $V_I$ (see Note 1) | −0.5 V to $V_{CC}$ + 0.5 V |
| Output voltage range, $V_O$ (see Note 1) | −0.5 V to $V_{CC}$ + 0.5 V |
| Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{CC}$) | ±20 mA |
| Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) | ±20 mA |
| Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) | ±50 mA |
| Continuous current through $V_{CC}$ or GND | ±200 mA |
| Package thermal impedance, $\theta_{JA}$ (see Note 2) | 86°C/W |
| Storage temperature range, $T_{stg}$ | −65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 3 V | 2.1 | | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 3 V | | 0.9 | V |
| | | $V_{CC}$ = 4.5 V | | 1.35 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 3 V | | −12 | mA |
| | | $V_{CC}$ = 4.5 V | | −24 | |
| | | $V_{CC}$ = 5.5 V | | −24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 3 V | | 12 | mA |
| | | $V_{CC}$ = 4.5 V | | 24 | |
| | | $V_{CC}$ = 5.5 V | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 8 | ns/V |
| $T_A$ | Operating free-air temperature | | −55 | 125 | °C |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | | |
| $V_{OH}$ | | $I_{OH}$ = −50 µA | 3 V | 2.9 | 4.49 | | 2.9 | | V |
| | | | 4.5 V | 4.4 | 5.49 | | 4.4 | | |
| | | | 5.5 V | 5.4 | 5.49 | | 5.4 | | |
| | | $I_{OH}$ = −12 mA | 3 V | 2.56 | | | 2.4 | | |
| | | $I_{OH}$ = −24 mA | 4.5 V | 3.86 | | | 3.7 | | |
| | | | 5.5 V | 4.86 | | | 4.7 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 µA | 3 V | | 0.002 | 0.1 | | 0.1 | V |
| | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | |
| | | | 5.5 V | | 0.001 | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 12 mA | 3 V | | | 0.36 | | 0.5 | |
| | | $I_{OL}$ = 24 mA | 4.5 V | | | 0.36 | | 0.5 | |
| | | | 5.5 V | | | 0.36 | | 0.5 | |
| $I_I$ | Data pins | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | µA |
| | Control pins | | | | | ±0.1 | | ±1 | |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 40 | µA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | 5 V | | 3 | | | | pF |

### timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| | | | $T_A$ = 25°C | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | | | |
| $f_{clock}$ | Clock frequency | | | 100 | | 70 | MHz |
| $t_w$ | Pulse duration | $\overline{PRE}$ or $\overline{CLR}$ low | 5.5 | | 8 | | ns |
| | | CLK | 5.5 | | 8 | | |
| $t_{su}$ | Setup time, data before CLK↑ | Data | 4 | | 5 | | ns |
| | | $\overline{PRE}$ or $\overline{CLR}$ inactive | 0 | | 0.5 | | |
| $t_h$ | Hold time, data after CLK↑ | | 0.5 | | 0.5 | | ns |

### timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | | $T_A$ = 25°C | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | | | |
| $f_{clock}$ | Clock frequency | | | 140 | | 95 | MHz |
| $t_w$ | Pulse duration | $\overline{PRE}$ or $\overline{CLR}$ low | 4.5 | | 5.5 | | ns |
| | | CLK | 4.5 | | 5.5 | | |
| $t_{su}$ | Setup time, data before CLK↑ | Data | 3 | | 4 | | ns |
| | | $\overline{PRE}$ or $\overline{CLR}$ inactive | 0 | | 0.5 | | |
| $t_h$ | Hold time, data after CLK↑ | | 0.5 | | 0.5 | | ns |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | 100 | 125 | | 70 | | MHz |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | 3.5 | 8 | 12 | 1 | 13 | ns |
| $t_{PHL}$ | | | 4 | 10.5 | 12 | 1 | 14 | |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | 4.5 | 8 | 13.5 | 1 | 17.5 | ns |
| $t_{PHL}$ | | | 3.5 | 8 | 14 | 1 | 13.5 | |

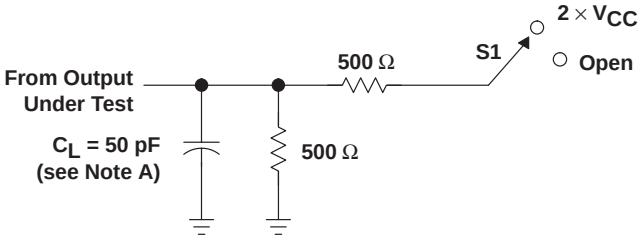
### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $f_{max}$ | | | 140 | 160 | | 95 | | MHz |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | 2.5 | 6 | 9 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | 3 | 8 | 9.5 | 1 | 10.5 | |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | 3.5 | 6 | 10 | 1 | 12 | ns |
| $t_{PHL}$ | | | 2.5 | 6 | 10 | 1 | 10 | |

### operating characteristics, $V_{CC}$ = 3.3 V, $T_A$ = 25°C

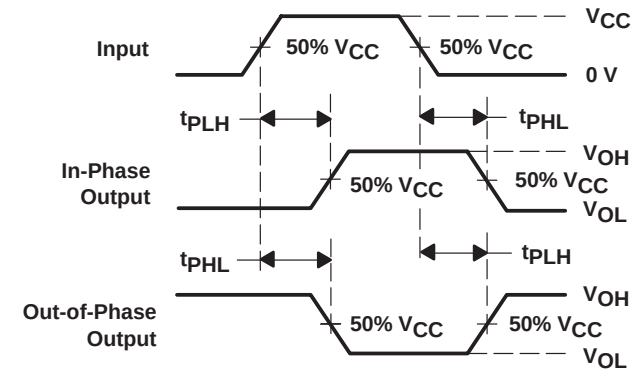
| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF, | f = 1 MHz | 45 | pF |

## PARAMETER MEASUREMENT INFORMATION

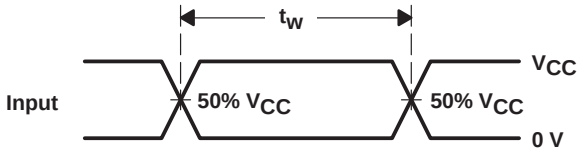



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |

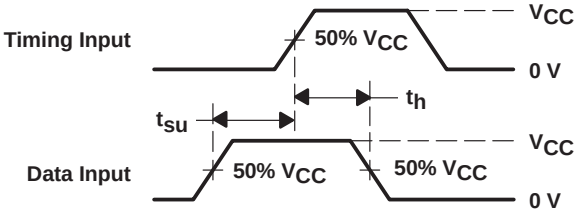
LOAD CIRCUIT




VOLTAGE WAVEFORMS




VOLTAGE WAVEFORMS




VOLTAGE WAVEFORMS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AC74MDREP | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | SAC74MEP | Samples |
| V62/04617-01XE | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | SAC74MEP | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**OTHER QUALIFIED VERSIONS OF SN74AC74-EP :**

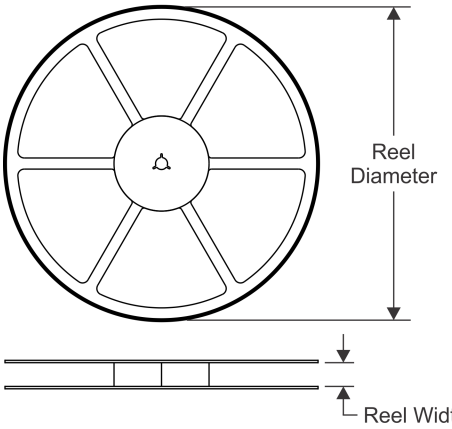
- Catalog: SN74AC74
- Military: SN54AC74

NOTE: Qualified Version Definitions:

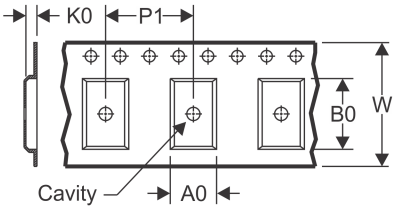
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

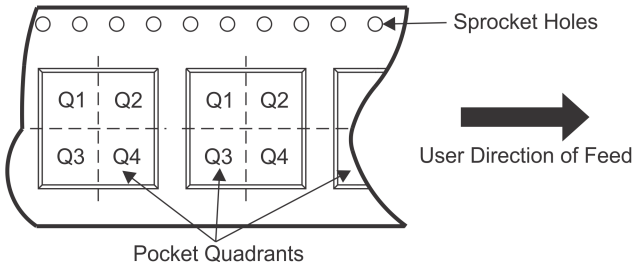



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

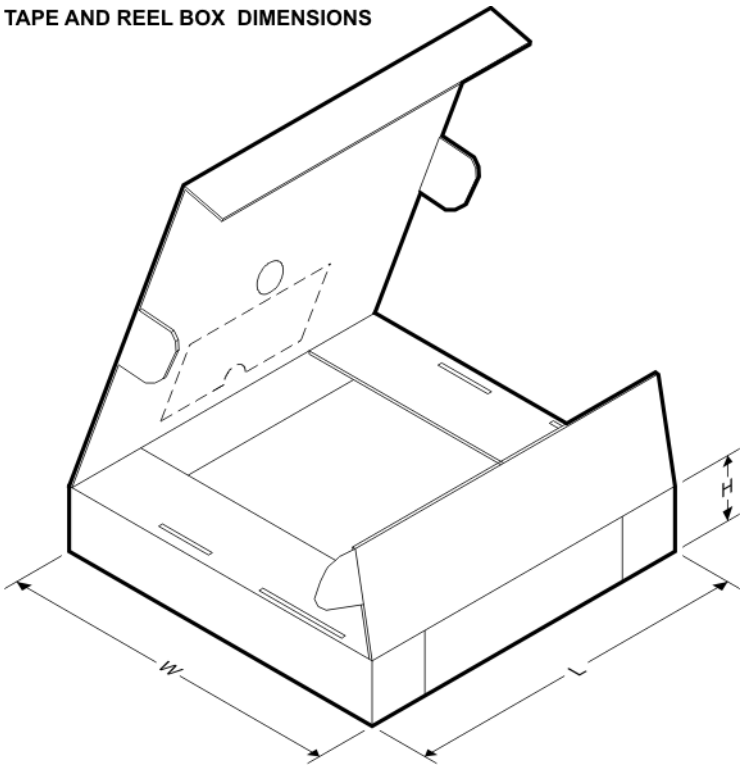
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AC74MDREP | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AC74MDREP | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |

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