SN74AHC4066 Quadruple Bilateral Analog Switch

1 Features

- 1V to 5.5V V_{CC} operation
- Supports mixed-mode voltage operation on all ports
- High on-off output-voltage ratio
- Low crosstalk between switches
- Individual switch controls
- Extremely low input current
- ESD protection exceeds JESD 22:
  - 2000V Human-Body Model (A114-A)
  - 200V Machine Model (A115-A)
  - 1000V Charged-Device Model (C101)

2 Applications

- Analog signal switching or multiplexing:
  - Signal gating, modulator, squelch control, demodulator, chopper, commutating switch
- Digital signal switching and multiplexing
  - Audio and video signal routing
- Transmission-gate logic implementation
- Analog-to-digital and digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain
- Motor speed control
- Battery chargers
- DC-DC converter

3 Description

This quadruple silicon-gate CMOS analog switch is designed for 1V to 5.5V VCC operation.

The switch is designed to handle both analog and digital signals. Each switch permits signals with amplitudes of up to 5.5V (peak) to be transmitted in either direction.

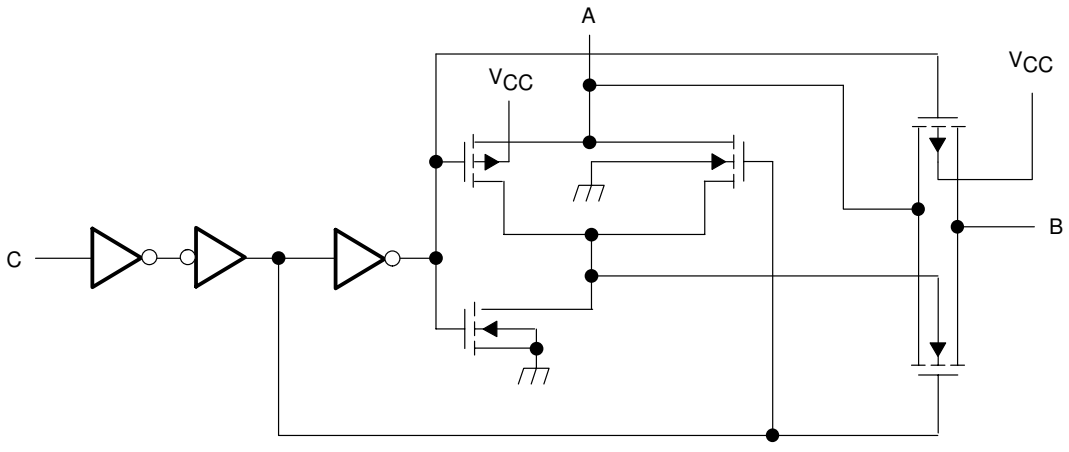
Each switch section has its own enable input control (C). A high-level voltage applied to C turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN74AHC4066	D (SOIC, 14)	8.65mm × 6mm
	PW (TSSOP, 14)	5mm × 6.4mm
	RGY (VQFN, 14)	3.5mm × 3.5mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram, Each Switch (Positive Logic)

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4 Pin Configuration and Functions

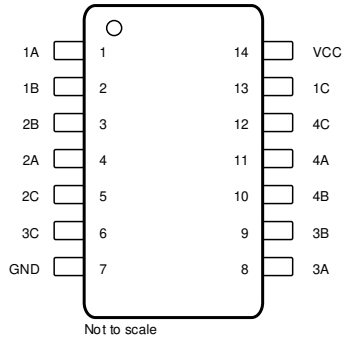


Figure 4-1. D or PW Package, 14-Pin SOIC or TSSOP (Top View)

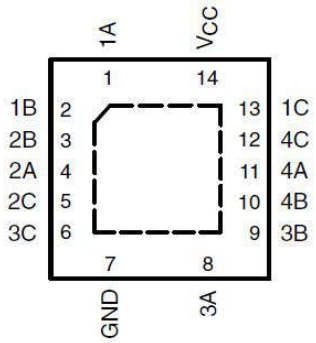


Figure 4-2. RGY Package, 14-Pin QFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1A	1	I/O	Switch 1 input/output
1B	2	I/O	Switch 1 output/input
2B	3	I/O	Switch 2 output/input
2A	4	I/O	Switch 2 input/output
2C	5	I	Switch 2 control
3C	6	I	Switch 3 control
GND	7	—	Ground
3A	8	I/O	Switch 3 input/output
3B	9	I/O	Switch 3 output/input
4B	10	I/O	Switch 4 output/input
4A	11	I/O	Switch 4 input/output
4C	12	I	Switch 4 control
1C	13	I	Switch 1 control
V_{CC}	14	—	Power

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.5	7	V
V_I	Input voltage range		–0.5	7	V
V_{IO}	Switch I/O voltage range		–0.5 to V_{CC}	+0.5	V
I_{IK}	Control-input clamp current	$V_I < 0$		-20	mA
I_I	I/O port diode current	$V_I < 0$ or $V_{I/O} > V_{CC}$		±50	mA
	On-state switch current	$V_{I/O}$ = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature		–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground unless otherwise specified.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. CDM value for N package only.

5.3 Thermal Information

THERMAL METRIC(1)		SN74AHC4066			UNIT
		D	PW	RGY	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	127.7	150.6	91.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	81.8	78.2	91.8	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	50.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	84.2	93.7	66.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	39.5	24.6	20.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	83.7	93.1	66.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1 (1)	5.5	V
V_{IH}	High-level input voltage, control inputs	V_{CC} = 2V	1.5		V
		V_{CC} = 2.3V to 2.7V	V_{CC} × 0.7		
		V_{CC} = 3V to 3.6V	V_{CC} × 0.7		
		V_{CC} = 4.5V to 5.5V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage, control inputs	V_{CC} = 2V		0.5	V
		V_{CC} = 2.3V to 2.7V		V_{CC} × 0.3	
		V_{CC} = 3V to 3.6V		V_{CC} × 0.3	
		V_{CC} = 4.5V to 5.5V		V_{CC} × 0.3	
V_I	Control input voltage		0	5.5	V
$V_{I/O}$	Input/output voltage		0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise and fall time	V_{CC} = 2.3V to 2.7V		200	ns/V
		V_{CC} = 3V to 3.6V		100	
		V_{CC} = 4.5V to 5.5V		20	
T_A	Operating free-air temperature		–40	85	°C

(1) With supply voltages at or below 2V, the analog switch on-state resistance becomes very nonlinear. Only digital signals should be transmitted at these low supply voltages.
(2) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*.

5.5 Electrical Characteristics

T_A = –40 to +85 °C unless otherwise specified.

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
r_{on}	On-state switch resistance	I_T = –1mA, V_I = 0 to V_{CC}, V_C = V_{IH} (see Figure 6-1)	2.3V		38	180		225	Ω
			3V		29	150		190	
			4.5V		21	75		100	
$r_{on(p)}$	Peak on-state resistance	I_T = –1mA, V_I = V_{CC} to GND, V_C = V_{IH}	2.3V		143	500		600	Ω
			3V		57	180		225	
			4.5V		31	100		125	
Δr_{on}	Difference in on-state resistance between switches	I_T = –1mA, V_I = V_{CC} to GND, V_C = V_{IH}	2.3V		6	30		40	Ω
			3V		3	20		30	
			4.5V		2	15		20	
I_{IH} I_{IL}	Control input current	V_C = 0 or V_{CC}	5.5			±0.1		±1	µA
$I_{s(off)}$	Off-state switch leakage current	V_I = V_{CC} and V_O = GND, or V_I = GND and V_O = V_{CC}, V_C = V_{IL} (see Figure 6-2)	5.5V			±0.1		±1	µA

5.5 Electrical Characteristics (continued)

T_A = –40 to +85 °C unless otherwise specified.

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
$I_{s(on)}$	On-state switch leakage current	V_I = V_{CC} or GND, V_C = V_{IH} (see Figure 6-3)	5.5V			±0.1		±1	µA
I_{CC}	Supply current	V_I = V_{CC} or GND	5.5V					20	µA
C_{iC}	Control input capacitance				1.5				pF
C_{iO}	Switch input/output capacitance				5.5				pF
C_F	Feed-through capacitance				0.5				pF

5.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 2.5V ± 0.2V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			MIN	MAX	UNIT
					MIN	TYP	MAX			
t_{PLH}, t_{PHL}	Propagation delay time	A or B	B or A	C_L = 50pF (see Figure 6-4)		1.2	10		16	ns
t_{PZH}, t_{PZL}	Switch turn-on time	C	A or B	C_L = 50pF R_L = 1kΩ, (see Figure 6-5)		3.3	15		20	ns
t_{PLZ}, t_{PHZ}	Switch turn-off time	C	A or B	C_L = 50pF R_L = 1kΩ, (see Figure 6-5)		6	15		23	ns
t_{PLZ}, t_{PHZ}	Propagation delay time	A or B	B or A	C_L = 50pF (see Figure 6-6)		2.6	12		18	ns
t_{PLZ}, t_{PHZ}	Switch turn-on time	C	A or B	C_L = 50pF R_L = 1kΩ, (see Figure 6-8)		4.2	25		32	ns
t_{PLZ}, t_{PHZ}	Switch turn-off time	C	A or B	C_L = 50pF R_L = 1kΩ, (see Figure 6-8)		9.6	25		32	ns

5.7 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 3.3V ± 0.3V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			MIN	MAX	UNIT
					MIN	TYP	MAX			
t_{PLH}, t_{PHL}	Propagation delay time	A or B	B or A	C_L = 50pF (see Figure 6-4)		0.8	6		10	ns
t_{PZH}, t_{PZL}	Switch turn-on time	C	A or B	C_L = 50pF R_L = 1kΩ, (see Figure 6-5)		2.3	11		15	ns
t_{PLZ}, t_{PHZ}	Switch turn-off time	C	A or B	C_L = 50pF R_L = 1kΩ, (see Figure 6-5)		4.5	11		15	ns
t_{PLZ}, t_{PHZ}	Propagation delay time	A or B	B or A	C_L = 50pF (see Figure 6-6)		1.5	9		12	ns
t_{PLZ}, t_{PHZ}	Switch turn-on time	C	A or B	C_L = 50pF R_L = 1kΩ, (see Figure 6-8)		3	18		22	ns

5.7 Switching Characteristics (continued)

over recommended operating free-air temperature range, V_{CC} = 3.3V ± 0.3V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLZ}, t_{PHZ} Switch turn-off time	C	A or B	C_L = 50pF, R_L = 1kΩ, (see Figure 6-8)		7.2	18		22	ns

5.8 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5V ± 0.5V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}, t_{PHL} Propagation delay time	A or B	B or A	C_L = 50pF (see Figure 6-4)		0.3	4		7	ns
t_{PZH}, t_{PZL} Switch turn-on time	C	A or B	C_L = 50pF, R_L = 1kΩ, (see Figure 6-5)		1.6	7		10	ns
t_{PLZ}, t_{PHZ} Switch turn-off time	C	A or B	C_L = 50pF, R_L = 1kΩ, (see Figure 6-5)		3.2	7		10	ns
t_{PLZ}, t_{PHZ} Propagation delay time	A or B	B or A	C_L = 50pF (see Figure 6-6)		0.6	6		8	ns
t_{PLZ}, t_{PHZ} Switch turn-on time	C	A or B	C_L = 50pF, R_L = 1kΩ, (see Figure 6-8)		2.1	12		16	ns
t_{PLZ}, t_{PHZ} Switch turn-off time	C	A or B	C_L = 50pF, R_L = 1kΩ, (see Figure 6-8)		5.1	12		16	ns

5.9 Analog Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	T_A = 25°C			UNIT
					MIN	TYP	MAX	
Frequency response (switch on)	A or B	B or A	C_L = 50pF, R_L = 600Ω, f_{in} = 1MHz (sine wave), $20\log_{10}(V_O/V_I)$ = -3 dB (see Figure 6-4)	2.3V		60		MHz
				3V		75		
				4.5V		100		
Crosstalk (between any switches)	A or B	B or A	C_L = 50pF, R_L = 600Ω, f_{in} = 1MHz (sine wave) (see Figure 6-4)	2.3V		-45		dB
				3V		-45		
				4.5V		-45		
Crosstalk (control input to signal output)	C	A or B	C_L = 50pF, R_L = 600Ω, f_{in} = 1MHz (sine wave) (see Figure 6-4)	2.3V		15		mV
				3V		20		
				4.5V		50		
Feed-through attenuation (switch off)	A or B	B or A	C_L = 50pF, R_L = 600Ω, f_{in} = 1MHz (sine wave) (see Figure 6-4)	2.3V		-40		dB
				3V		-40		
				4.5V		-40		

5.9 Analog Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		V_{CC}	T_A = 25°C			UNIT
						MIN	TYP	MAX	
Sine-wave distortion	A or B	B or A	C_L = 50pF, R_L = 10kΩ, f_{in} = 1kHz (sine wave) (see Figure 6-4)	V_I = $2V_{p-p}$	2.3V		0.1		%
				V_I = $2.5V_{p-p}$	3V		0.1		
				V_I = $4V_{p-p}$	4.5V		0.1		

5.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50pF,	f = 10MHz	4.5	pF

6 Parameter Measurement Information

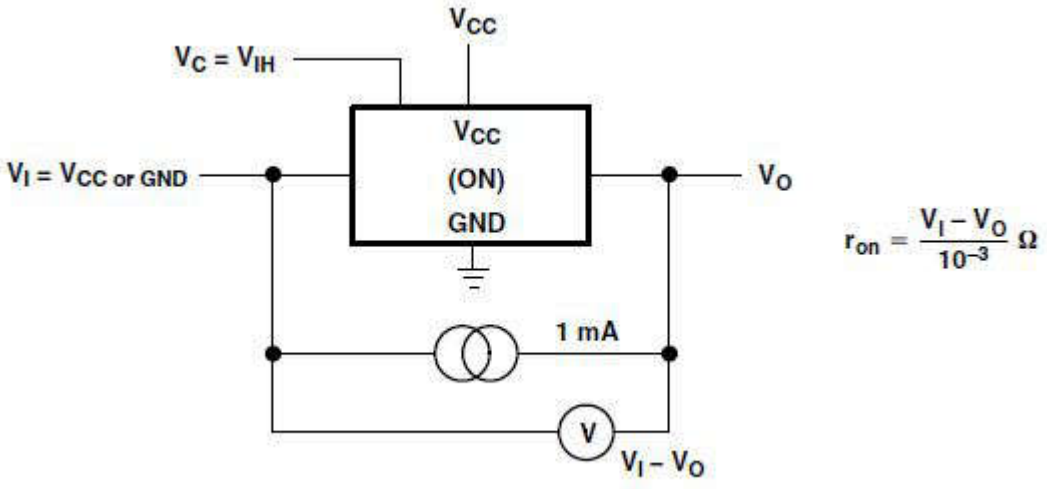


Figure 6-1. ON-State Resistance Test Circuit

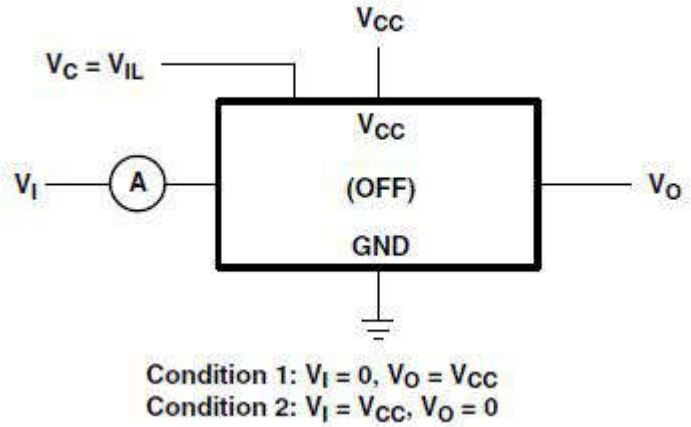


Figure 6-2. OFF-State Switch Leakage-Current Test Circuit

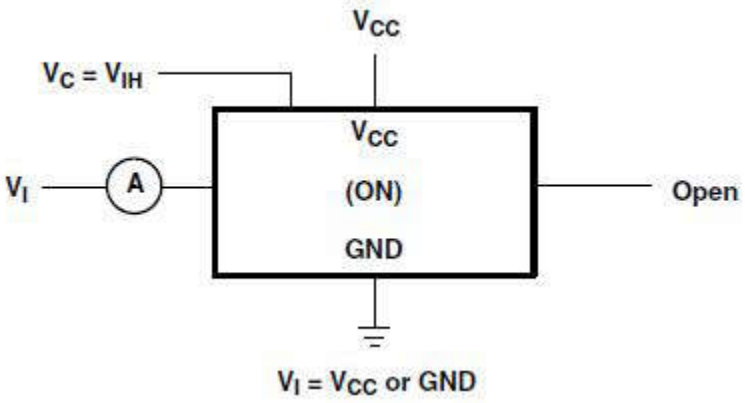


Figure 6-3. ON-State Leakage-Current Test Circuit

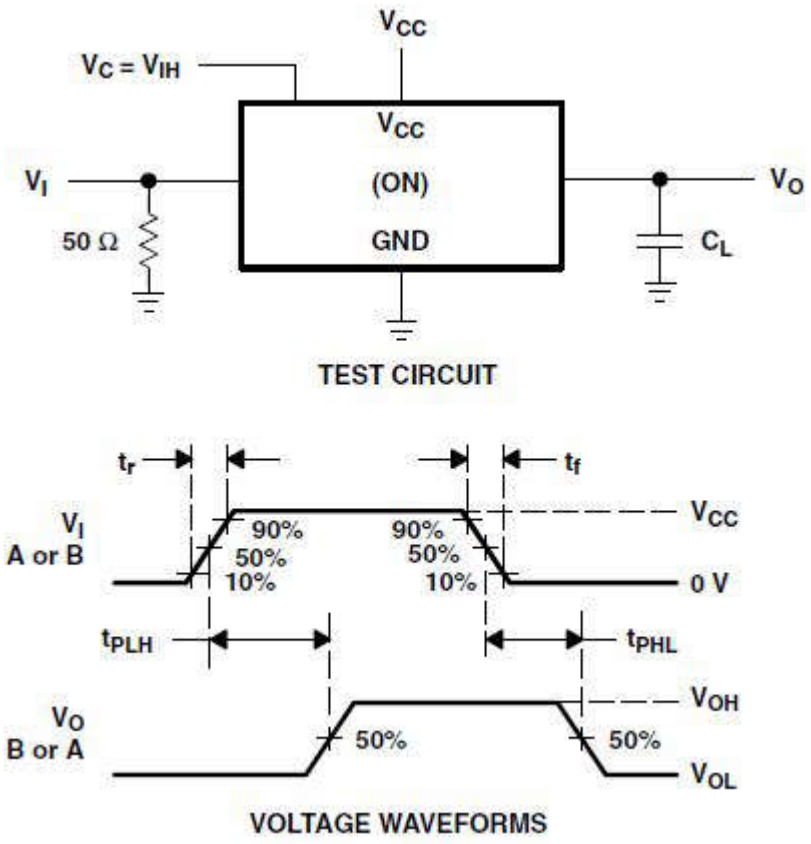
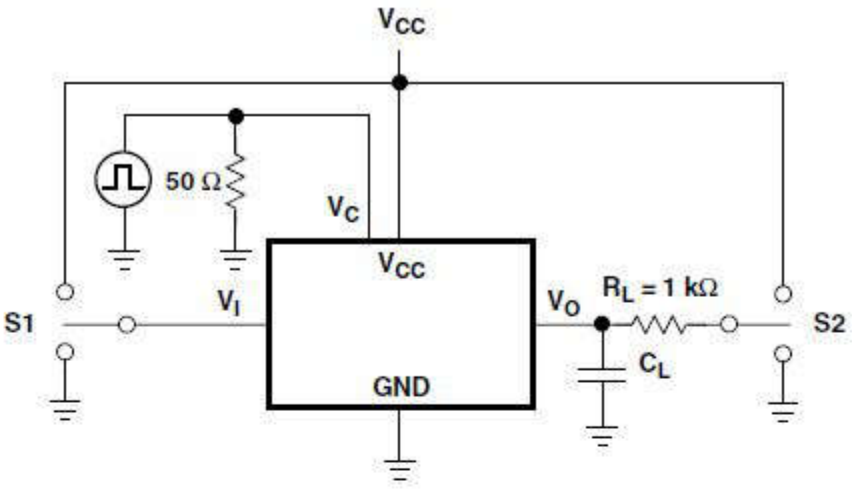
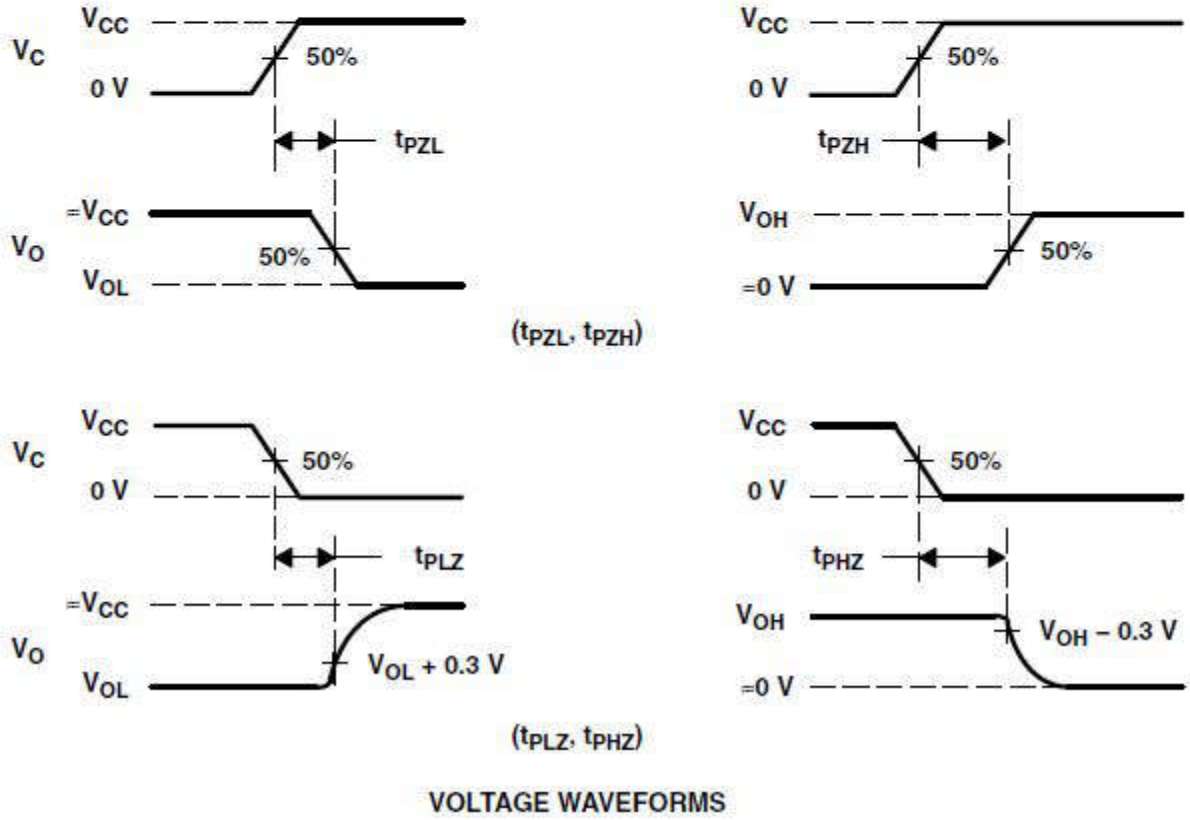


Figure 6-4. Propagation Delay Time, Signal Input to Signal Output



TEST CIRCUIT

TEST	S1	S2
t_{PZL}	GND	V_{CC}
t_{PZH}	V_{CC}	GND
t_{PLZ}	GND	V_{CC}
t_{PHZ}	V_{CC}	GND



VOLTAGE WAVEFORMS

Figure 6-5. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output

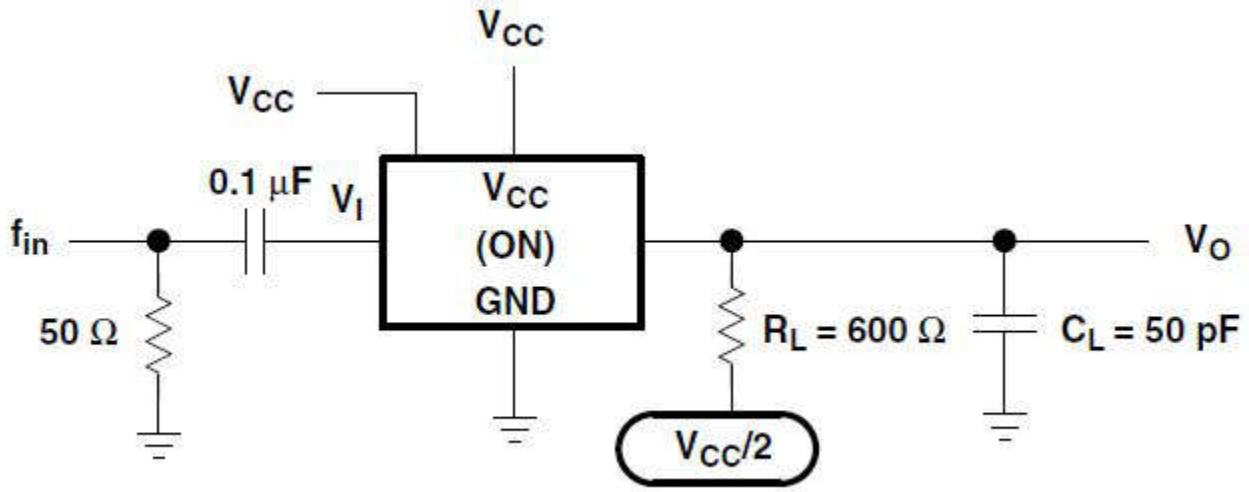


Figure 6-6. Frequency Response (Switch On)

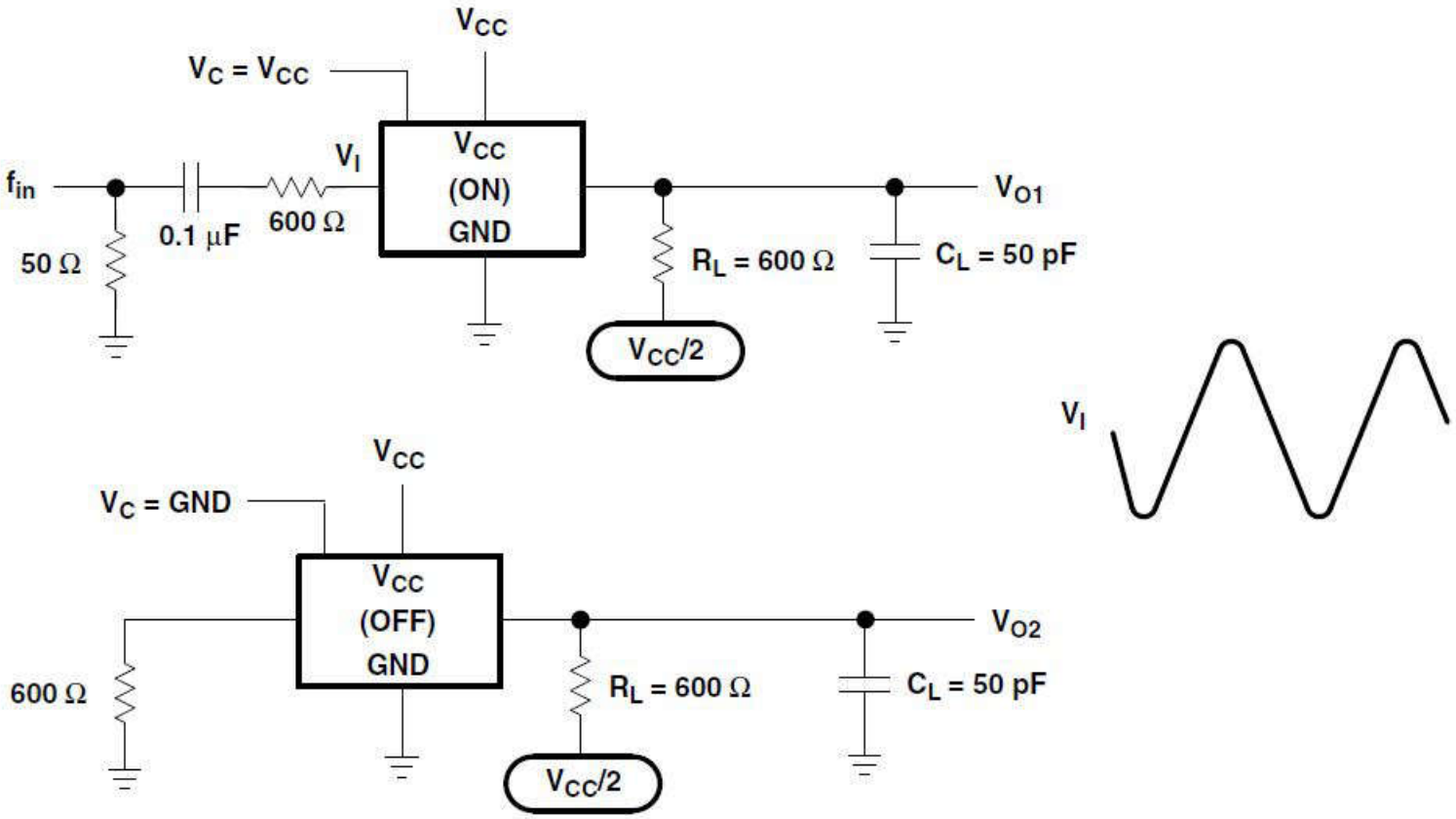


Figure 6-7. Crosstalk Between Any Two Switches

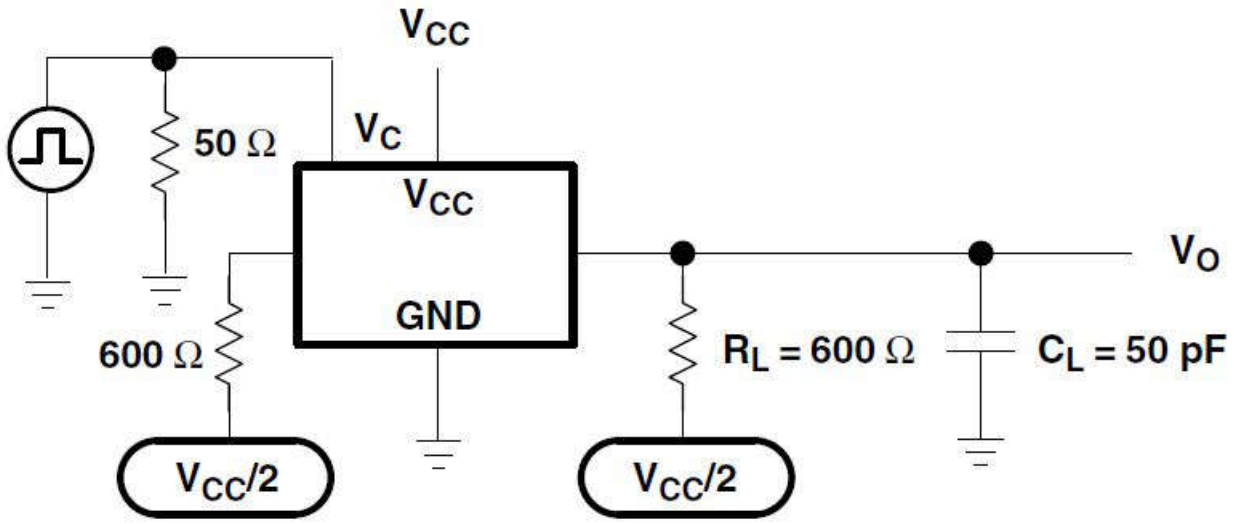


Figure 6-8. Crosstalk (Control Input - Switch Output)

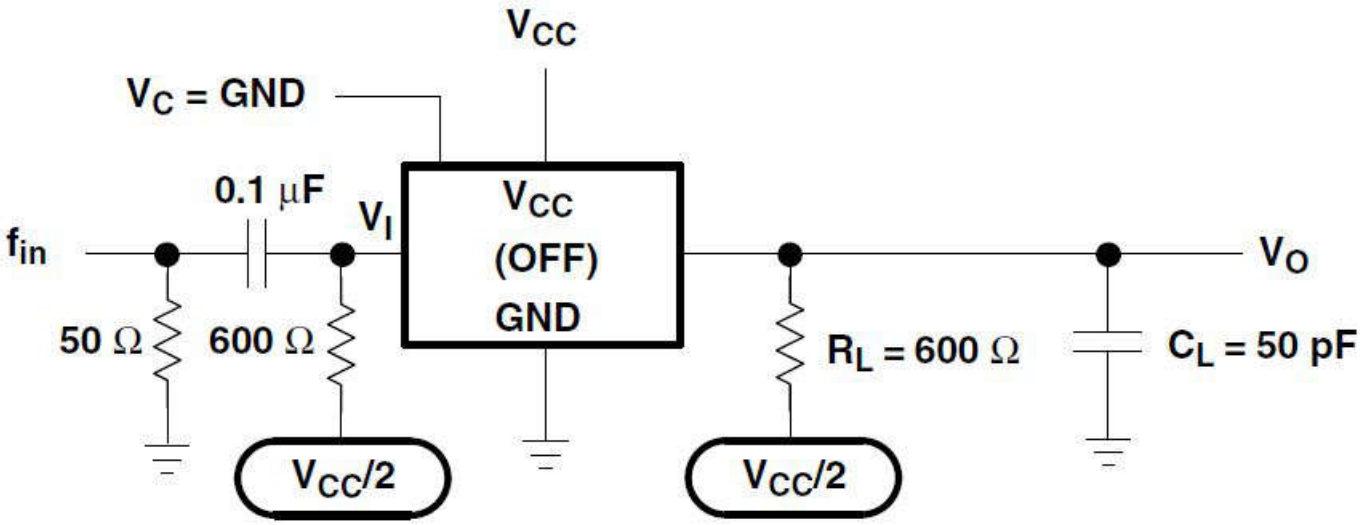


Figure 6-9. Feed-Through Attenuation (Switch Off)

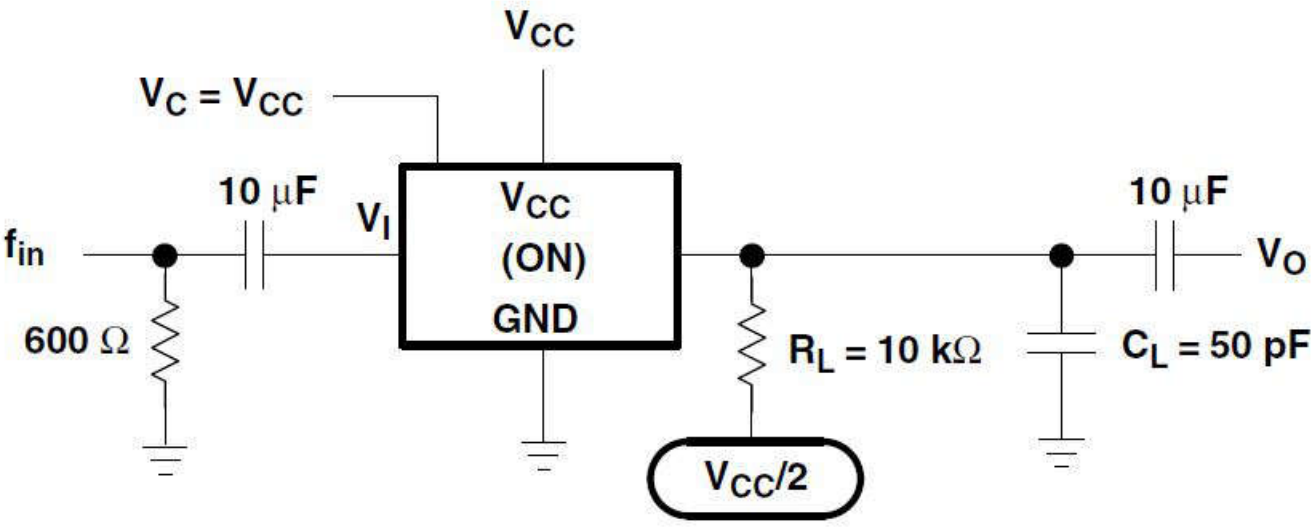


Figure 6-10. Sine-Wave Distortion

7 Detailed Description

7.1 Overview

The SN74AHC4066 device is a silicon-gate CMOS quadruple analog switch designed for 1V to 6V VCC operation. It is designed to handle both analog and digital signals. Each switch permits signals with amplitudes of up to 6V (peak) to be transmitted in either direction. A high-level voltage applied to the control pin C enables the respective switch to begin propagating signals across the device.

7.2 Functional Block Diagram

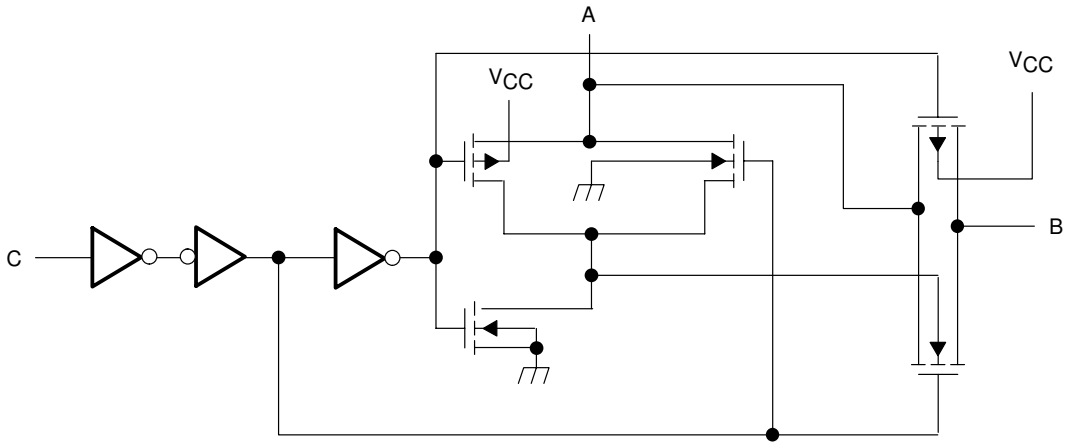


Figure 7-1. Logic Diagram, Each Switch (Positive Logic)

7.3 Device Functional Modes

Table 7-1 lists the functions for the SN74AHC4066 device.

Table 7-1. Function Table (Each Switch)

INPUT CONTROL (C)	SWITCH
L	OFF
H	ON

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application notes

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2003) to Revision A (February 2024)	Page
• Updated the data sheet to only include the *D*, *PW*, or *RGY* packages	1
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated the *Thermal Information*	3
• Updated V_{CC} operation from: 2V - 5.5V to: 1V - 5.5V	4

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC4066D	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC4066	
SN74AHC4066DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA4066	Samples
SN74AHC4066DGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA4066	Samples
SN74AHC4066DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC4066	Samples
SN74AHC4066N	ACTIVE	PDIP	N	14	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHC4066N	Samples
SN74AHC4066NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC4066	Samples
SN74AHC4066PW	LIFEBUY	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA4066	
SN74AHC4066PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA4066	Samples
SN74AHC4066RGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HA4066	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

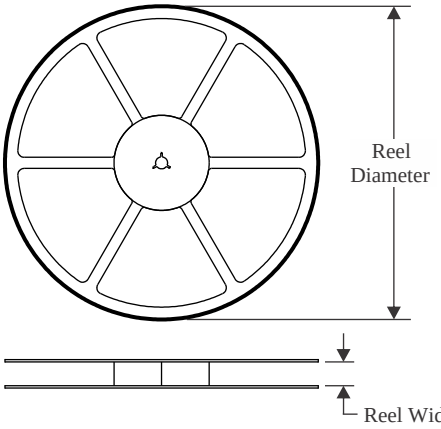
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

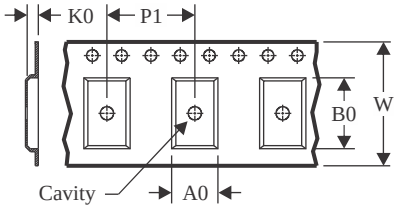
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

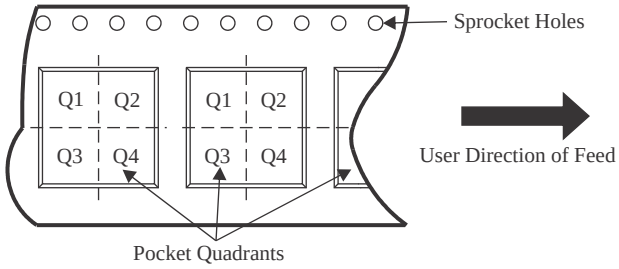


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

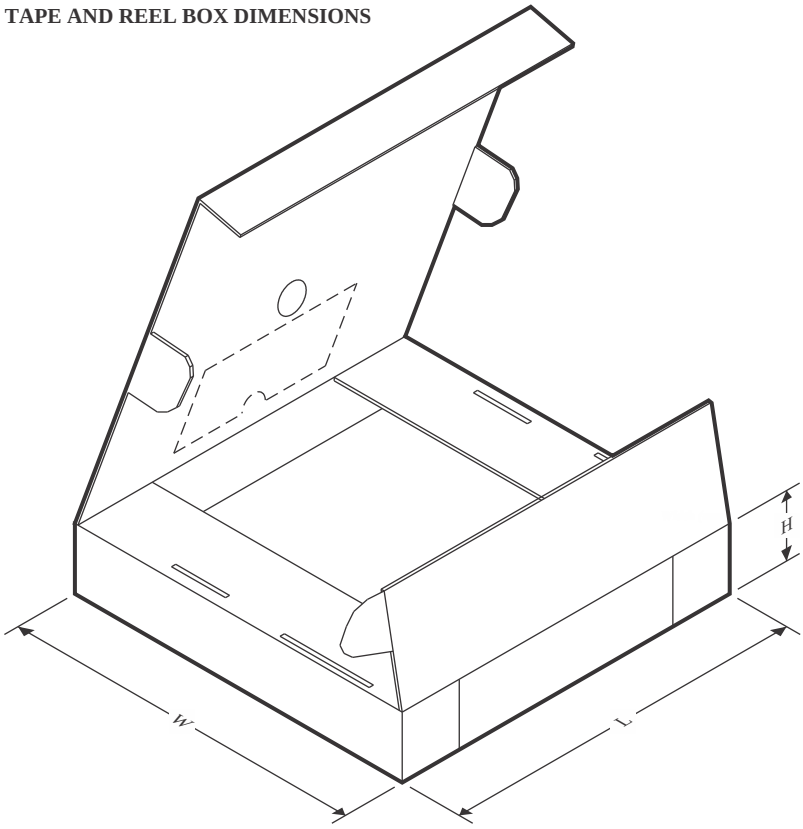
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC4066DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC4066DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC4066DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC4066NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHC4066PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC4066RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

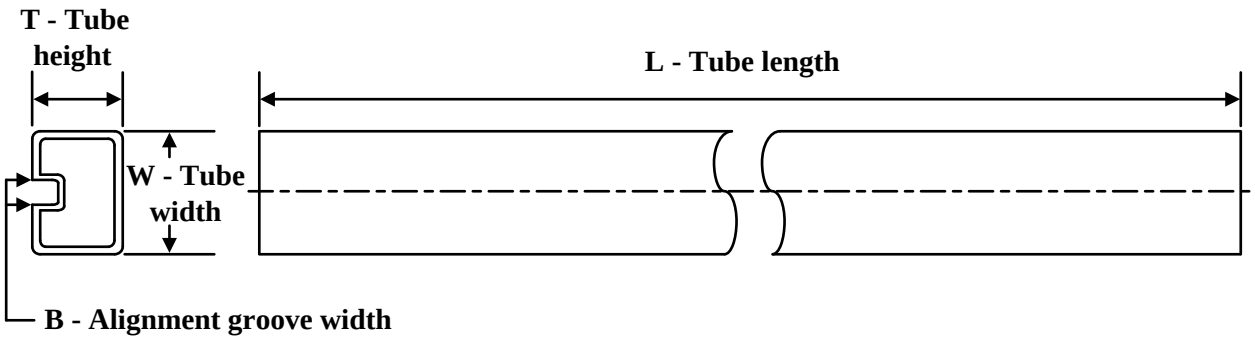
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC4066DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74AHC4066DGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74AHC4066DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74AHC4066NSR	SO	NS	14	2000	356.0	356.0	35.0
SN74AHC4066PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHC4066RGYR	VQFN	RGY	14	3000	367.0	367.0	35.0

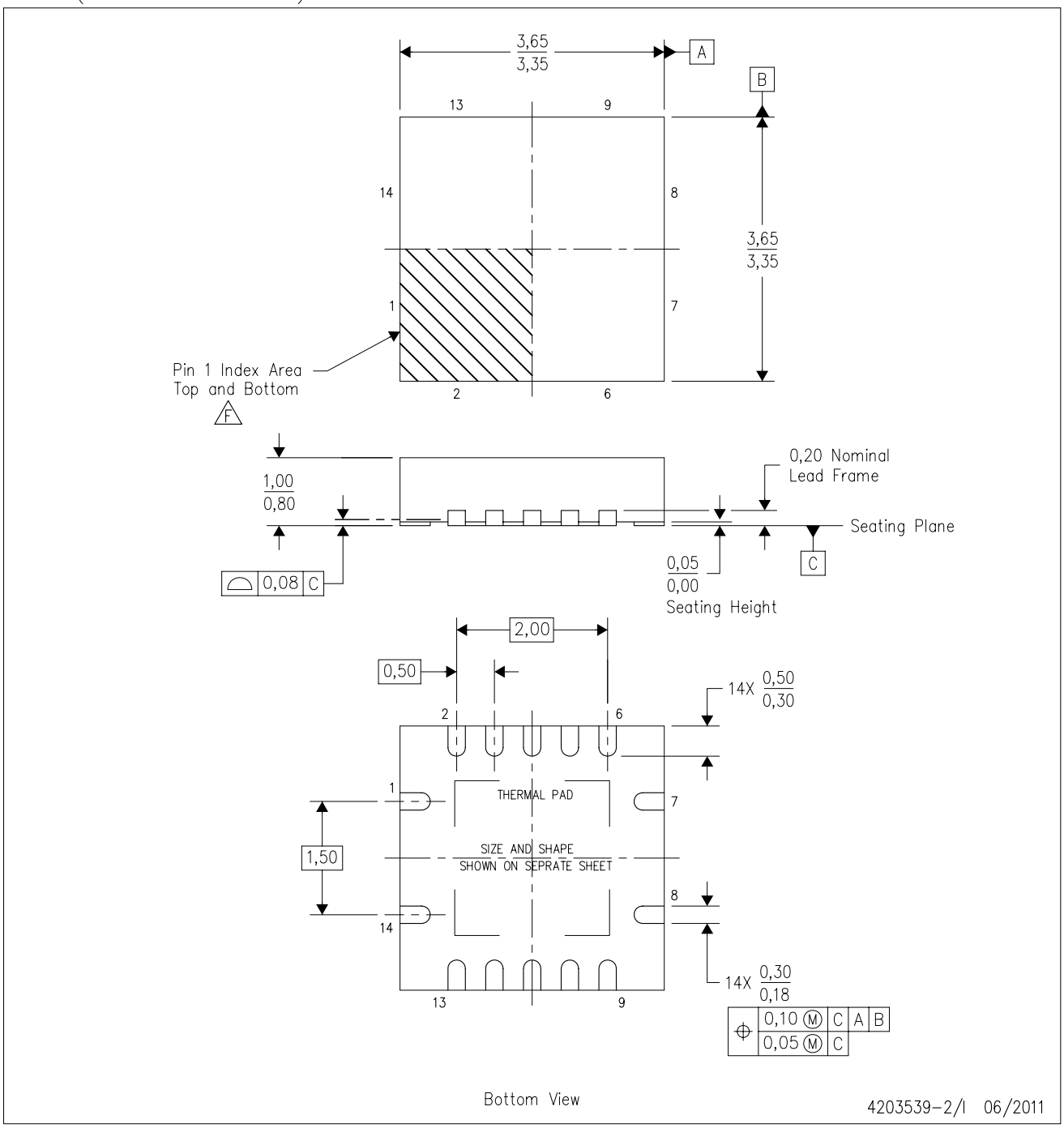
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74AHC4066D	D	SOIC	14	50	506.6	8	3940	4.32
SN74AHC4066N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC4066PW	PW	TSSOP	14	90	530	10.2	3600	3.5

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

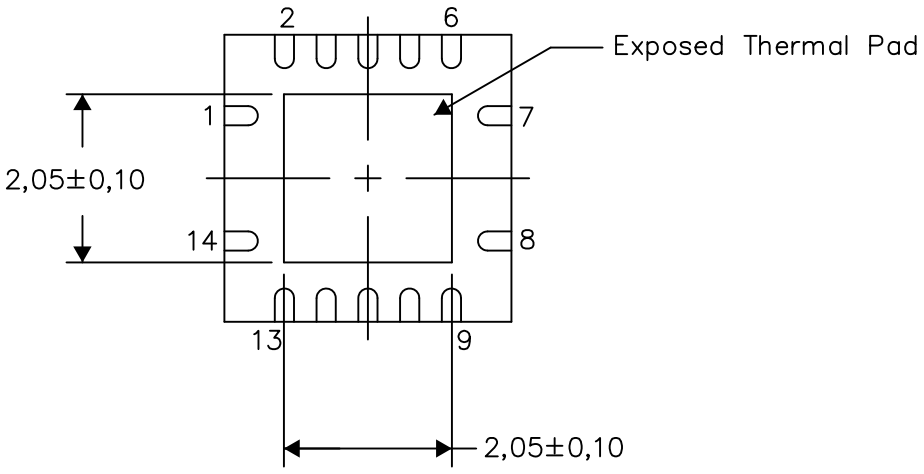
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



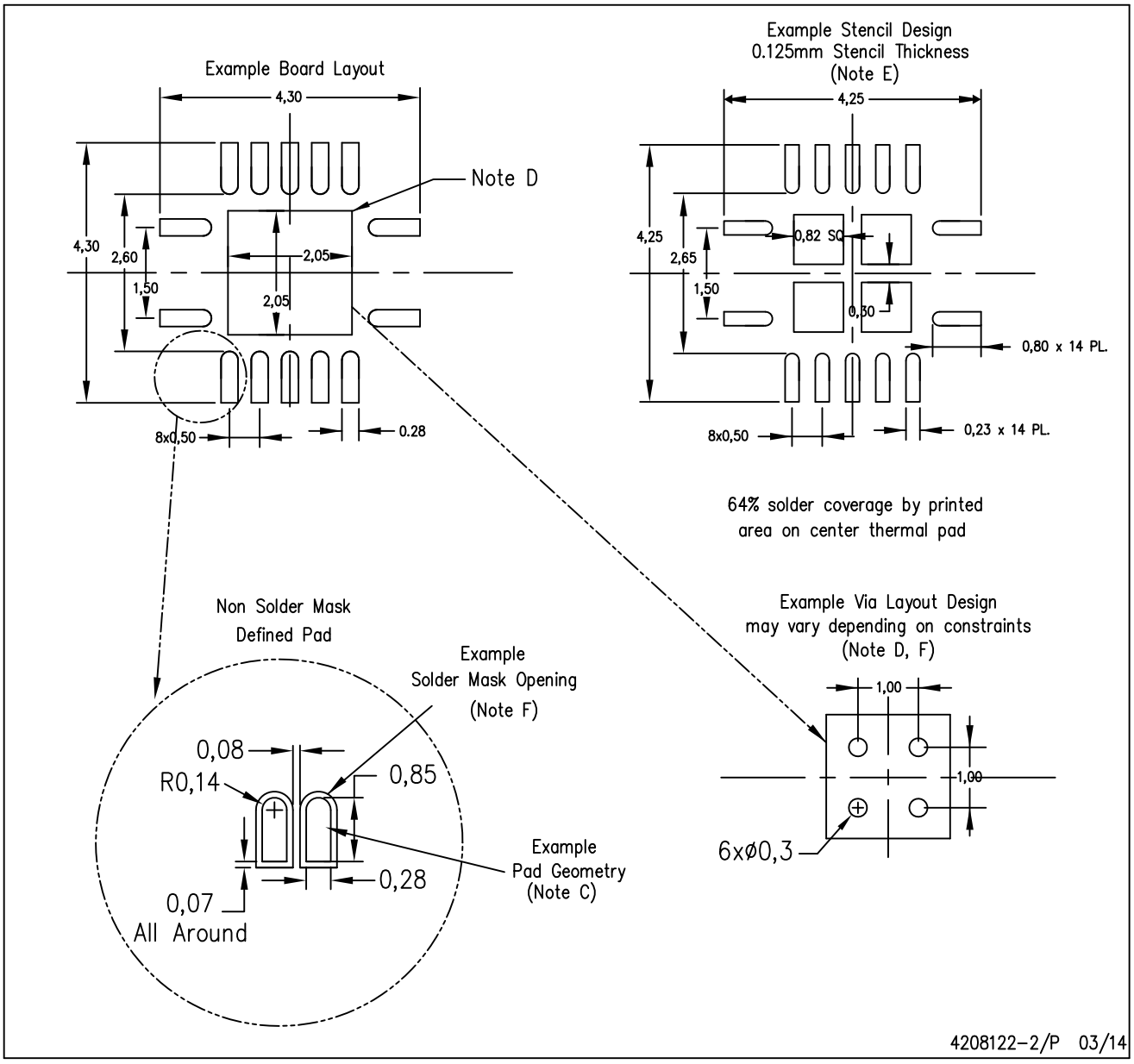
Bottom View

Exposed Thermal Pad Dimensions

4206353–2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

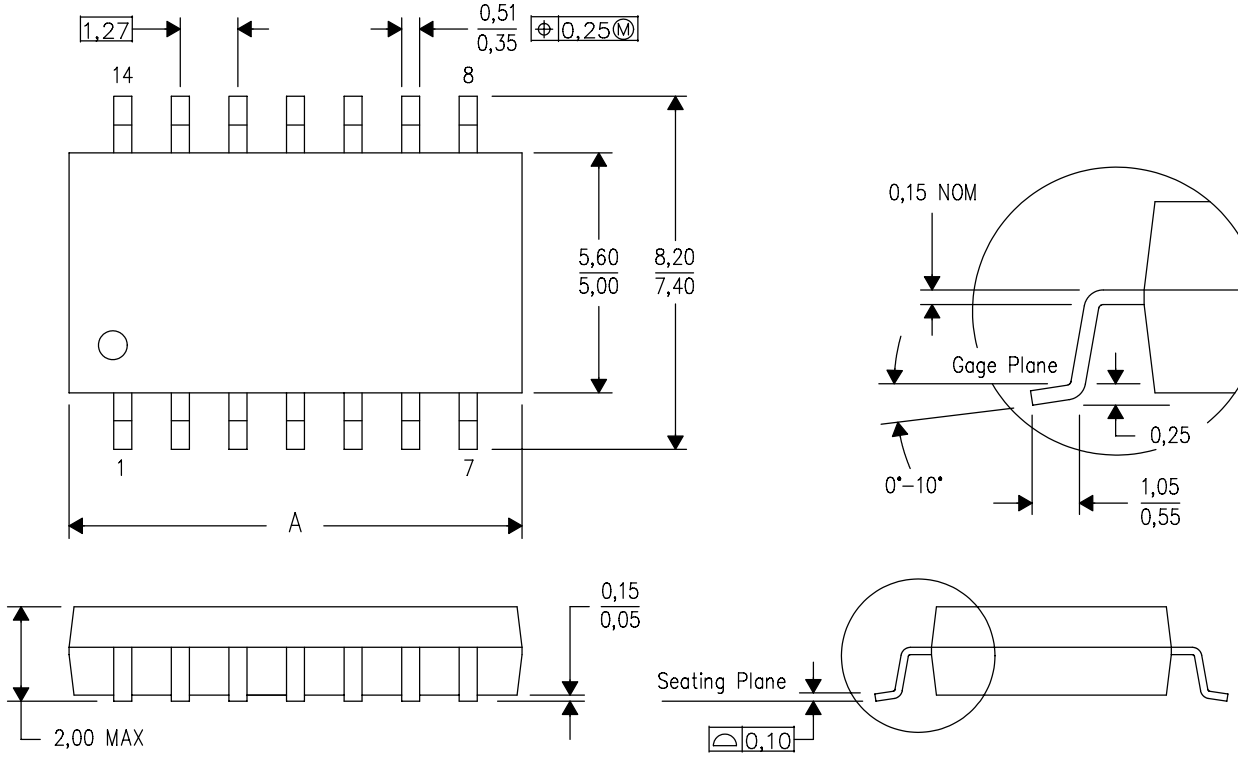


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



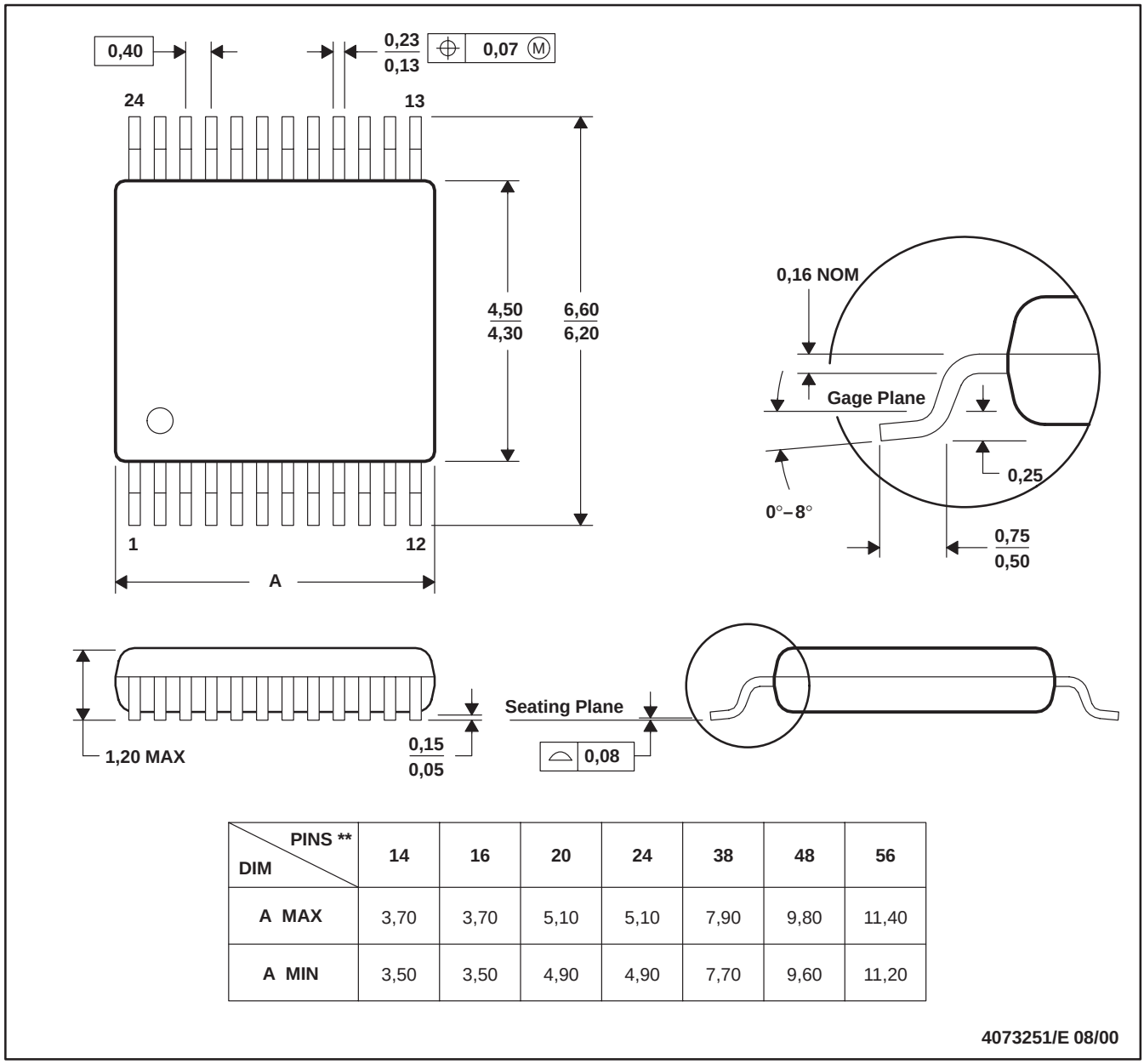
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

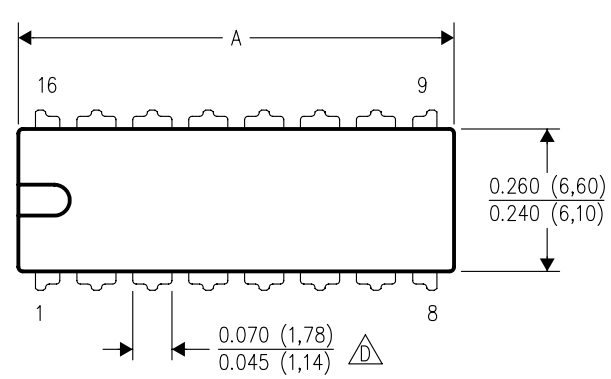
4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

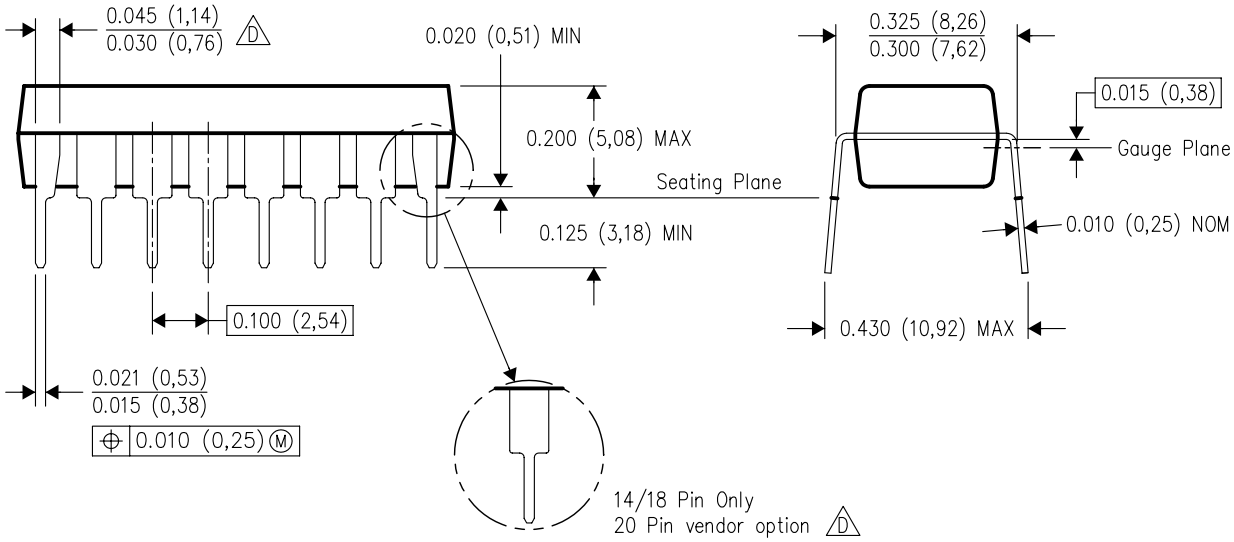
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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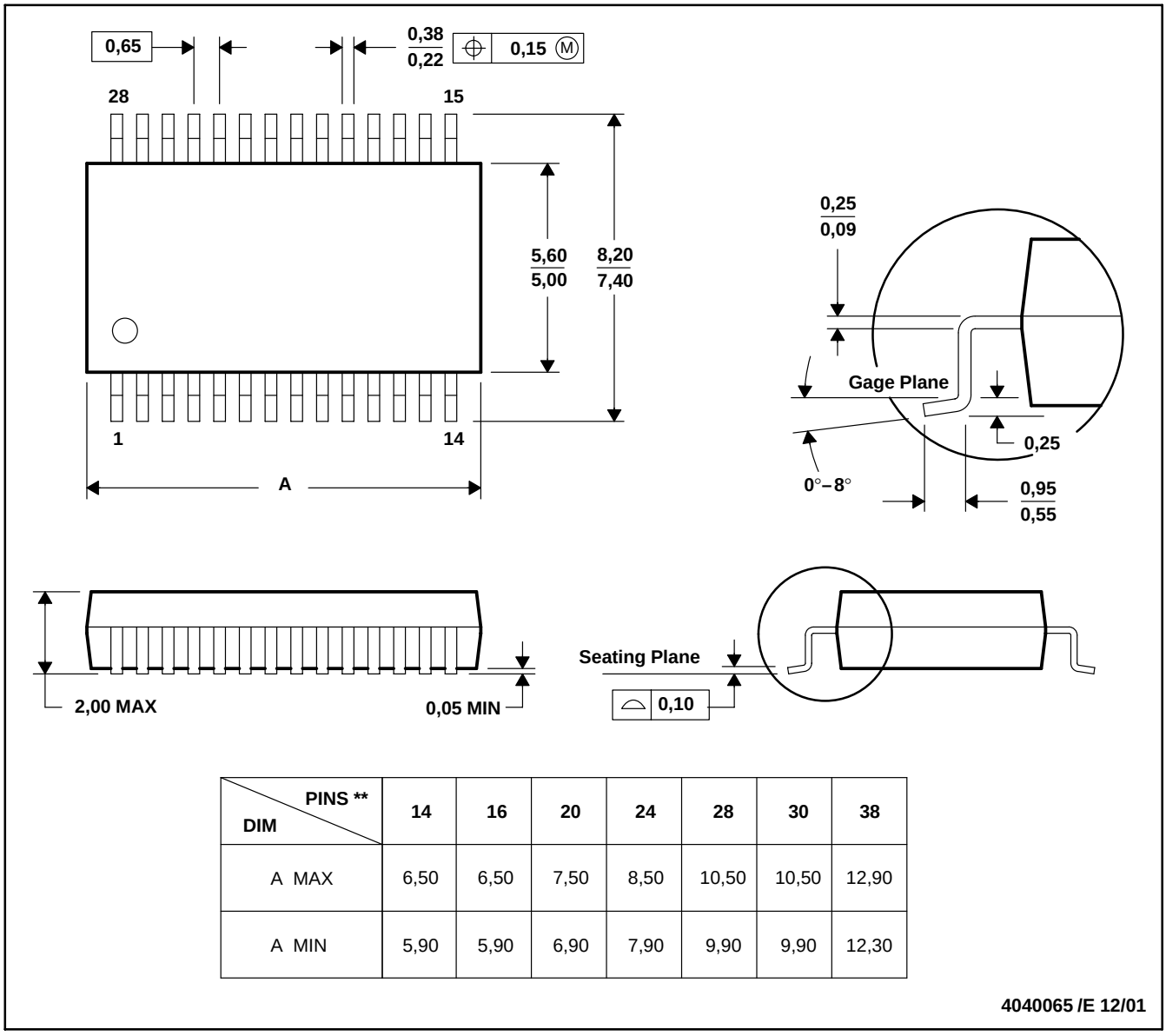
DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

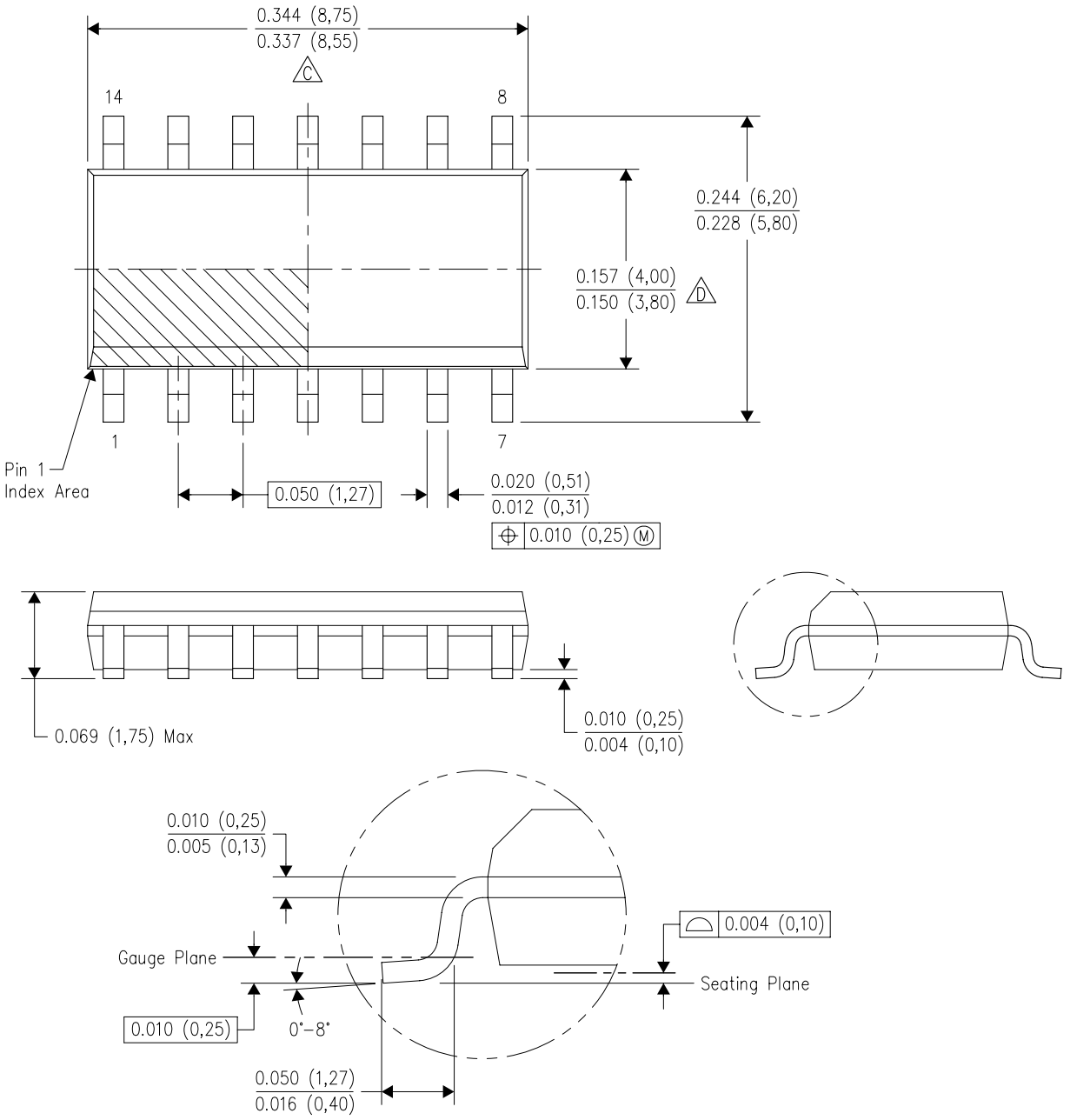


DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

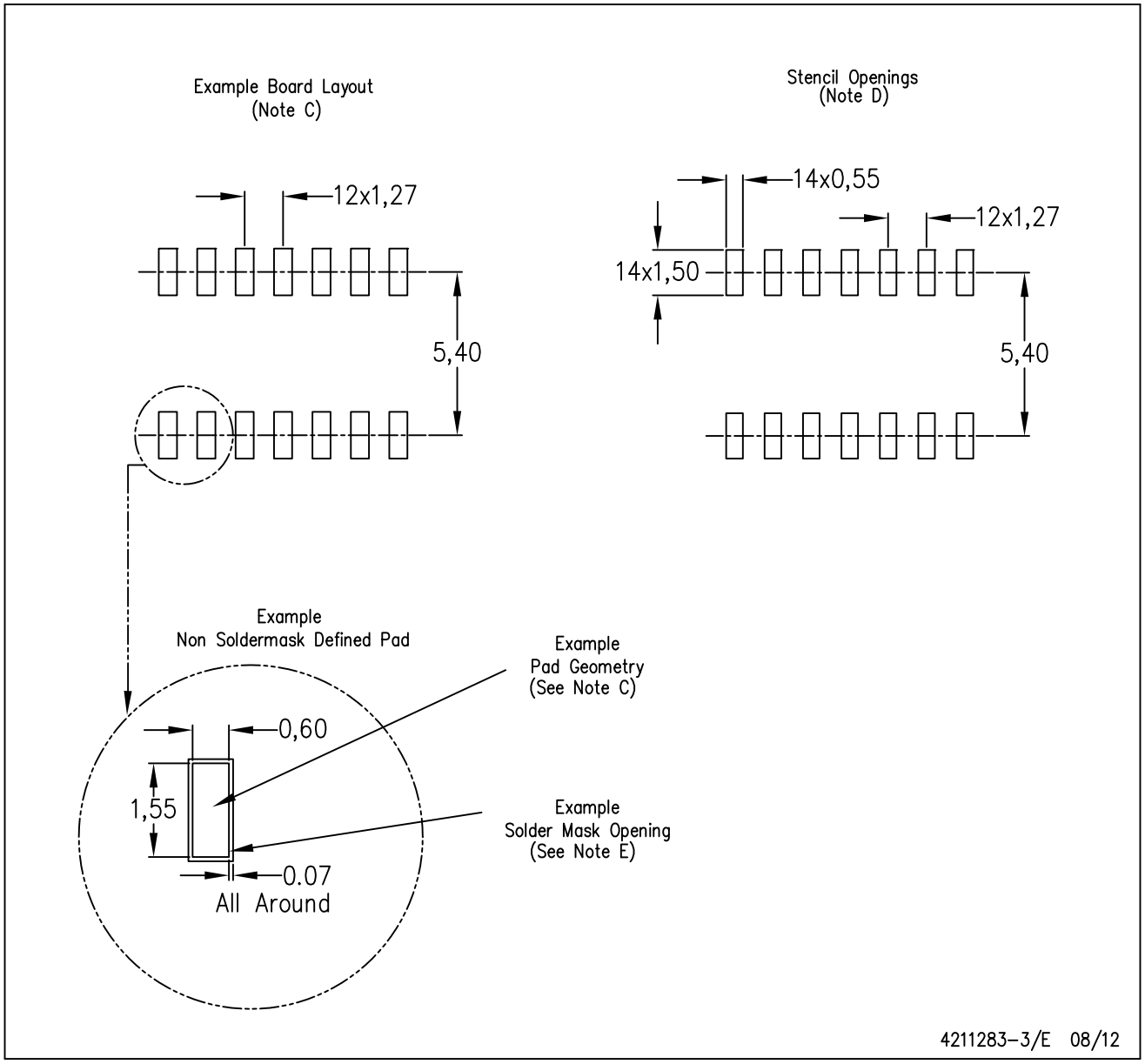
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

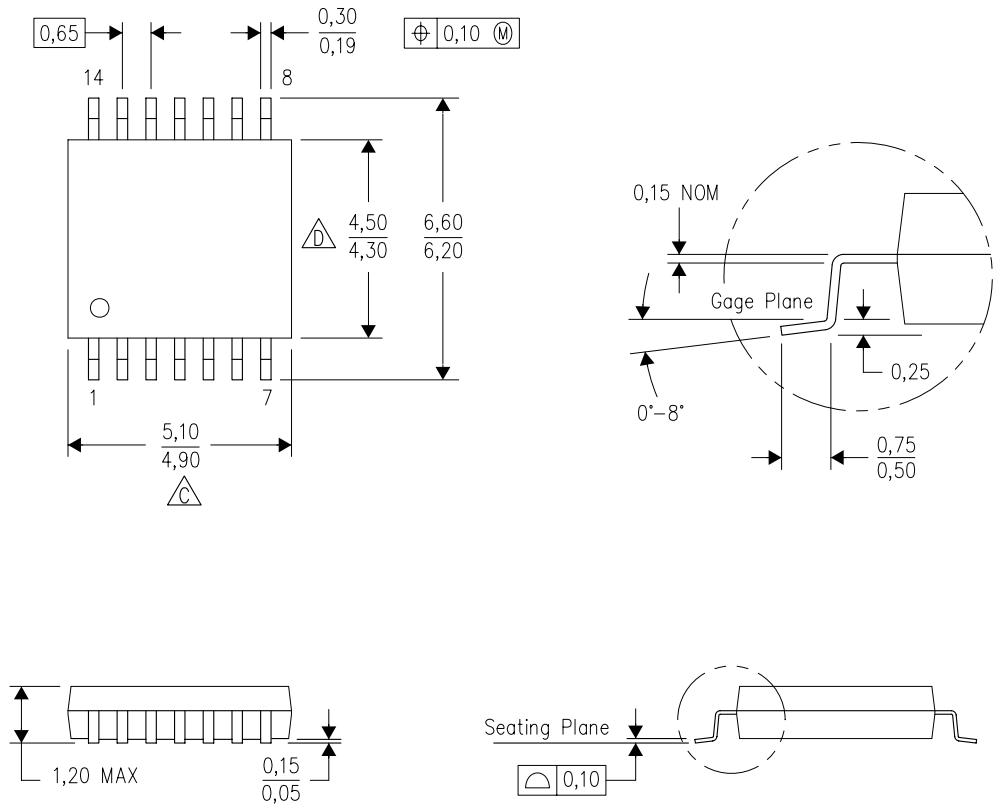
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

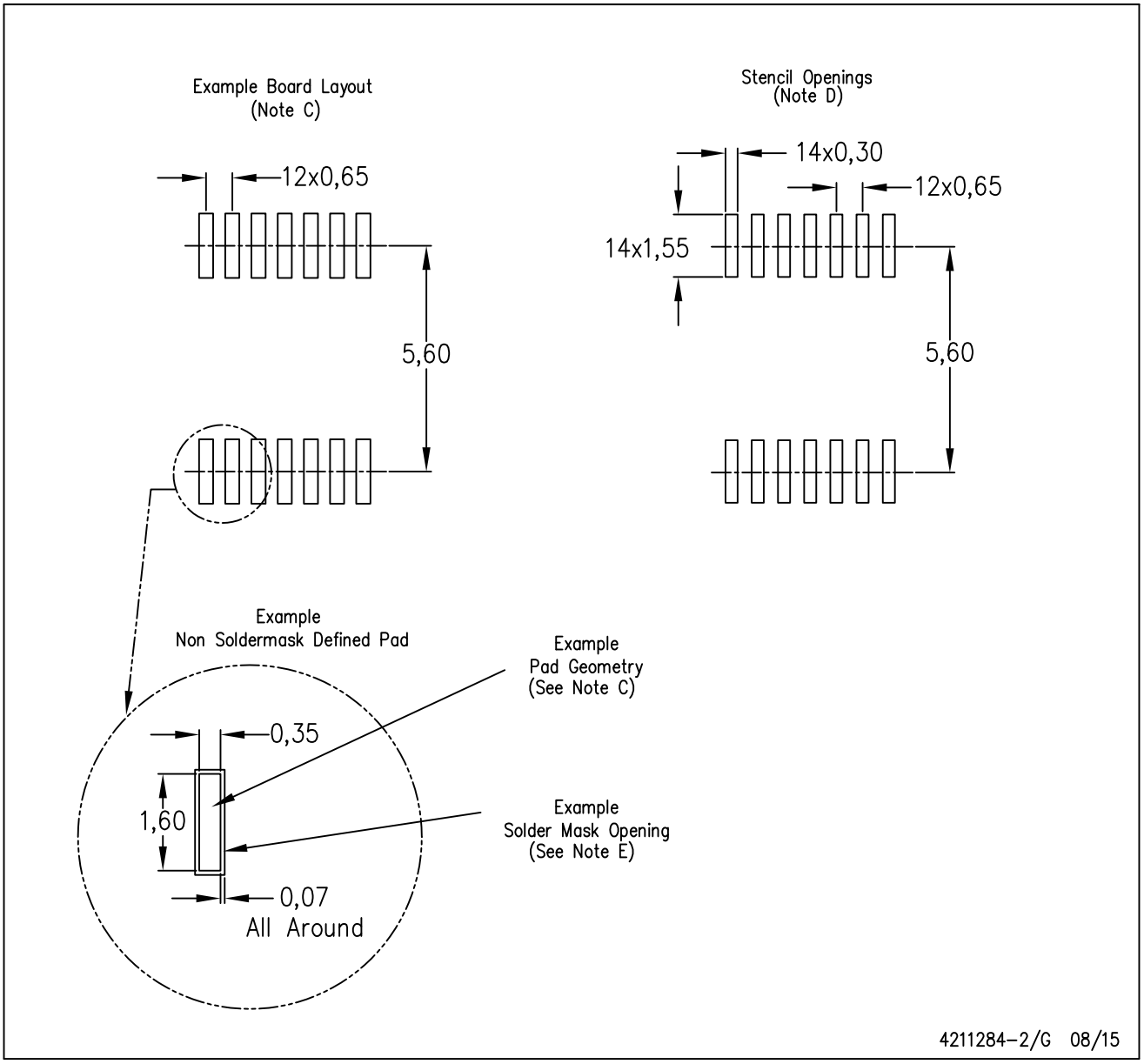
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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