

SN54AS1032A, SN74AS1032A QUADRUPLE 2-INPUT POSITIVE-OR BUFFERS/DRIVERS

SDAS072B – DECEMBER 1982 – REVISED JANUARY 1995

- Driver Version of 'AS32
- High Capacitive-Drive Capability
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

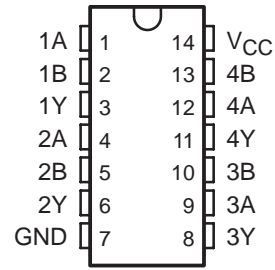
These devices contain four independent 2-input positive-OR buffers/drivers. They perform the Boolean functions $Y = A + B$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54AS1032A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS1032A is characterized for operation from 0°C to 70°C .

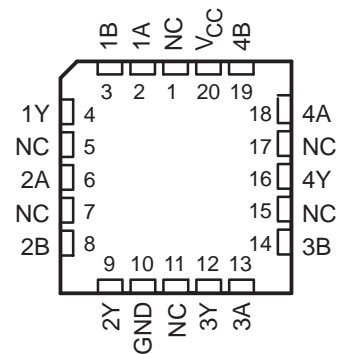
FUNCTION TABLE
(each gate)

| INPUTS | | OUTPUT Y |
|--------|---|-------------|
| A | B | |
| H | X | H |
| X | H | H |
| L | L | L |

SN54AS1032A . . . J PACKAGE
SN74AS1032A . . . D OR N PACKAGE
(TOP VIEW)

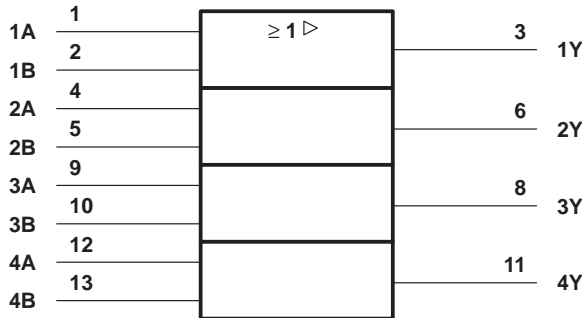


SN54AS1032A . . . FK PACKAGE
(TOP VIEW)

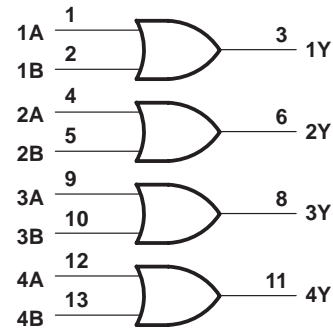


NC – No internal connection

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, and N packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------|
| Supply voltage, V_{CC} | 7 V |
| Input voltage, V_I | 7 V |
| Operating free-air temperature range, T_A : SN54AS1032A | -55°C to 125°C |
| SN74AS1032A | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions‡

| | | SN54AS1032A | | | SN74AS1032A | | | UNIT |
|----------|--------------------------------|-------------|-----|-----|-------------|-----|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I_{OH} | High-level output current | | | -40 | | | -48 | mA |
| I_{OL} | Low-level output current | | | 40 | | | 48 | mA |
| T_A | Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

‡ These high sink- or source-current devices are not recommended for use above 40 MHz.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SN54AS1032A | | | SN74AS1032A | | | UNIT |
|---------------------|---|--------------|------|------|--------------|------|------|------|
| | | MIN | TYP§ | MAX | MIN | TYP§ | MAX | |
| V_{IK} | $V_{CC} = 4.5$ V, $I_I = -18$ mA | | | -1.2 | | | -1.2 | V |
| V_{OH} | $V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -2$ mA | $V_{CC} - 2$ | | | $V_{CC} - 2$ | | | V |
| | $V_{CC} = 4.5$ V, $I_{OH} = -3$ mA | 2.4 | 3.2 | | 2.4 | 3.2 | | |
| | $V_{CC} = 4.5$ V, $I_{OH} = -40$ mA | 2 | | | | | | |
| V_{OL} | $V_{CC} = 4.5$ V, $I_{OH} = -48$ mA | | | | 2 | | | V |
| | $V_{CC} = 4.5$ V, $I_{OL} = 40$ mA | 0.25 | | | 0.5 | | | |
| | $V_{CC} = 4.5$ V, $I_{OL} = 48$ mA | | | | 0.35 | | | |
| I_I | $V_{CC} = 5.5$ V, $V_I = 7$ V | | | 0.1 | | | 0.1 | mA |
| I_{IH} | $V_{CC} = 5.5$ V, $V_I = 2.7$ V | | | 20 | | | 20 | μA |
| I_{IL} | $V_{CC} = 5.5$ V, $V_I = 0.4$ V | | | -0.5 | | | -0.5 | mA |
| I_{O}^{\parallel} | $V_{CC} = 5.5$ V, $V_O = 2.25$ V | -50 | | -200 | -50 | | -200 | mA |
| I_{CCH} | $V_{CC} = 5.5$ V, $V_I = 4.5$ V | | 7.7 | 11.5 | | 7.7 | 11.5 | mA |
| I_{CCL} | $V_{CC} = 5.5$ V, $V_I = 0$ | | 14.7 | 24 | | 14.7 | 24 | mA |

§ All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

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switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}^\dagger$ | | | | UNIT |
|-----------|-----------------|----------------|---|-----|-------------|-----|------|
| | | | SN54AS1032A | | SN74AS1032A | | |
| | | | MIN | MAX | MIN | MAX | |
| t_{PLH} | A or B | Y | 1 | 7 | 1 | 6.3 | ns |
| t_{PHL} | | | 1 | 7 | 1 | 6.3 | |

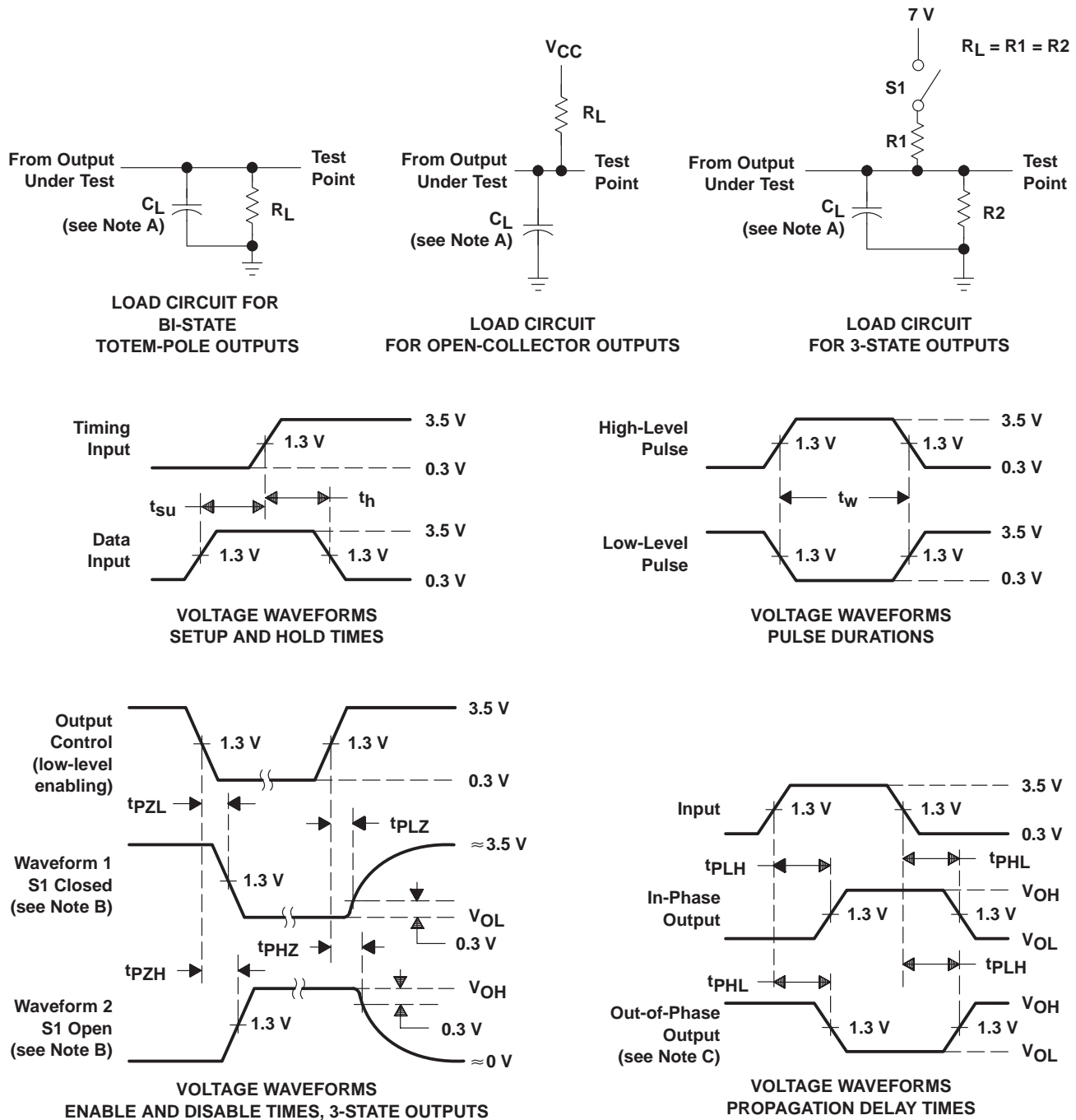
[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74AS1032AD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS1032A | Samples |
| SN74AS1032AN | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74AS1032AN | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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