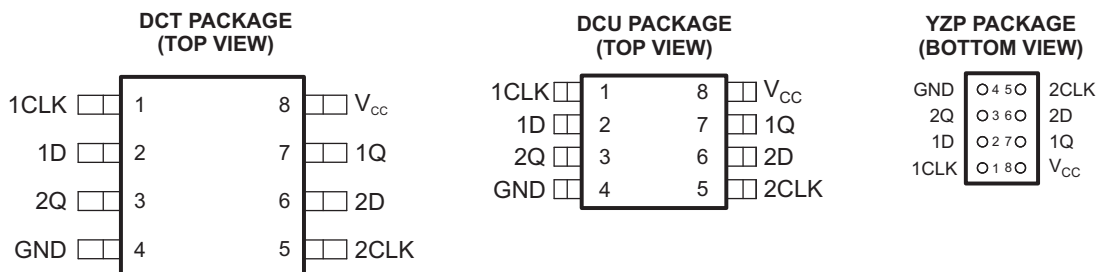


FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial Power-Down-Mode Operation
- Sub-1-V Operable
- Max t_{pd} of 1.9 ns at 1.8 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 8 -mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This single positive-edge-triggered D-type flip-flop is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

When data at the data (D) input meets the setup time requirement, the data is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽²⁾
–40°C to 85°C	NanoFree™ – WCSP (DSBGA)	Reel of 3000	SN74AUC2G79YZPR	__ _UR_
	0.23-mm Large Bump – YZP (Pb-free)			
	SSOP – DCT	Reel of 3000	SN74AUC2G79DCTR	U79_ _
	VSSOP – DCU	Reel of 3000	SN74AUC2G79DCUR	U79_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.

DCU: The actual top-side marking has one additional character that designates the assembly/test site.

YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

SN74AUC2G79

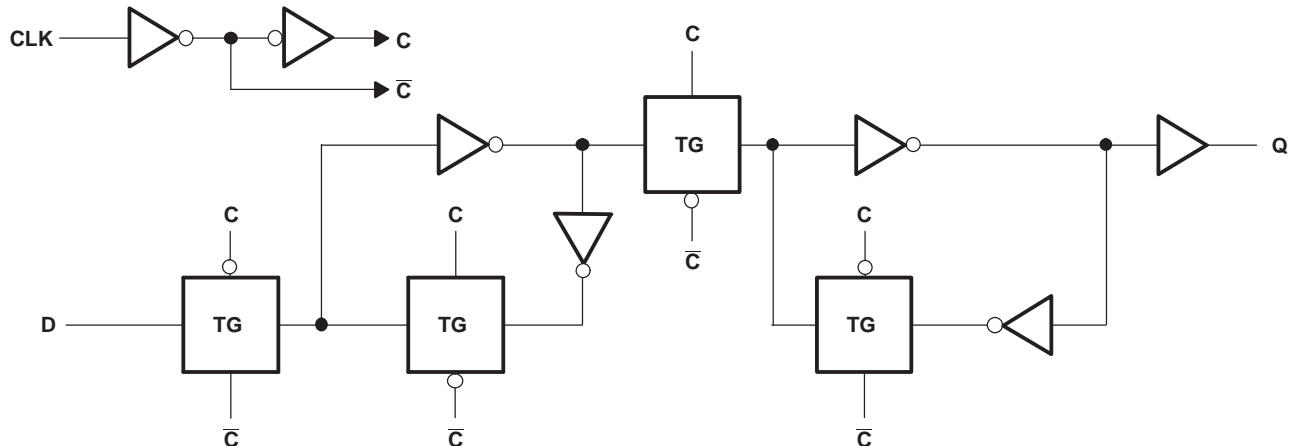
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCES536C–DECEMBER 2003–REVISED JANUARY 2007

FUNCTION TABLE

INPUTS		OUTPUT Q
CLK	D	
↑	H	H
↑	L	L
L	X	Q ₀

LOGIC DIAGRAM, EACH FLIP-FLOP (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	−0.5	3.6	V
V _I	Input voltage range ⁽²⁾	−0.5	3.6	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	−0.5	3.6	V
V _O	Output voltage range ⁽²⁾	−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current		−50	mA
I _{OK}	Output clamp current		−50	mA
I _O	Continuous output current		±20	mA
	Continuous current through V _{CC} or GND		±100	mA
θ _{JA}	Package thermal impedance ⁽³⁾	DCT package	220	°C/W
		DCU package	227	
		YZP package	102	
T _{stg}	Storage temperature range	−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		0.8	2.7	V
V _{IH}	High-level input voltage	V _{CC} = 0.8 V	V _{CC}		V
		V _{CC} = 1.1 V to 1.95 V	0.65 × V _{CC}		
		V _{CC} = 2.3 V to 2.7 V	1.7		
V _{IL}	Low-level input voltage	V _{CC} = 0.8 V	0		V
		V _{CC} = 1.1 V to 1.95 V	0.35 × V _{CC}		
		V _{CC} = 2.3 V to 2.7 V	0.7		
V _I	Input voltage		0	3.6	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 0.8 V	−0.7		mA
		V _{CC} = 1.1 V	−3		
		V _{CC} = 1.4 V	−5		
		V _{CC} = 1.65 V	−8		
		V _{CC} = 2.3 V	−9		
I _{OL}	Low-level output current	V _{CC} = 0.8 V	0.7		mA
		V _{CC} = 1.1 V	3		
		V _{CC} = 1.4 V	5		
		V _{CC} = 1.65 V	8		
		V _{CC} = 2.3 V	9		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 0.8 V to 1.65 V ⁽²⁾	20		ns/V
		V _{CC} = 1.65 V to 2.3 V ⁽³⁾	20		
		V _{CC} = 2.3 V to 2.7 V ⁽³⁾	20		
T _A	Operating free-air temperature		−40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(2) The data was taken at C_L = 15 pF, R_L = 2 kΩ (see Figure 1).

(3) The data was taken at C_L = 30 pF, R_L = 500 Ω (see Figure 1).

SN74AUC2G79

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCES536C–DECEMBER 2003–REVISED JANUARY 2007

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}		I _{OH} = −100 μA	0.8 V to 2.7 V	V _{CC} − 0.1			V
		I _{OH} = −0.7 mA	0.8 V	0.55			
		I _{OH} = −3 mA	1.1 V	0.8			
		I _{OH} = −5 mA	1.4 V	1			
		I _{OH} = −8 mA	1.65 V	1.2			
		I _{OH} = −9 mA	2.3 V	1.8			
V _{OL}		I _{OL} = 100 μA	0.8 V to 2.7 V	0.2			V
		I _{OL} = 0.7 mA	0.8 V	0.25			
		I _{OL} = 3 mA	1.1 V	0.3			
		I _{OL} = 5 mA	1.4 V	0.4			
		I _{OL} = 8 mA	1.65 V	0.45			
		I _{OL} = 9 mA	2.3 V	0.6			
I _I	D or CLK inputs	V _I = V _{CC} or GND	0 to 2.7 V	±5			μA
I _{off}		V _I or V _O = 2.7 V	0	±10			μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	0.8 V to 2.7 V	10			μA
C _i		V _I = V _{CC} or GND	2.5 V	2.5			pF

(1) All typical values are at T_A = 25°C.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

		V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V	V _{CC} = 1.5 V ± 0.1 V	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	UNIT
		TYP	MIN MAX	MIN MAX	MIN MAX	MIN MAX	
f _{clock}	Clock frequency	50	200	225	250	275	MHz
t _w	Pulse duration, CLK high or low	2.4	1	1	1	1	ns
t _{su}	Setup time before CLK↑	1.6	0.9	0.6	0.6	0.5	ns
t _h	Hold time, data after CLK↑	0	0	0	0.1	0.1	ns

Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V	V _{CC} = 1.5 V ± 0.1 V	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	UNIT					
			TYP	MIN	MAX	MIN	MAX		MIN	TYP	MAX	MIN	MAX
f _{max}			50	200		225		250		275	MHz		
t _{pd}	CLK	Q	5	1	3.9	0.8	2.5	0.3	1	1.9	0.3	1.3	ns

Switching Characteristics

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see [Figure 1](#))

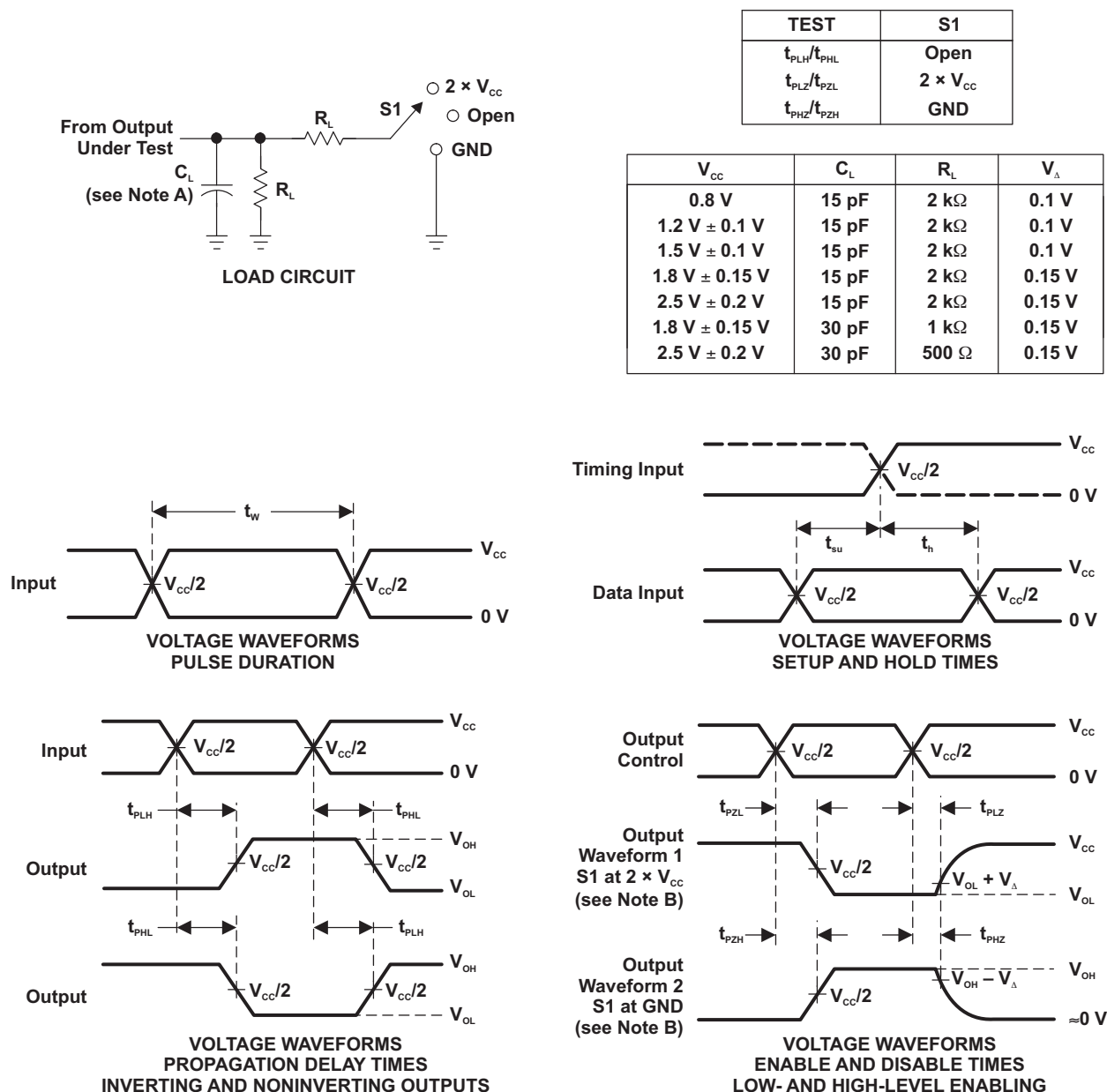
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V			V _{CC} = 2.5 V ± 0.2 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}			250			275			ns
t _{pd}	CLK	Q	0.8	1.5	2.4	0.6	1.8		ns

Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V}$	$V_{CC} = 1.5\text{ V}$	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	$f = 10\text{ MHz}$	16	16.2	18	19.8	29.2	pF
	CLK		1.1	1.1	1.2	1.5	2.7	
	Total		17.1	17.3	19.2	21.3	31.9	

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50 \Omega$, slew rate \geq 1 V/ns.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUC2G79DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	U79 (R ~ Z)	Samples
SN74AUC2G79DCUR	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 85	(U79Q ~ U79R)	Samples
SN74AUC2G79YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	URN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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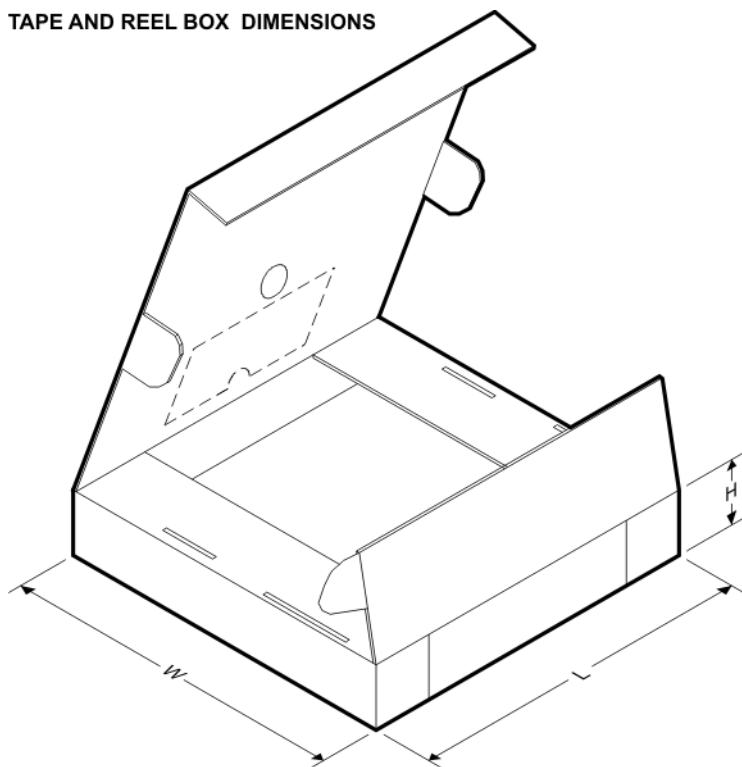
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC2G79DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74AUC2G79DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G79DCUR	VSSOP	DCU	8	3000	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G79YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

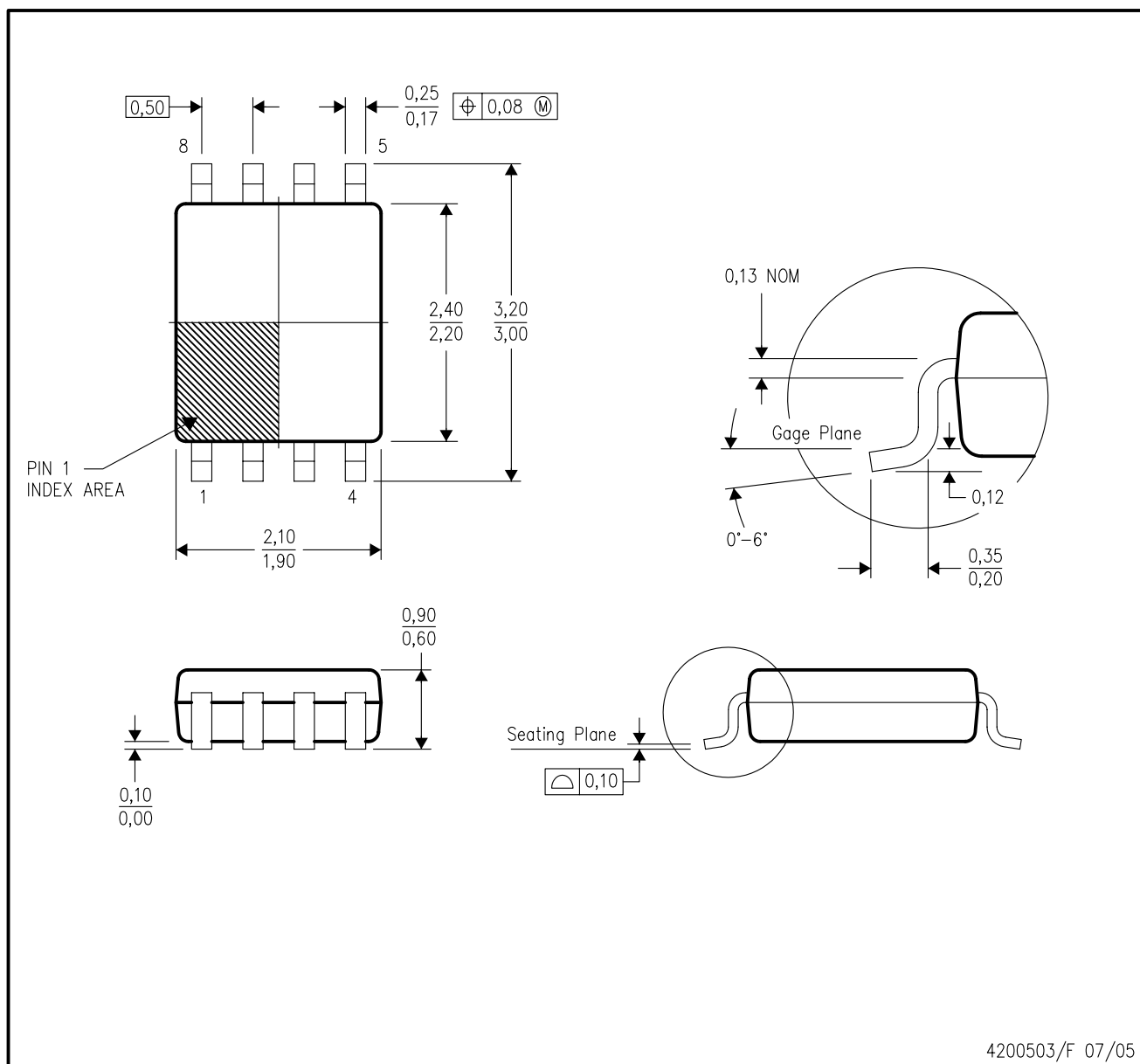


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC2G79DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
SN74AUC2G79DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUC2G79DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUC2G79YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)

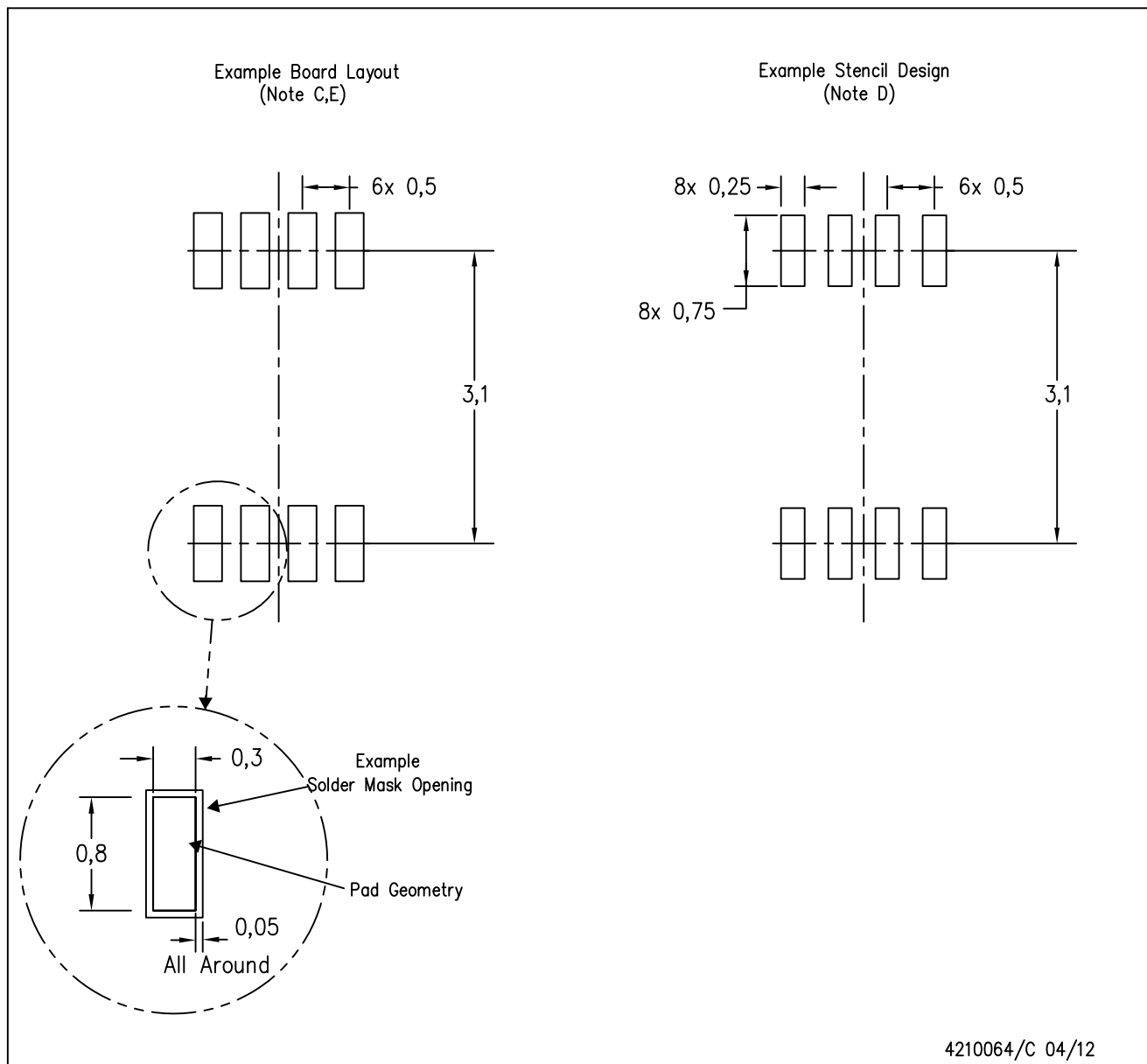


NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8)

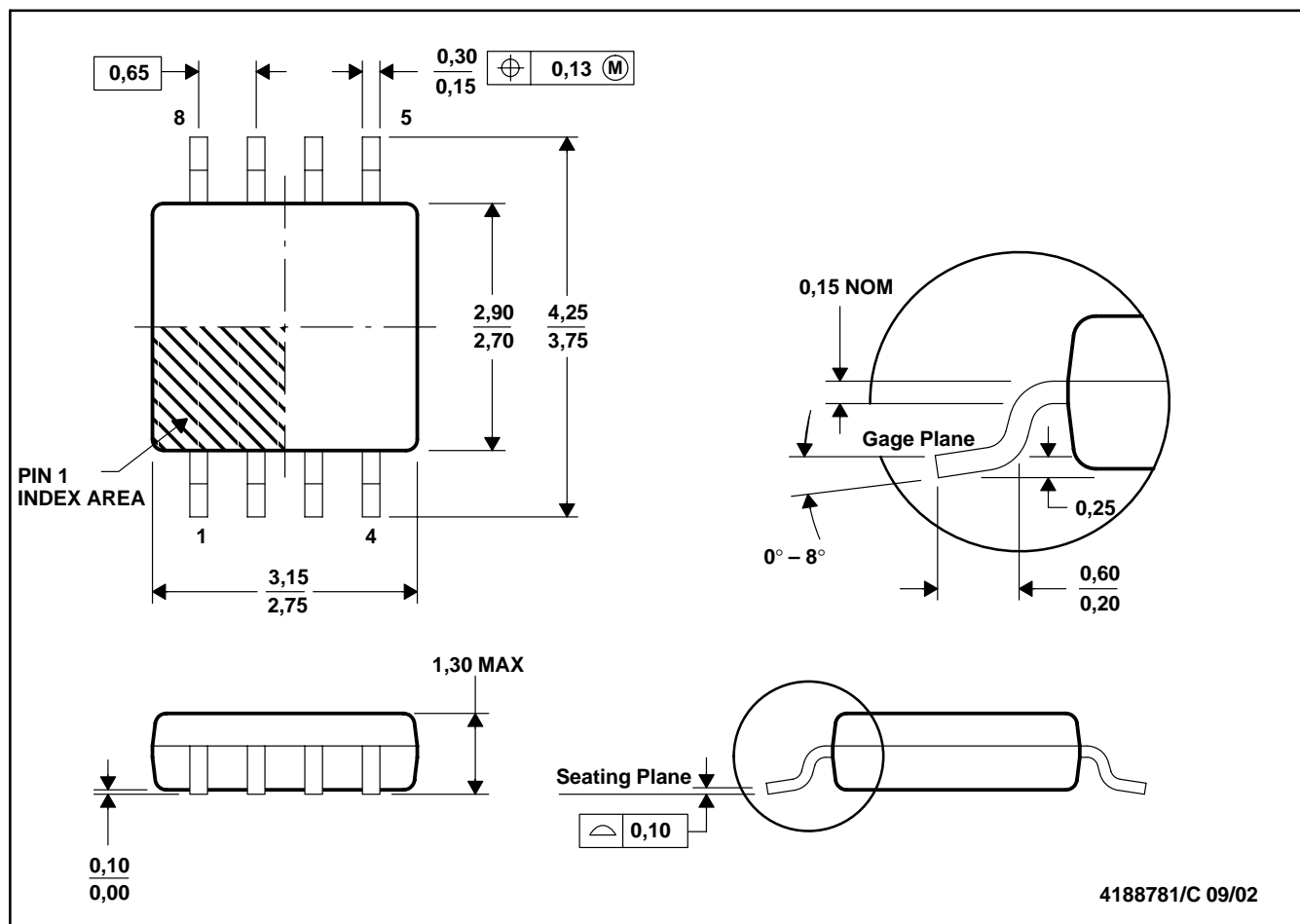
PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DCT (R-PDSO-G8)

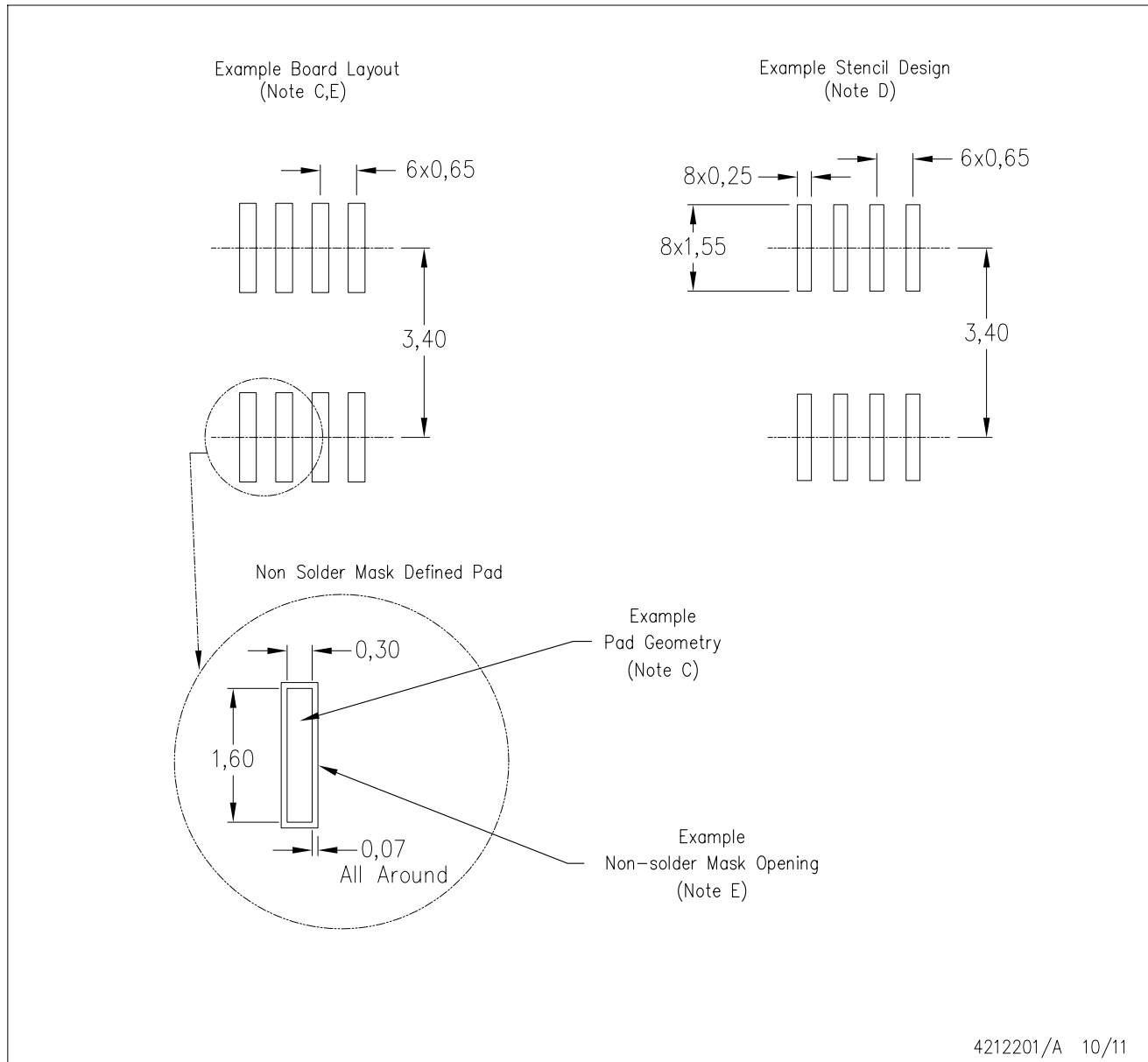
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - Falls within JEDEC MO-187 variation DA.

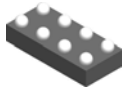
DCT (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

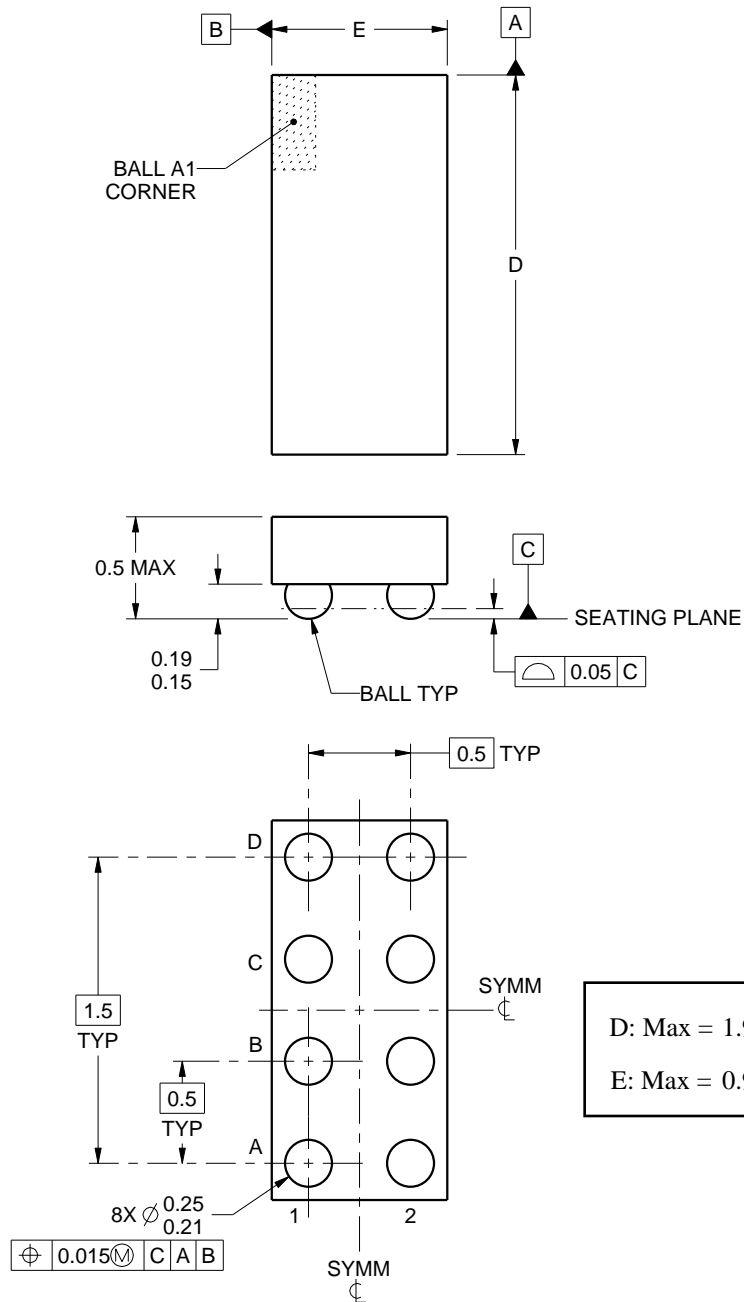
YZP0008



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



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NOTES:

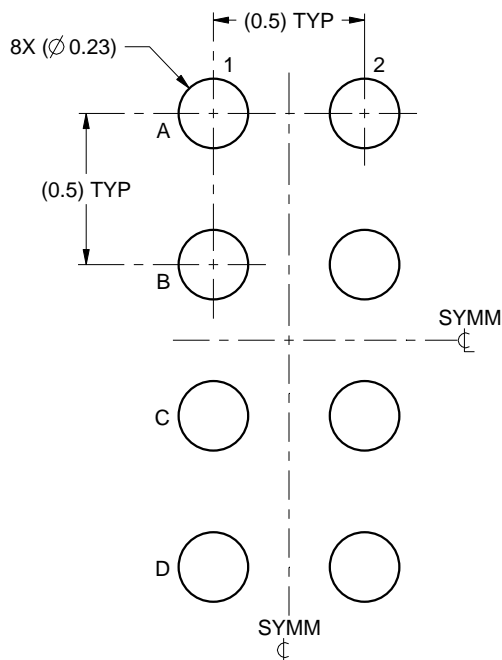
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

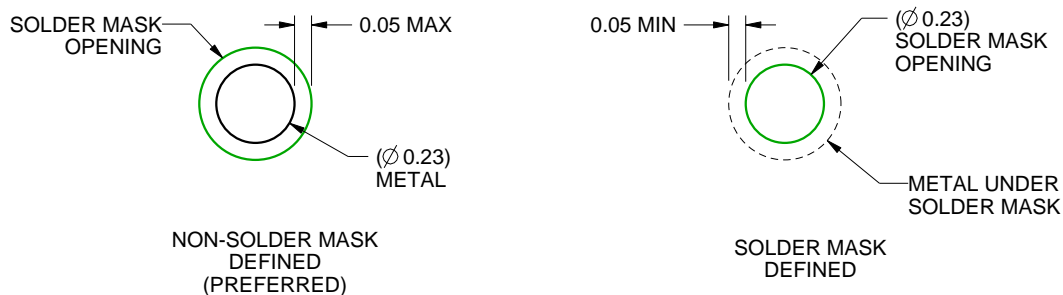
YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

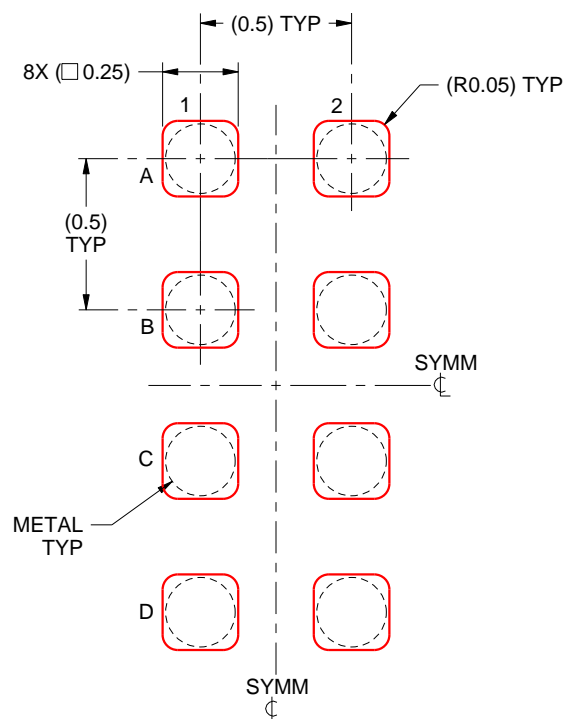
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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