24-Bit Dual-Supply Bus Transceiver with Configurable Voltage Translation And 3-State Outputs

1 Features

- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, All Outputs Are in the High-Impedance State
- Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over Full 1.2-V to 3.6-V Power-Supply Range
- I_{off} Supports Partial-Power-Down Mode Operation
- I/Os Are 4.6-V Tolerant
- Max Data Rates
  - 380 Mbps (1.8-V to 3.3-V Translation)
  - 200 Mbps (<1.8-V to 3.3-V Translation)
  - 200 Mbps (Translate to 2.5 V or 1.8 V)
  - 150 Mbps (Translate to 1.5 V)
  - 100 Mbps (Translate to 1.2 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 8000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Personal Electronics
- Industrial
- Enterprise
- Telecom

3 Description

This 24-bit noninverting bus transceiver uses two separate configurable power-supply rails. The SN74AVC24T245 is optimized to operate with V_{CCA}/V_{CCB} set at 1.4 V to 3.6 V. It is operational with V_{CCA}/V_{CCB} as low as 1.2 V. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVC24T245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the outputs so the buses are effectively isolated.

The SN74AVC24T245 is designed so that the control pins (1DIR, 2DIR, 3DIR, 4DIR, 5DIR, 6DIR, 1 $\overline{OE}$, 2 $\overline{OE}$, 3 $\overline{OE}$, 4 $\overline{OE}$, 5 $\overline{OE}$, and 6 $\overline{OE}$) are supplied by V_{CCA}.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, then both ports are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CCA} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
SN74AVC24T245GRG/ZRG	LFBGA	10.00 mm × 4.50 mm
SN74AVC24T245NMU	nFBGA	10.00 mm × 4.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

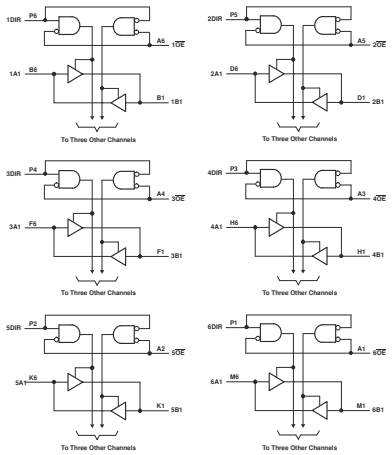


Figure 3-1. Logic Diagram

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2005) to Revision E (August 2020)	Page
• Updated document to current TI data sheet format	1
• Removed Ordering Information table	1
• Added Applications list, Device Information table	1
• Added NMU package option to Device Information table	1
• Added NMU package to pinout drawing	3
• Added ESD Ratings table	6
• Added Thermal Information table	8
• Added NMU package to Thermal Information table	8
• Added Typical Characteristics section	13
• Added Detailed Description section	16
• Added Application and Implementation section	18
• Added Power Supply Recommendations section	21
• Added Layout section	21
• Added Device and Documentation Support section	22
• Added Mechanical, Packaging, and Orderable Information section	22

5 Pin Configuration and Functions

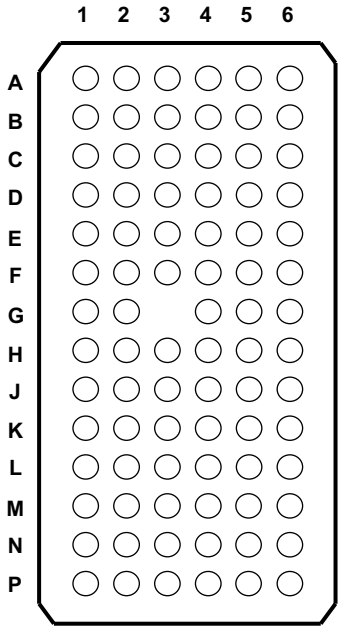


Figure 5-1. GRG/ZRG, NMU Package 83-Pin LFBGA, nFBGA Top View

Table 5-1. Pin Assignments

	1	2	3	4	5	6
A	6 $\overline{OE}$	5 $\overline{OE}$	4 $\overline{OE}$	3 $\overline{OE}$	2 $\overline{OE}$	1 $\overline{OE}$
B	1B1	1B2	V_{CCB}	V_{CCA}	1A2	1A1
C	1B3	1B4	GND	GND	1A4	1A3
D	2B1	2B2	V_{CCB}	V_{CCA}	2A2	2A1
E	2B3	2B4	GND	GND	2A4	2A3
F	3B1	3B2	GND	GND	3A2	3A1
G	3B3	3B4		GND	3A4	3A3
H	4B1	4B2	V_{CCB}	V_{CCA}	4A2	4A1
J	4B3	4B4	GND	GND	4A4	4A3
K	5B1	5B2	GND	GND	5A2	5A1
L	5B3	5B4	V_{CCB}	V_{CCA}	5A4	5A3
M	6B1	6B2	GND	GND	6A2	6A1
N	6B3	6B4	V_{CCB}	V_{CCA}	6A4	6A3
P	6DIR	5DIR	4DIR	3DIR	2DIR	1DIR

Table 5-2. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	6 $\overline{OE}$	Input	Tri-State output-mode enables. Pull $\overline{OE}$ high to place all outputs in Tri-State mode. Referenced to V_{CCA}.
A2	5 $\overline{OE}$	Input	Tri-State output-mode enables. Pull $\overline{OE}$ high to place all outputs in Tri-State mode. Referenced to V_{CCA}.
A3	4 $\overline{OE}$	Input	Tri-State output-mode enables. Pull $\overline{OE}$ high to place all outputs in Tri-State mode. Referenced to V_{CCA}.
A4	3 $\overline{OE}$	Input	Tri-State output-mode enables. Pull $\overline{OE}$ high to place all outputs in Tri-State mode. Referenced to V_{CCA}.

Table 5-2. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
A5	2 $\overline{OE}$	Input	Tri-State output-mode enables. Pull $\overline{OE}$ high to place all outputs in Tri-State mode. Referenced to V_{CCA}.
A6	1 $\overline{OE}$	Input	Tri-State output-mode enables. Pull $\overline{OE}$ high to place all outputs in Tri-State mode. Referenced to V_{CCA}.
B1	1B1	Input/Output	Referenced to V_{CCB}.
B2	1B2	Input/Output	Referenced to V_{CCB}.
B3	V_{CCB}	—	B-port supply voltage. 1.2 V ≤ V_{CCB} ≤ 3.6 V.
B4	V_{CCA}	—	A-port supply voltage. 1.2 V ≤ V_{CCA} ≤ 3.6 V.
B5	1A2	Input/Output	Referenced to V_{CCA}.
B6	1A1	Input/Output	Referenced to V_{CCA}.
C1	1B3	Input/Output	Referenced to V_{CCB}.
C2	1B4	Input/Output	Referenced to V_{CCB}.
C3	GND	—	Ground.
C4	GND	—	Ground.
C5	1A4	Input/Output	Referenced to V_{CCA}.
C6	1A3	Input/Output	Referenced to V_{CCA}.
D1	2B1	Input/Output	Referenced to V_{CCB}.
D2	2B2	Input/Output	Referenced to V_{CCB}
D3	V_{CCB}	—	B-port supply voltage. 1.2 V ≤ V_{CCB} ≤ 3.6 V.
D4	V_{CCA}	—	A-port supply voltage. 1.2 V ≤ V_{CCA} ≤ 3.6 V.
D5	2A2	Input/Output	Referenced to V_{CCA}.
D6	2A1	Input/Output	Referenced to V_{CCA}.
E1	2B3	Input/Output	Referenced to V_{CCB}.
E2	2B4	Input/Output	Referenced to V_{CCB}.
E3	GND	—	Ground.
E4	GND	—	Ground.
E5	2A4	Input/Output	Referenced to V_{CCA}.
E6	2A3	Input/Output	Referenced to V_{CCA}.
F1	3B1	Input/Output	Referenced to V_{CCB}.
F2	3B2	Input/Output	Referenced to V_{CCB}
F3	GND	—	Ground.
F4	GND	—	Ground.
F5	3A2	Input/Output	Referenced to V_{CCA}.
F6	3A1	Input/Output	Referenced to V_{CCA}.
G1	3B3	Input/Output	Referenced to V_{CCB}.
G2	3B4	Input/Output	Referenced to V_{CCB}.
G4	GND	—	Ground.
G5	3A4	Input/Output	Referenced to V_{CCA}.
G6	3A3	Input/Output	Referenced to V_{CCA}.
H1	4B1	Input/Output	Referenced to V_{CCB}.
H2	4B2	Input/Output	Referenced to V_{CCB}.
H3	V_{CCB}	—	B-port supply voltage. 1.2 V ≤ V_{CCB} ≤ 3.6 V.
H4	V_{CCA}	—	A-port supply voltage. 1.2 V ≤ V_{CCA} ≤ 3.6 V.
H5	4A2	Input/Output	Referenced to V_{CCA}.
H6	4A1	Input/Output	Referenced to V_{CCA}.

Table 5-2. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
J1	4B3	Input/Output	Referenced to V_{CCB}.
J2	4B4	Input/Output	Referenced to V_{CCB}.
J3	GND	—	Ground.
J4	GND	—	Ground.
J5	4A4	Input/Output	Referenced to V_{CCA}.
J6	4A3	Input/Output	Referenced to V_{CCA}.
K1	5B1	Input/Output	Referenced to V_{CCB}.
K2	5B2	Input/Output	Referenced to V_{CCB}.
K3	GND	—	Ground.
K4	GND	—	Ground.
K5	5A2	Input/Output	Referenced to V_{CCA}.
K6	5A1	Input/Output	Referenced to V_{CCA}.
L1	5B3	Input/Output	Referenced to V_{CCB}.
L2	5B4	Input/Output	Referenced to V_{CCB}.
L3	V_{CCB}	—	B-port supply voltage. 1.2 V ≤ V_{CCB} ≤ 3.6 V.
L4	V_{CCA}	—	A-port supply voltage. 1.2 V ≤ V_{CCA} ≤ 3.6 V.
L5	5A4	Input/Output	Referenced to V_{CCA}.
L6	5A3	Input/Output	Referenced to V_{CCA}.
M1	6B1	Input/Output	Referenced to V_{CCB}.
M2	6B2	Input/Output	Referenced to V_{CCB}.
M3	GND	—	Ground.
M4	GND	—	Ground.
M5	6A2	Input/Output	Referenced to V_{CCA}.
M6	6A1	Input/Output	Referenced to V_{CCA}.
N1	6B3	Input/Output	Referenced to V_{CCB}.
N2	6B4	Input/Output	Referenced to V_{CCB}.
N3	V_{CCB}	—	B-port supply voltage. 1.2 V ≤ V_{CCB} ≤ 3.6 V.
N4	V_{CCA}	—	A-port supply voltage. 1.2 V ≤ V_{CCA} ≤ 3.6 V.
N5	6A4	Input/Output	Referenced to V_{CCA}.
N6	6A3	Input/Output	Referenced to V_{CCA}.
P1	6DIR	Input	Direction-control signal. Referenced to V_{CCA}.
P2	5DIR	Input	Direction-control signal. Referenced to V_{CCA}.
P3	4DIR	Input	Direction-control signal. Referenced to V_{CCA}.
P4	3DIR	Input	Direction-control signal. Referenced to V_{CCA}.
P5	2DIR	Input	Direction-control signal. Referenced to V_{CCA}.
P6	1DIR	Input	Direction-control signal. Referenced to V_{CCA}.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage range		–0.5	4.6	V
V_I	Input voltge range(2)	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage range applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CCA}, V_{CCB}, and GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The output positive-voltage rating may be exceeded up to 4.6-V maximum if the output current rating is observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±8000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

6.3 Recommended Operating Conditions

		(1) (2) (3)	V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}	Supply voltage				1.2	3.6	V
V_{IH}	High-level input voltage	Data inputs(4)	1.2 V to 1.95 V		V_{CCI} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Data inputs(4)	1.2 V to 1.95 V			V_{CCI} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA})(5)	1.2 V to 1.95 V		V_{CCA} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA})(5)	1.2 V to 1.95 V			V_{CCA} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.2 V		–3	mA
				1.4 V to 1.6 V		–6	
				1.65 V to 1.95 V		–8	
				2.3 V to 2.7 V		–9	
				3 V to 3.6 V		–12	
I_{OL}	Low-level output current			1.2 V		3	mA
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
Δt/Δv	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				–40	85	°C

(1) V_{CCI} is the V_{CC} associated with the data input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V.
(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V.

6.4 Thermal Information

THERMAL METRIC[1]		SN74AVC24T245			UNIT
		GRG	ZRG	NMU	
		83	83	83	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.1	38.1	44.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.8	22.8	24.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.0	17.0	29.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.44	0.44	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.9	16.9	29.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)(2) (3)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to 85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
V_{OH}		I_{OH} = –100 µA	$V_I = V_{IH}$	1.2 V to 3.6 V	1.2 V to 3.6 V				V_{CCO} – 0.2		V
		I_{OH} = –3 mA		1.2 V	1.2 V		0.95				
		I_{OH} = –6 mA		1.4 V	1.4 V				1.05		
		I_{OH} = –8 mA		1.65 V	1.65 V				1.2		
		I_{OH} = –9 mA		2.3 V	2.3 V				1.75		
		I_{OH} = –12 m		3 V	3 V				2.3		
V_{OL}		I_{OL} = 100 µA	$V_I = V_{IL}$	1.2 V to 3.6 V	1.2 V to 3.6 V					0.2	V
		I_{OL} = 3 mA		1.2 V	1.2 V		0.15				
		I_{OL} = 6 mA		1.4 V	1.4 V					0.35	
		I_{OL} = 8 mA		1.65 V	1.65 V					0.45	
		I_{OL} = 9 mA		2.3 V	2.3 V					0.55	
		I_{OL} = 12 mA		3 V	3 V					0.7	
I_I	Control inputs	$V_I = V_{CCA}$ or GND		1.2 V to 3.6 V	1.2 V to 3.6 V		±0.025	±0.25		±1	µA
I_{off}	A or B port	V_I or V_O = 0 to 3.6 V		0 V	0 to 3.6 V		±0.1	±2.5		±5	µA
	A or B port			0 to 3.6 V	0 V		±0.1	±2.5		±5	
I_{OZ} (1)	A or B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE} = V_{IH}$		3.6 V	3.6 V		±0.5	±2.5		±5	µA
I_{CCA}		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V					40	µA
				0 V	3.6 V					–5	
				3.6 V	0 V					40	
I_{CCB}		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V					40	µA
				0 V	3.6 V					40	
				3.6 V	0 V					–5	
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V					75	µA
C_i	Control inputs	V_I = 3.3 V or GND		3.3 V	3.3 V		3.5				pF
C_{io}	A or B port	V_O = 3.3 V or GND		3.3 V	3.3 V		7				pF

(1) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) V_{CCI} is the V_{CC} associated with the input port.

6.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 1.2 V (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V	V_{CCB} = 1.8 V	V_{CCB} = 2.5 V	V_{CCB} = 3.3 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
t_{PLH}	A	B	4.1	3.3	3	2.8	3.2	ns
t_{PHL}			4.1	3.3	3	2.8	3.2	
t_{PLH}	B	A	4.4	4	3.8	3.6	3.5	ns
t_{PHL}			4.4	4	3.8	3.6	3.5	
t_{PZH}	$\overline{OE}$	A	6.4	6.4	6.4	6.4	6.4	ns
t_{PZL}			6.4	6.4	6.4	6.4	6.4	
t_{PZH}	$\overline{OE}$	B	6	4.6	4	3.4	3.2	ns
t_{PZL}			6	4.6	4	3.4	3.2	
t_{PHZ}	$\overline{OE}$	A	6.6	6.6	6.6	6.6	6.8	ns
t_{PLZ}			6.6	6.6	6.6	6.6	6.8	
t_{PHZ}	$\overline{OE}$	B	6	4.9	4.9	4.2	5.3	ns
t_{PLZ}			6	4.9	4.9	4.2	5.3	

6.7 Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3.6	0.5	6.2	0.5	5.2	0.5	4.1	0.5	3.7	ns
t_{PHL}			3.6	0.5	6.2	0.5	5.2	0.5	4.1	0.5	3.7	
t_{PLH}	B	A	3.3	0.5	6.2	0.5	5.9	0.5	5.6	0.5	5.5	ns
t_{PHL}			3.3	0.5	6.2	0.5	5.9	0.5	5.6	0.5	5.5	
t_{PZH}	$\overline{OE}$	A	4.3	1	10.1	1	10.1	1	10.1	1	10.1	ns
t_{PZL}			4.3	1	10.1	1	10.1	1	10.1	1	10.1	
t_{PZH}	$\overline{OE}$	B	5.6	1	10.1	0.5	8.1	0.5	5.9	0.5	5.2	ns
t_{PZL}			5.6	1	10.1	0.5	8.1	0.5	5.9	0.5	5.2	
t_{PHZ}	$\overline{OE}$	A	4.5	1.5	9.1	1.5	9.1	1.5	9.1	1.5	9.1	ns
t_{PLZ}			4.5	1.5	9.1	1.5	9.1	1.5	9.1	1.5	9.1	
t_{PHZ}	$\overline{OE}$	B	5.5	1.5	8.7	1.5	7.5	1	6.5	1	6.3	ns
t_{PLZ}			5.5	1.5	8.7	1.5	7.5	1	6.5	1	6.3	

6.8 Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3.4	0.5	5.9	0.5	4.8	0.5	3.7	0.5	3.3	ns
t_{PHL}			3.4	0.5	5.9	0.5	4.8	0.5	3.7	0.5	3.3	
t_{PLH}	B	A	3	0.5	5.2	0.5	4.8	0.5	4.5	0.5	4.4	ns
t_{PHL}			3	0.5	5.2	0.5	4.8	0.5	4.5	0.5	4.4	
t_{PZH}	$\overline{OE}$	A	3.4	1	7.8	1	7.8	1	7.8	1	7.8	ns
t_{PZL}			3.4	1	7.8	1	7.8	1	7.8	1	7.8	
t_{PZH}	$\overline{OE}$	B	5.4	1	9.2	0.5	7.4	0.5	5.3	0.5	4.5	ns
t_{PZL}			5.4	1	9.2	0.5	7.4	0.5	5.3	0.5	4.5	
t_{PHZ}	$\overline{OE}$	A	4.2	1.5	7.7	1.5	7.7	1.5	7.7	1.5	7.7	ns
t_{PLZ}			4.2	1.5	7.7	1.5	7.7	1.5	7.7	1.5	7.7	
t_{PHZ}	$\overline{OE}$	B	5.2	1.5	8.4	1.5	7.1	1	5.9	1	5.7	ns
t_{PLZ}			5.2	1.5	8.4	1.5	7.1	1	5.9	1	5.7	

6.9 Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3.2	0.5	5.6	0.5	4.5	0.5	3.3	0.5	2.8	ns
t_{PHL}			3.2	0.5	5.6	0.5	4.5	0.5	3.3	0.5	2.8	
t_{PLH}	B	A	2.6	0.5	4.1	0.5	3.7	0.5	3.3	0.5	3.2	ns
t_{PHL}			2.6	0.5	4.1	0.5	3.7	0.5	3.3	0.5	3.2	
t_{PZH}	$\overline{OE}$	A	2.5	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	ns
t_{PZL}			2.5	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	
t_{PZH}	$\overline{OE}$	B	5.2	0.5	9.4	0.5	7.3	0.5	5.1	0.5	4.5	ns
t_{PZL}			5.2	0.5	9.4	0.5	7.3	0.5	5.1	0.5	4.5	
t_{PHZ}	$\overline{OE}$	A	3	1	6.1	1	6.1	1	6.1	1	6.1	ns
t_{PLZ}			3	1	6.1	1	6.1	1	6.1	1	6.1	
t_{PHZ}	$\overline{OE}$	B	5	1	7.9	1	6.6	1	6.1	1	5.2	ns
t_{PLZ}			5	1	7.9	1	6.6	1	6.1	1	5.2	

6.10 Switching Charactertistics

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3.2	0.5	5.5	0.5	4.4	0.5	3.2	0.5	2.7	ns
t_{PHL}			3.2	0.5	5.5	0.5	4.4	0.5	3.2	0.5	2.7	
t_{PLH}	B	A	2.8	0.5	3.7	0.5	3.3	0.5	2.8	0.5	2.7	ns
t_{PHL}			2.8	0.5	3.7	0.5	3.3	0.5	2.8	0.5	2.7	
t_{PZH}	$\overline{OE}$	A	2.2	0.5	4.3	0.5	4.2	0.5	4.1	0.5	4	ns
t_{PZL}			2.2	0.5	4.3	0.5	4.2	0.5	4.1	0.5	4	
t_{PZH}	$\overline{OE}$	B	5.1	0.5	9.3	0.5	7.2	0.5	4.9	0.5	4	ns
t_{PZL}			5.1	0.5	9.3	0.5	7.2	0.5	4.9	0.5	4	
t_{PHZ}	$\overline{OE}$	A	3.4	0.5	5	0.5	5	0.5	5	0.5	5	ns
t_{PLZ}			3.4	0.5	5	0.5	5	0.5	5	0.5	5	
t_{PHZ}	$\overline{OE}$	B	4.9	1	7.7	1	6.5	1	5.2	0.5	5	ns
t_{PLZ}			4.9	1	7.7	1	6.5	1	5.2	0.5	5	

6.11 Operating Characteristics

V_{CCA} and V_{CCB} = 3.3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.5 V	V_{CCA} = V_{CCB} = 1.2 V	V_{CCA} = V_{CCB} = 1.8 V	V_{CCA} = V_{CCB} = 2.5 V	V_{CCA} = V_{CCB} = 3.3 V	UNIT
				TYP	TYP	TYP	TYP	TYP	
C_{pdA} (1)	A to B	Outputs enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	1	1	1	2	2	pF
		Outputs disabled		1	1	1	1	2	
	B to A	Outputs enabled		19	19	20	21	22	
		Outputs disabled		1	1	1	1	1	
C_{pdB} (1)	A to B	Outputs enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	19	19	20	21	22	pF
		Outputs disabled		1	1	1	1	1	
	B to A	Outputs enabled		1	1	1	2	2	
		Outputs disabled		1	1	1	1	2	

(1) Power dissipation capacitance per transceiver

6.12 Typical Characteristics

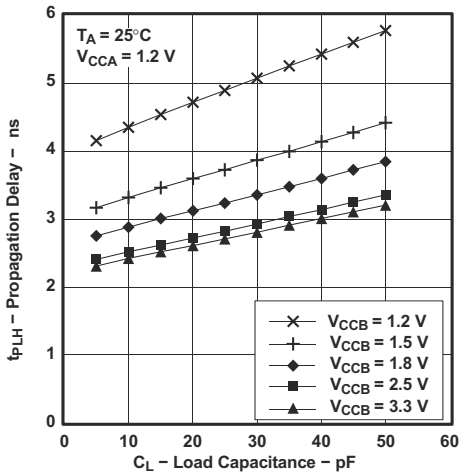


Figure 6-1. Propagation Delay vs Load Capacitance

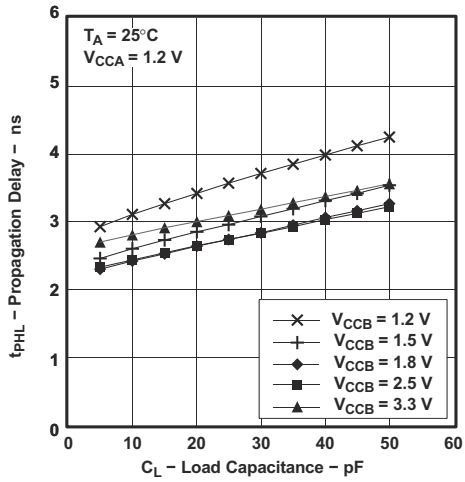


Figure 6-2. Propagation Delay vs Load Capacitance

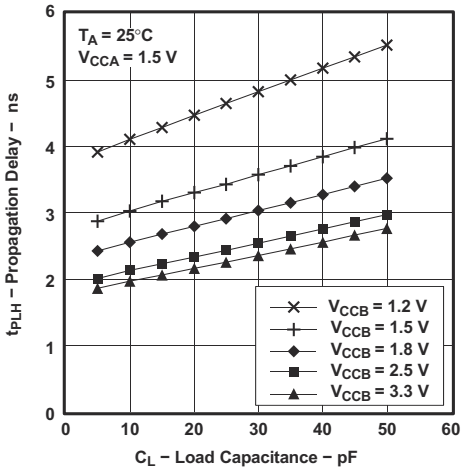


Figure 6-3. Typical Propagation Delay t_{PLH} (A to B) vs Load Capacitance

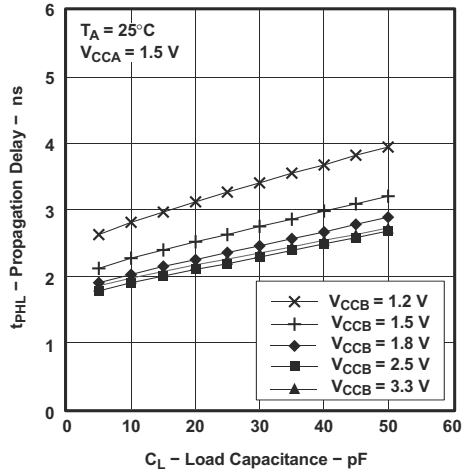


Figure 6-4. Typical Propagation Delay t_{PLH} (A to B) vs Load Capacitance

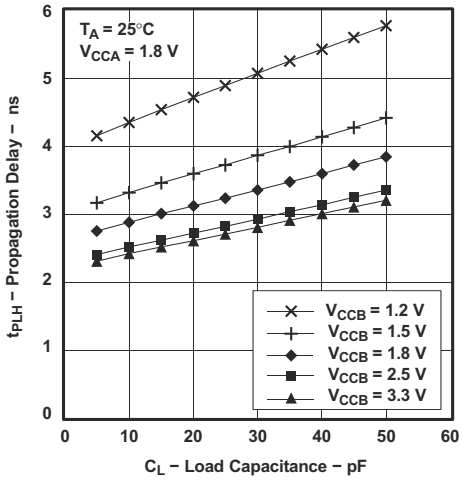


Figure 6-5. Typical Propagation Delay t_{PLH} (A to B) vs Load Capacitance

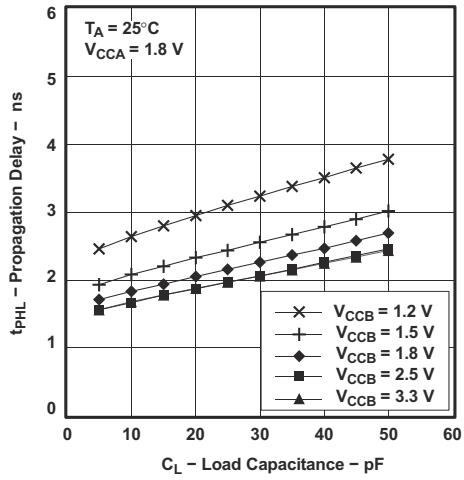


Figure 6-6. Typical Propagation Delay t_{PLH} (A to B) vs Load Capacitance

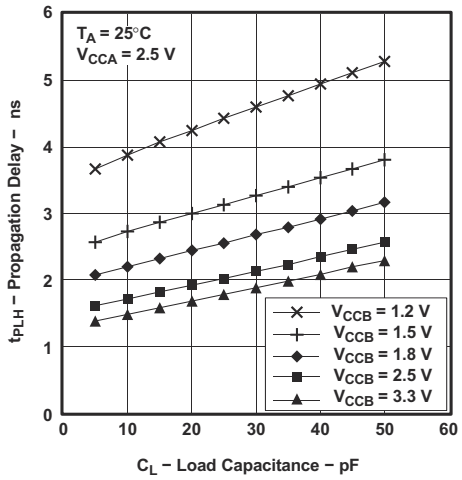


Figure 6-7. Typical Propagation Delay t_{PLH} (A to B) vs Load Capacitance

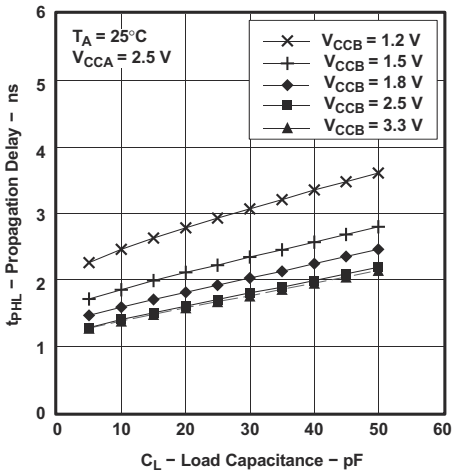


Figure 6-8. Typical Propagation Delay t_{PLH} (A to B) vs Load Capacitance

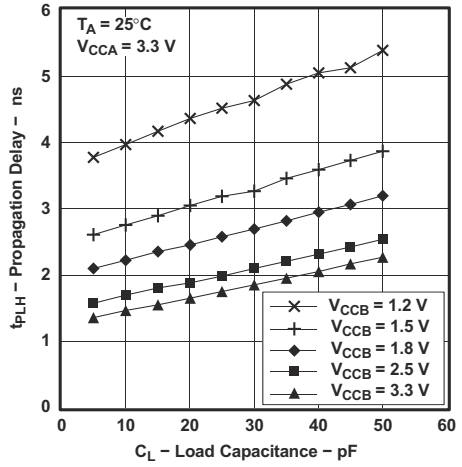


Figure 6-9. Typical Propagation Delay t_{PLH} (A to B) vs Load Capacitance

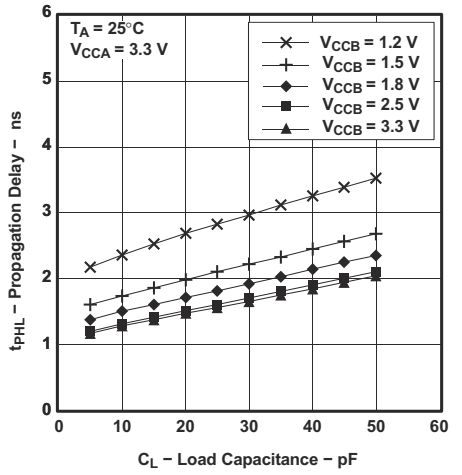
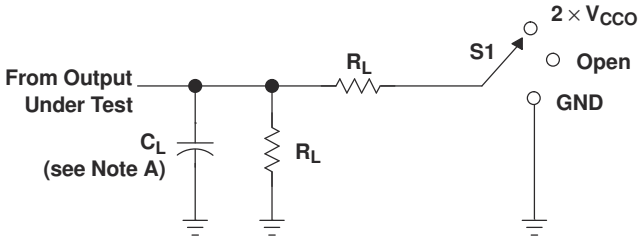


Figure 6-10. Propagation Delay vs Load Capacitance

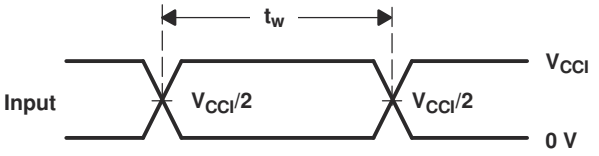
7 Parameter Measurement Information



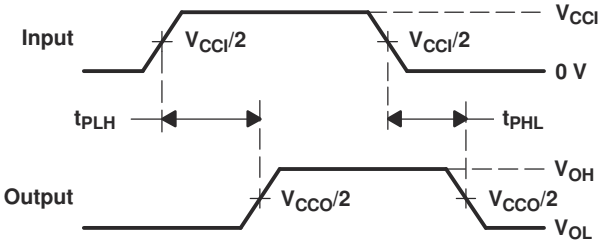
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

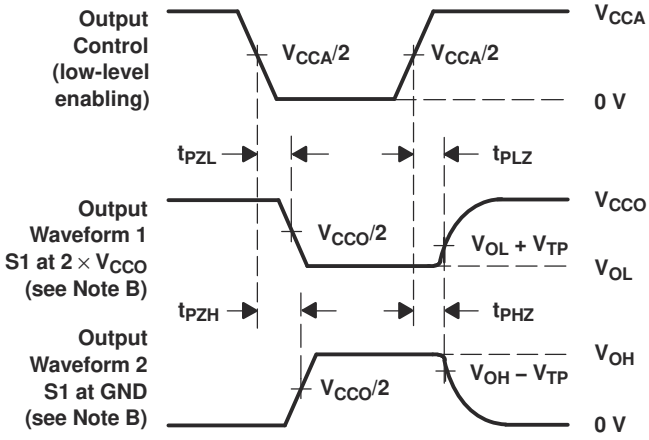
V_{CCO}	C_L	R_L	V_{TP}
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.

Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

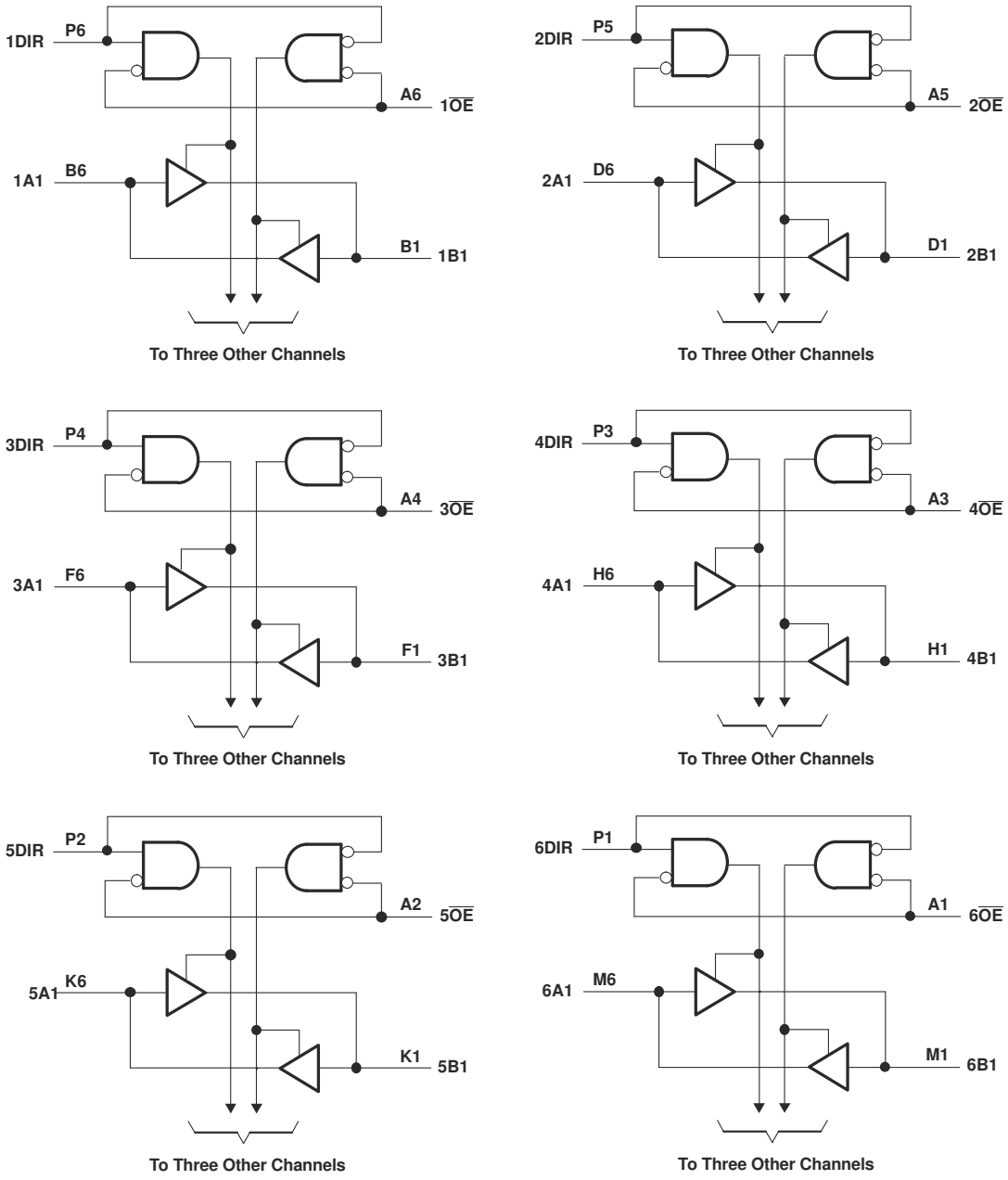
8.1 Overview

The SN74AVC24T245 is a 16-bit, dual-supply noninverting bidirectional voltage level translation. Pins A and control pins (DIR and $\overline{OE}$) are supported by V_{CCA} and pins B are supported by V_{CCB}. The A port can accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.2 V to 3.6 V. A high on DIR allows data transmission from A to B and a low on DIR allows data transmission from B to A when $\overline{OE}$ is set to low. When $\overline{OE}$ is set to high, both A and B are in the high-impedance state.

This device is fully specified for partial-power-down applications using off output current (I_{off}).

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, both ports are put in a high-impedance state.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range

Both V_{CCA} and V_{CCB} can be supplied at any voltage from 1.2 V to 3.6 V which makes the device suitable for translating between any of the low voltage nodes (1.2 V, 1.8 V, 2.5 V, and 3.3 V).

8.3.2 Partial-Power-Down Mode Operation

This device is fully specified for partial-power-down applications using off output current (I_{off}). The I_{off} circuitry will prevent backflow current by disabling I/O output circuits when device is in partial power-down mode.

8.3.3 V_{CC} Isolation

The V_{CC} isolation feature ensures that if either V_{CCA} or V_{CCB} are at GND, both ports will be in a high-impedance state (I_{OZ}). This prevents false logic levels from being presented to either bus.

8.4 Device Functional Modes

The SN74AVC24T245 is a voltage level translator that can operate from 1.2 V to 3.6 V (V_{CCA}) and 1.2 V to 3.6 V (V_{CCB}). The signal translation between 1.2 V and 3.6 V requires direction control and output enable control. When $\overline{OE}$ is low and DIR is high, data transmission is from A to B. When $\overline{OE}$ is low and DIR is low, data transmission is from B to A. When $\overline{OE}$ is high, both output ports will be high-impedance.

Table 8-1. Function Table (Each 4-Bit Section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74AVC24T245 device can be used in level-shifting applications for interfacing devices and addressing mixed voltage incompatibility. The SN74AVC24T245 device is ideal for data transmission where direction is different for each channel.

9.2 EnableTimes

Calculate the enable times for the SN74AVC24T245 using the following formulas:

$$t_{PZH} \text{ (DIR to A)} = t_{PLZ} \text{ (DIR to B)} + t_{PLH} \text{ (B to A)} \quad (1)$$

$$t_{PZL} \text{ (DIR to A)} = t_{PHZ} \text{ (DIR to B)} + t_{PHL} \text{ (B to A)} \quad (2)$$

$$t_{PZH} \text{ (DIR to B)} = t_{PLZ} \text{ (DIR to A)} + t_{PLH} \text{ (A to B)} \quad (3)$$

$$t_{PZL} \text{ (DIR to B)} = t_{PHZ} \text{ (DIR to A)} + t_{PHL} \text{ (A to B)} \quad (4)$$

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74AVC24T245 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

9.3 Typical Application

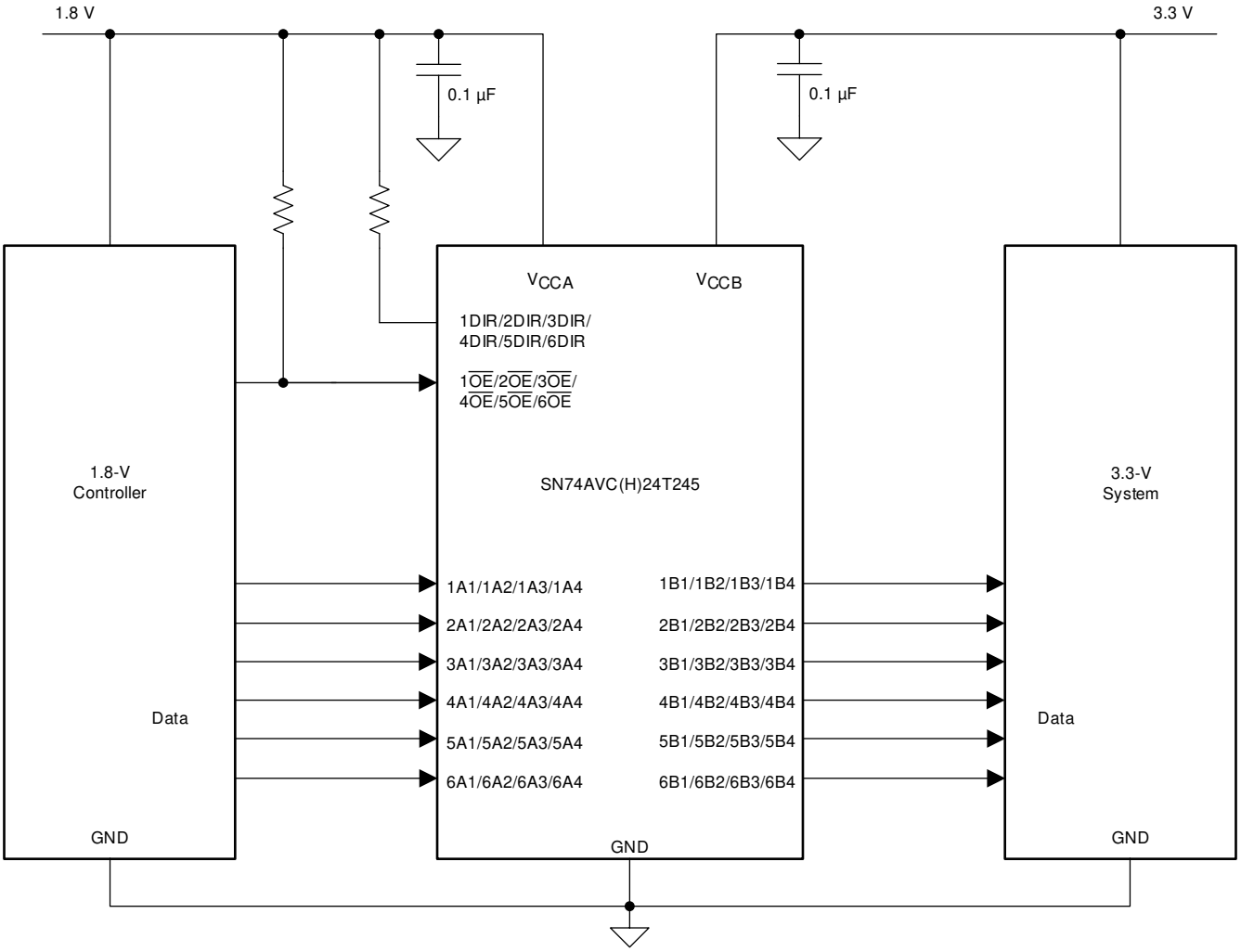


Figure 9-1. Application Schematic

9.3.1 Design Requirements

This device uses drivers which are enabled depending on the state of the DIR pin. The designer must know the intended flow of data and take care not to violate any of the high or low logic levels. Unused data inputs must not be floating, as this can cause excessive internal leakage on the input CMOS structure. Tie any unused input and output ports directly to ground.

For this design example, use the parameters listed in the *Electrical Characteristics*.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2 V to 3.6 V
Output voltage range	1.2 V to 3.6 V

9.3.2 Detailed Design Procedure

To begin the design process, determine the following:

9.3.2.1 Input Voltage Ranges

Use the supply voltage of the device that is driving the SN74AVC24T245 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.

9.3.2.2 Output Voltage Range

Use the supply voltage of the device that the SN74AVC24T245 device is driving to determine the output voltage range.

9.3.3 Application Curve

/

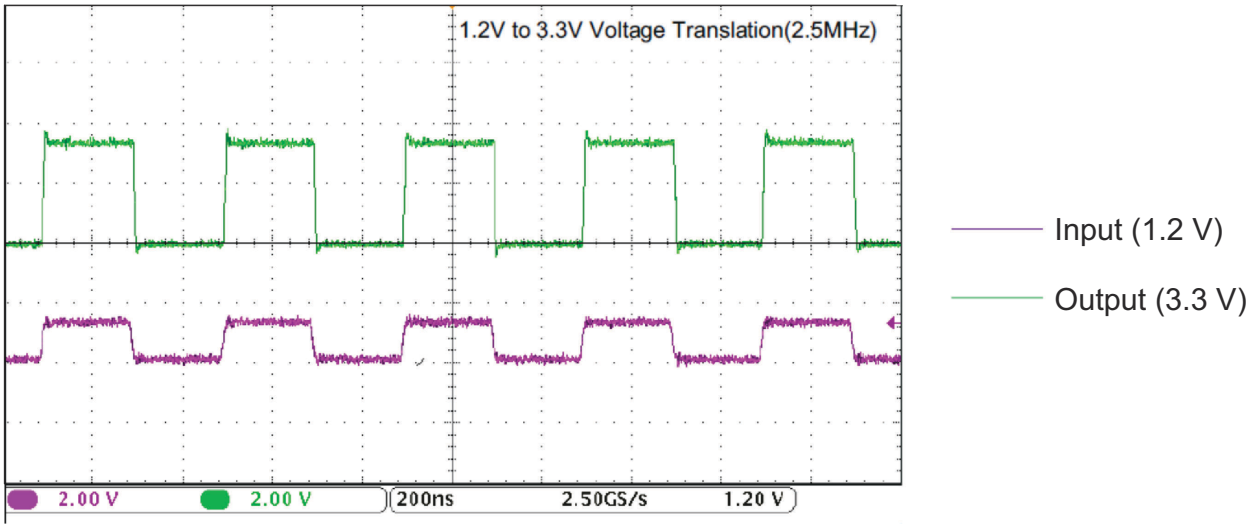


Figure 9-2. Translation Up (1.2 V to 3.3 V) at 2.5 MHz

10 Power Supply Recommendations

The SN74AVC24T245 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. VCCA accepts any supply voltage from 1.2 V to 3.6 V and V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. The A port and B port are designed to track V_{CCA} and V_{CCB}, respectively, allowing for low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V and 3.3-V voltage nodes.

The output-enable $\overline{OE}$ input circuit is designed so that it is supplied by V_{CCA} and when the $\overline{OE}$ input is high, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the $\overline{OE}$ input pin must be tied to V_{CCA} through a pullup resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pullup resistor to V_{CCA} is determined by the current-sinking capability of the driver.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit-board layout guidelines is recommended.

- Bypass capacitors must be used on power supplies.
- Short trace lengths must be used to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals, depending on the system requirements.

11.2 Layout Example

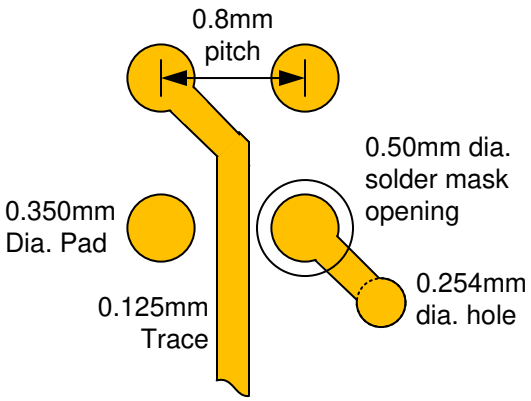


Figure 11-1. BGA Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.2 Related Documentation

For related documentation, see the following:

http://www.ti.com/lit/an/scea014/scea014.pdf

12.3 Trademarks

All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AVC24T245GRGR	LIFEBUY	BGA MICROSTAR JUNIOR	GRG	83	1000	TBD	SNPB	Level-1-240C-UNLIM	-40 to 85	WH245	
SN74AVC24T245NMUR	ACTIVE	NFBGA	NMU	83	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	2CPW	Samples
SN74AVC24T245ZRGR	ACTIVE	BGA MICROSTAR JUNIOR	ZRG	83	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	WH245	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

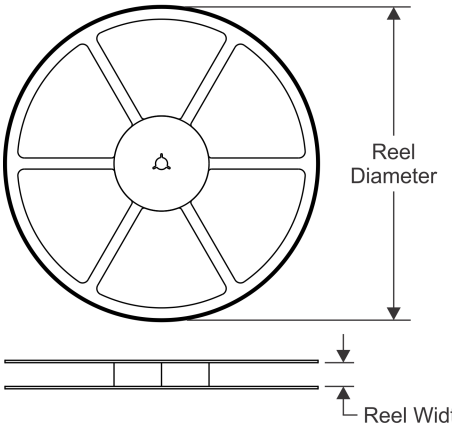
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

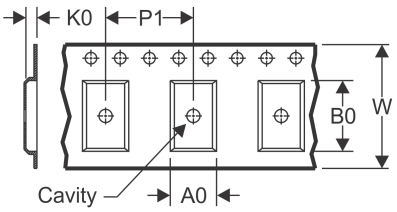
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

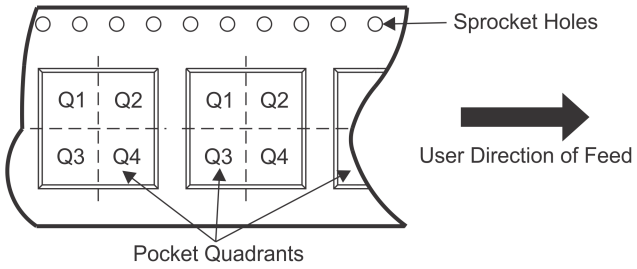


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

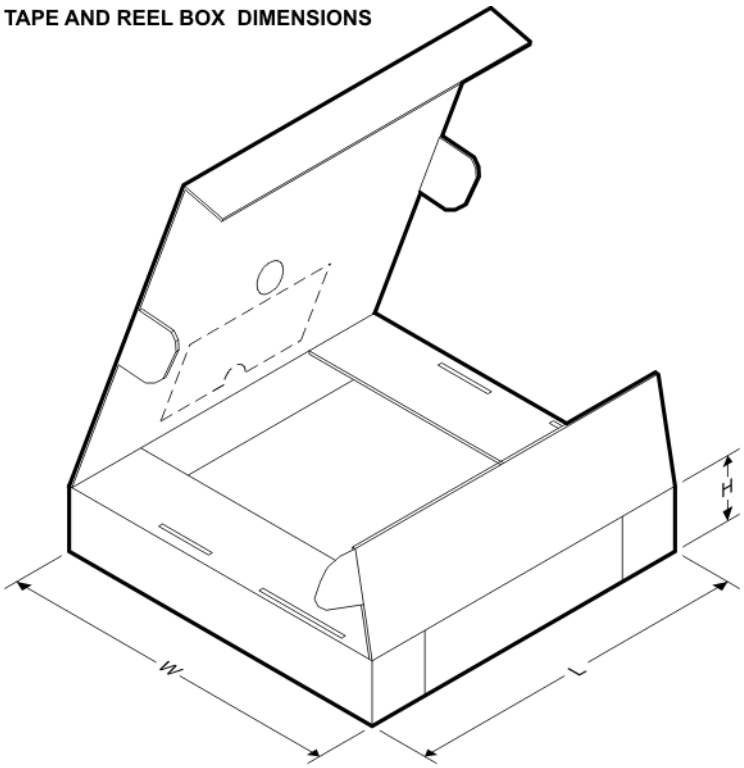
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC24T245GRGR	BGA MICROSTAR JUNIOR	GRG	83	1000	330.0	24.4	4.8	10.3	1.8	8.0	24.0	Q1
SN74AVC24T245ZRGR	BGA MICROSTAR JUNIOR	ZRG	83	1000	330.0	24.4	4.8	10.3	1.8	8.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

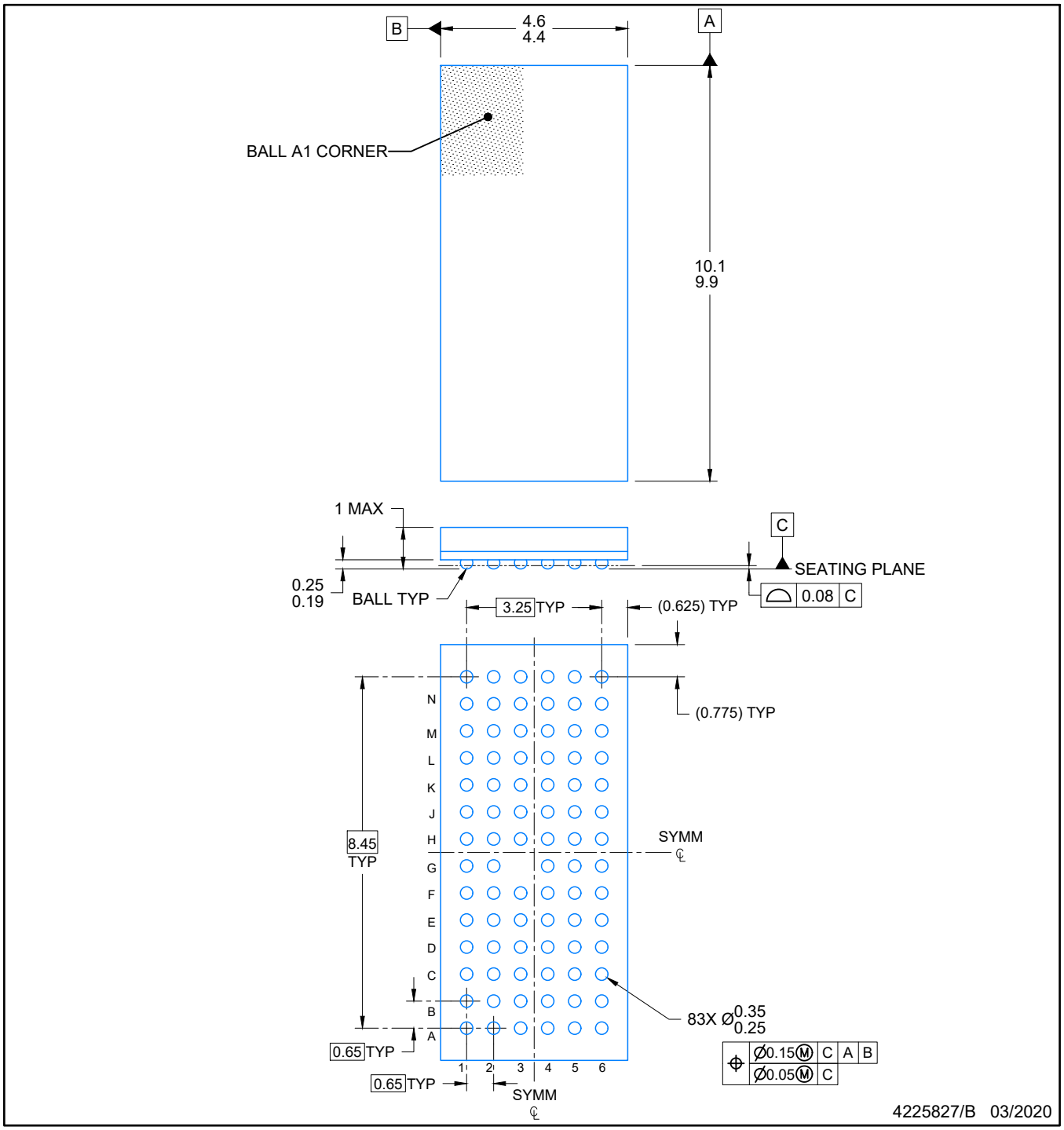
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC24T245GRGR	BGA MICROSTAR JUNIOR	GRG	83	1000	350.0	350.0	43.0
SN74AVC24T245ZRGR	BGA MICROSTAR JUNIOR	ZRG	83	1000	350.0	350.0	43.0

PACKAGE OUTLINE

NMU0083A

NFBGA - 1 mm max height

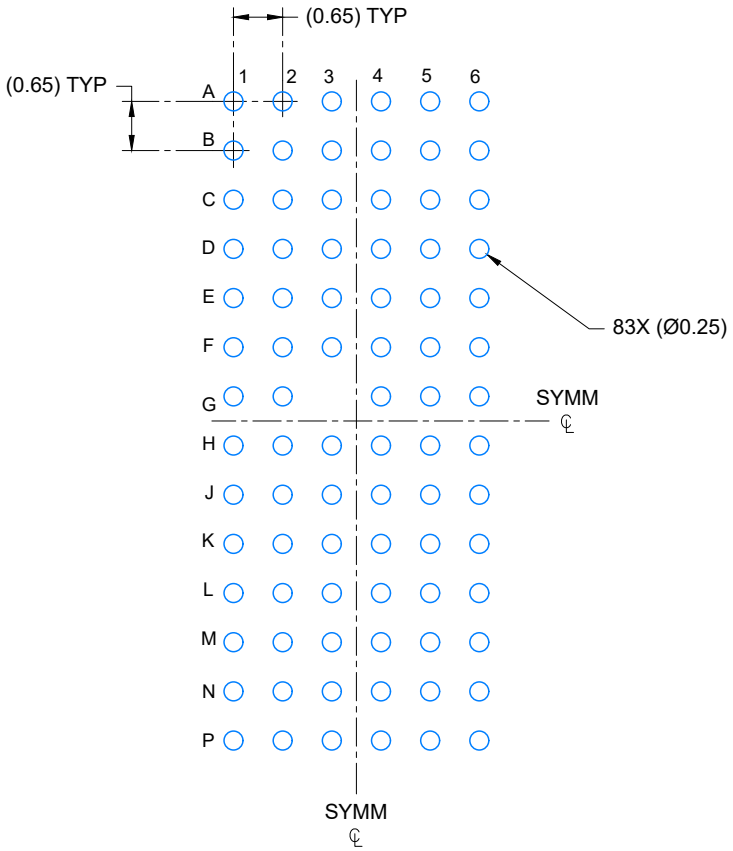
PLASTIC BALL GRID ARRAY



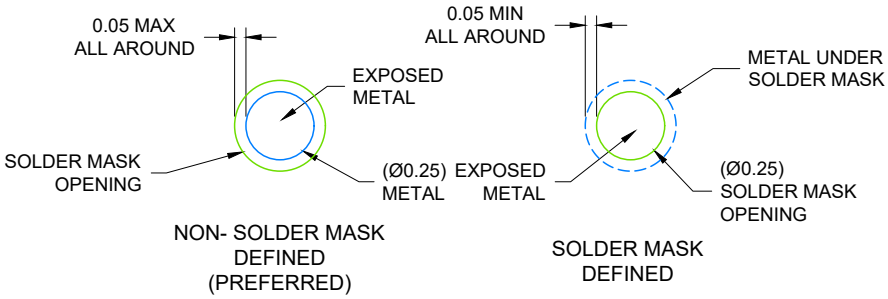
NOTES:

NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE: 10X

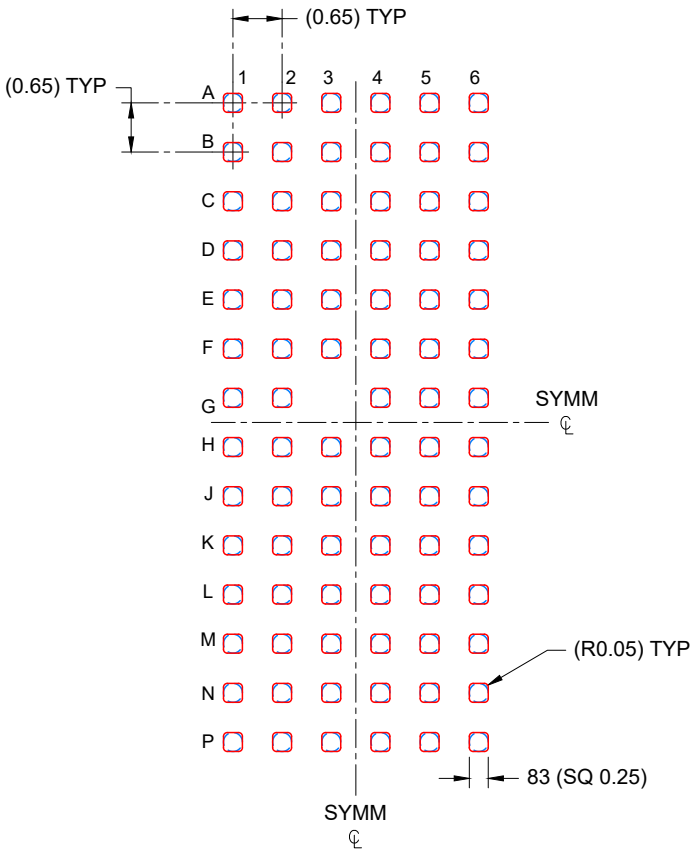


SOLDER MASK DETAILS
NOT TO SCALE

4225827/B 03/2020

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).



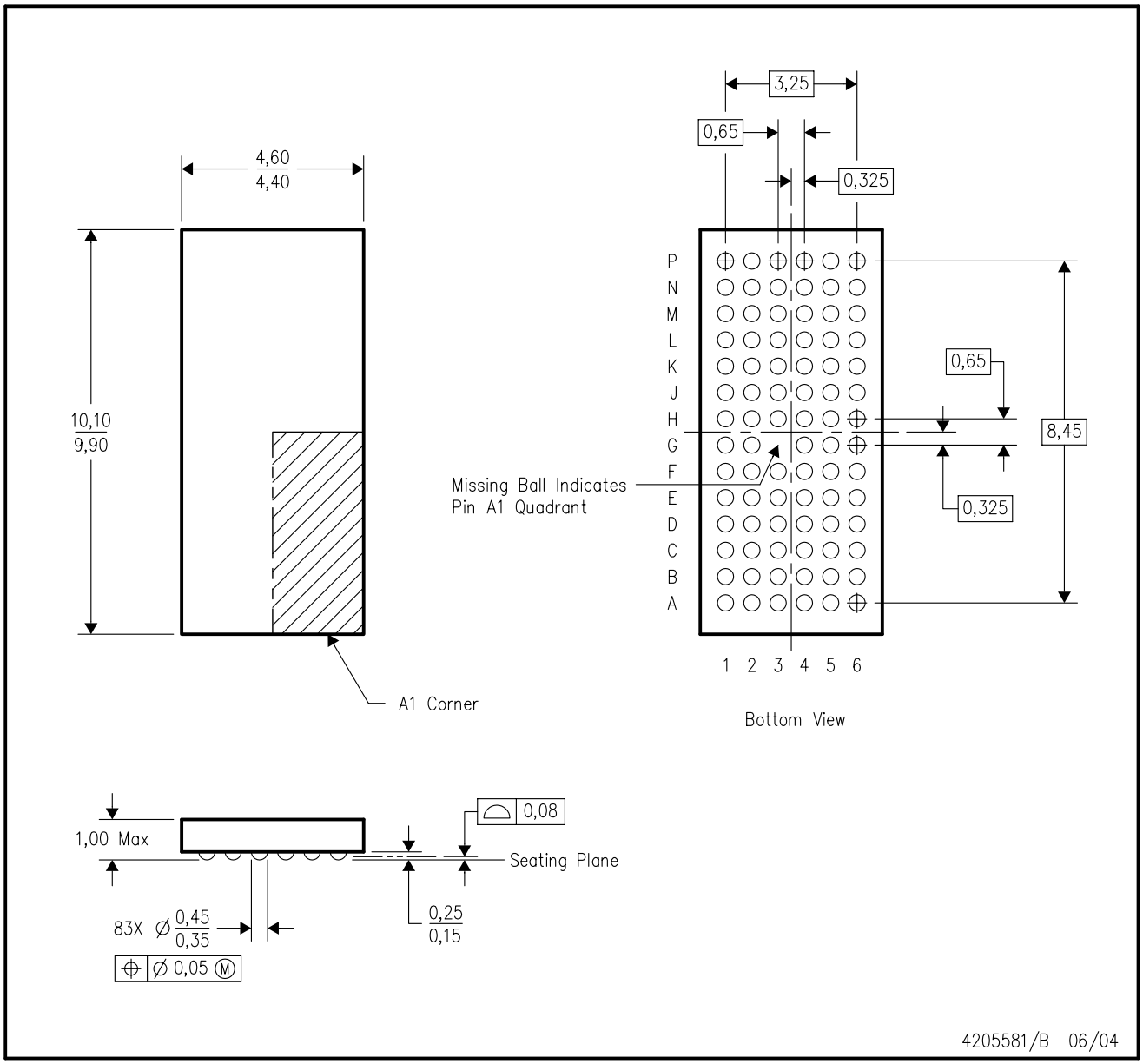
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4225827/B 03/2020

NOTES: (continued)

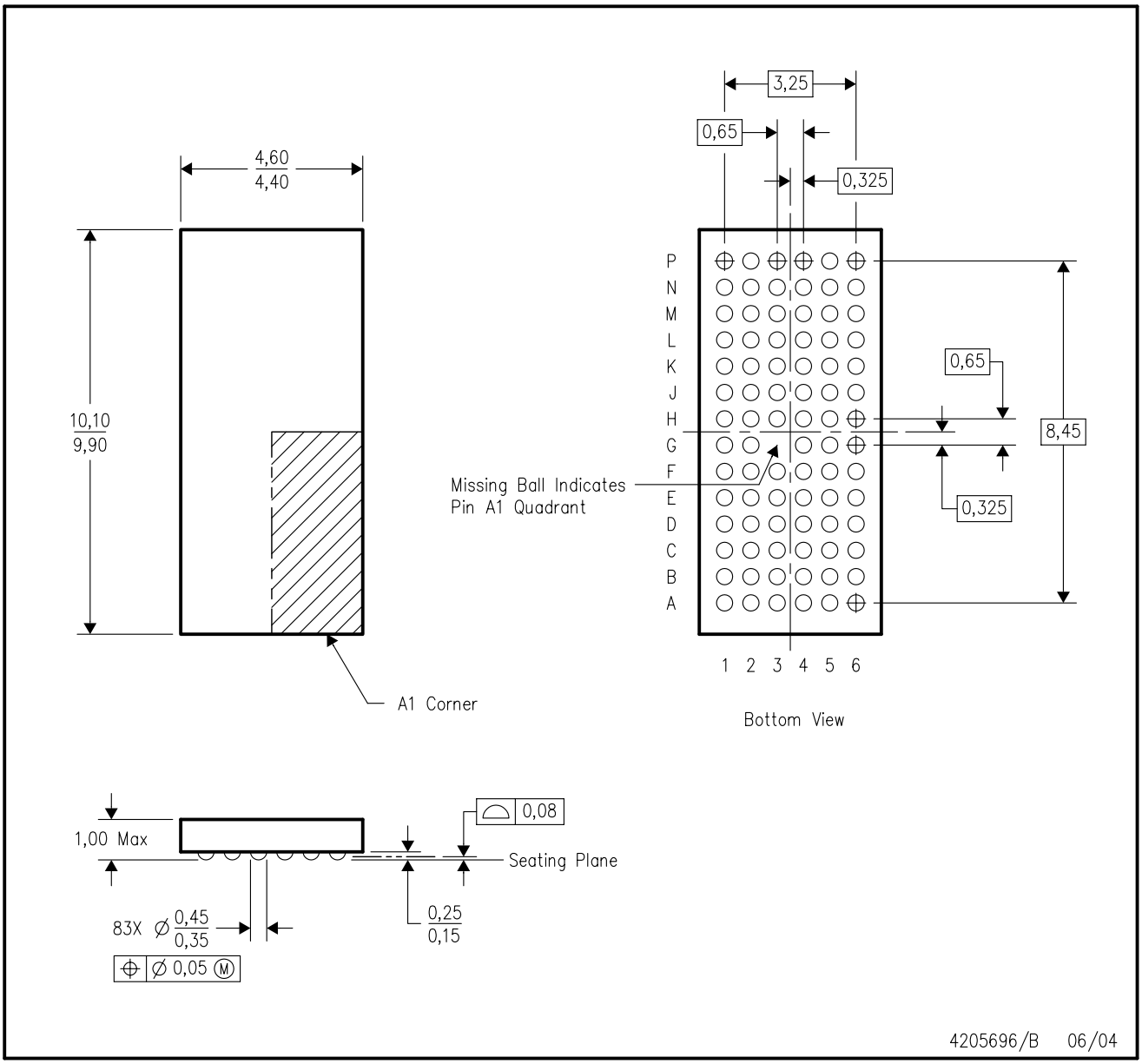
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

GRG (R–PBGA–N83) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. JEDEC MO–225 registration is pending.
D. This package is tin–lead (SnPb). Refer to the 83 ZRG package (drawing 4205696) for lead–free.

ZRG (R–PBGA–N83) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. JEDEC MO–225 registration is pending.
D. This package is lead–free. Refer to the 83 GRG package (drawing 4205581) for tin–lead (SnPb).

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