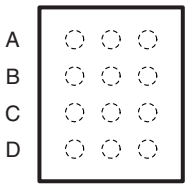
VOLTAGE-LEVEL SHIFTER FOR IC-USB INTERFACE

FEATURES

- **V_{CCA}, V_{CCB} Supply Voltage: 1.1 V to 3.6 V**
- **When V_{CCB} = 0 V, A-Port is Disabled and B-Port is Held at GND Through 120-kΩ Pulldown**
- **Crossover Skew of <1 ns**
- **Meets All Requirements of the IC-USB Standard**
- **Small Package: 0.4 mm pitch WCSP (1.2 mm × 1.6 mm)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II ESD Performance**
  - **A-Port (Host Side)**
    - **2000-V Human-Body Model**
    - **1000-V Charged-Device Model**
  - **B-Port (Peripheral Side)**
    - **8000-V Contact Discharge**
    - **15000-V Air-Gap Discharge**

YFP PACKAGE
(TOP VIEW)



	1	2	3
A	PD_EN	V_{CCA}	V_{CCB}
B	D+(A)	V_{CCA}	D+(B)
C	D–(A)	GND	D–(B)
D	DIR	GND	DIR_POL

DESCRIPTION/ORDERING INFORMATION

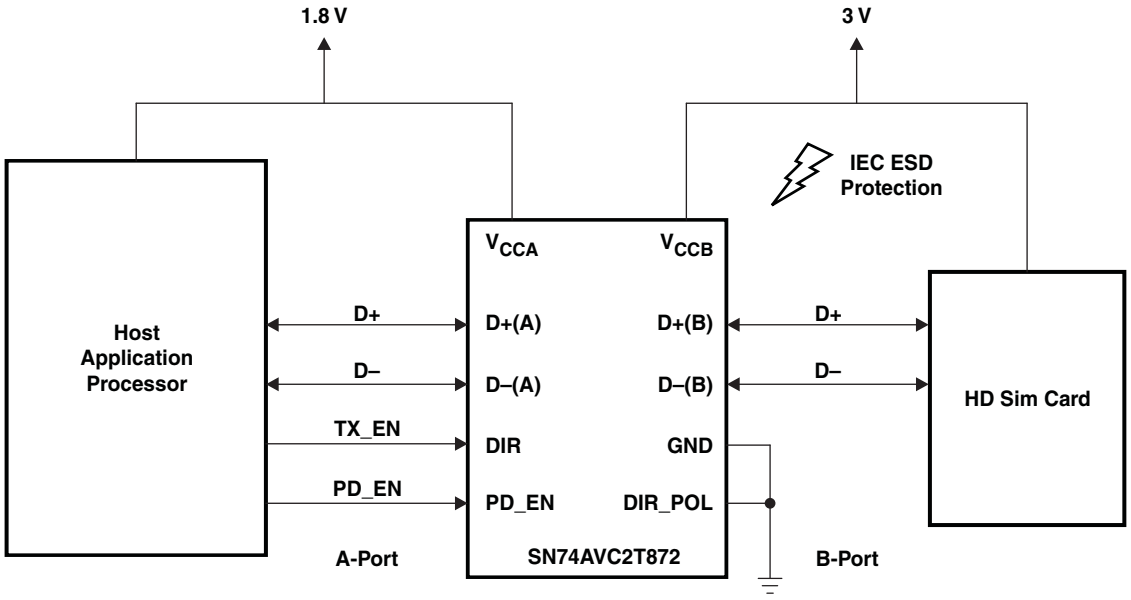
The SN74AVC2T872 is a 2-bit voltage level translator optimized for use in interchip USB (IC-USB) applications. V_{CCA} and V_{CCB} can each operate over the full range of 1.1 V to 3.6 V. The device has been designed to maintain crossover skew to be less than 1 ns. Each B-port has an integrated 120-kΩ pulldown resistor that can be enabled and disabled using the PD_EN control signal. If V_{CCB} = 0 V, the A-port I/Os are disabled (Hi-Z) and the B-port I/Os are held to GND through the 120-kΩ resistors. If V_{CCA} = 0 V, the A-port and B-port I/Os are disabled (Hi-Z).

ORDERING INFORMATION

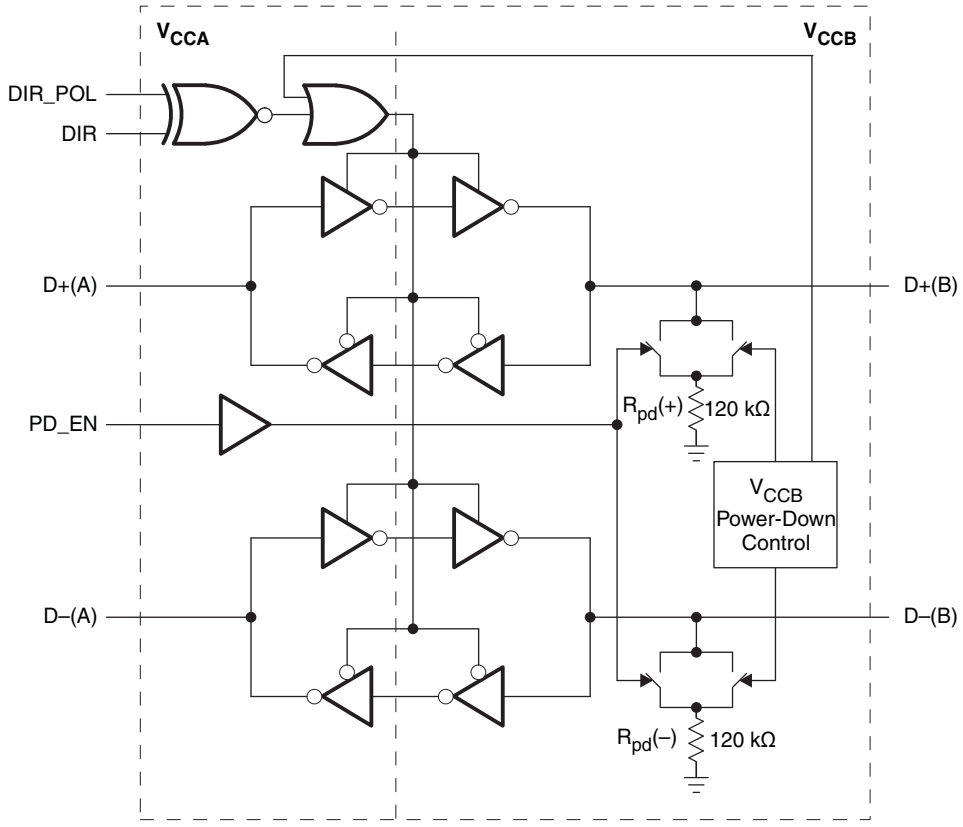
T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
–40°C to 85°C	WCSP – YFP	Reel of 3000	SN74AVC2T872YFPR	_ _ _ TU _

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) YFP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

TYPICAL APPLICATION BLOCK DIAGRAM



LOGIC DIAGRAM



TERMINAL FUNCTIONS

BALL NO.	NAME	FUNCTION
A1	PD_EN	Input to enable pulldown resistors on B-side. PD_EN = Low will disconnect the pulldown resistors. PD_EN = High will connect the pulldown resistors.
A2, B2	V_{CCA}	A-side supply voltage (1.1 V to 3.6 V)
A3	V_{CCB}	B-side supply voltage (1.1 V to 3.6 V)
B1	D+(A)	USB data signal connected to host.
B3	D+(B)	USB data signal connected to peripheral with internal 120 kΩ resistor to GND that can be disconnected by PD_EN.
C1	D–(A)	USB data signal connected to host.
C2, D2	GND	Ground
C3	D–(B)	USB data signal connected to peripheral with internal 120 kΩ resistor to GND that can be disconnected by PD_EN.
D1	DIR	Direction control input. If DIR_POL = Low, then DIR = Low allows A to B data flow. If DIR_POL = High, then DIR = High allows A to B data flow.
D3	DIR_POL	Direction polarity chooser. If DIR_POL = Low, then DIR = Low allows A to B data flow. If DIR_POL = High, then DIR = High allows A to B data flow.

FUNCTION TABLE

INPUTS		A-SIDE	B-SIDE	FUNCTION
DIR_POL	DIR			
L	L	Input	Output	A-to-B Data Flow
L	H	Output	Input	B-to-A Data Flow
H	L	Output	Input	B-to-A Data Flow
H	H	Input	Output	A-to-B Data Flow

B-SIDE PULLDOWN RESISTOR BEHAVIOR

V_{CCA}	V_{CCB}	PD_EN	PULLDOWN RESISTOR
			B-SIDE
0 V	X	X	None
1.1 to 3.6 V	0 V	X	120 kΩ to GND
1.1 to 3.6 V	1.1 to 3.6 V	L	None
1.1 to 3.6 V	1.1 to 3.6 V	H	120 kΩ to GND

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range(2)	I/O ports (A-Port)	–0.5	4.6	V
		I/O ports (B-Port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	A-Port	–0.5	4.6	V
		B-Port	–0.5	4.6	
V_O	Voltage range applied to any output in the high or low state(2)	A-Port	–0.5	V_{CCA} + 0.5	V
		B-Port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
θ_{JA}	Package thermal impedance(3)	YFP package		137.5	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)(2)(3)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.1	3.6	V
V_{CCB}	Supply voltage				1.1	3.6	V
V_{IH}	High-level input voltage	Data inputs(4)	1.1 V to 1.95 V		V_{CCI} × 0.65		V
			1.95 V to 2.7 V		1.65		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Data inputs(4)	1.1 V to 1.95 V			V_{CCI} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_{IH}	High-level input voltage	DIR, DIR_POL, PD_EN (referenced to V_{CCA})(5)	1.1 V to 1.95 V		V_{CCA} × 0.65		V
			1.95 V to 2.7 V		V_{CCA} × 0.65		
			2.7 V to 3.6 V		V_{CCA} × 0.65		
V_{IL}	Low-level input voltage	DIR, DIR_POL, PD_EN (referenced to V_{CCA})(5)	1.1 V to 1.95 V			V_{CCA} × 0.35	V
			1.95 V to 2.7 V			V_{CCA} × 0.35	
			2.7 V to 3.6 V			V_{CCA} × 0.35	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.1 to 1.3 V		–2	mA
				1.4 V to 1.6 V		–6	
				1.65 V to 1.95 V		–8	
				2.3 V to 2.7 V		–9	
				3 V to 3.6 V		–12	
I_{OL}	Low-level output current			1.1 V to 1.3 V		2	mA
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
Δt/Δv	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				–40	85	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. All unused control inputs of the device must be held at V_{CCA} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(4) For data input values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V.
(5) For control input values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V.

ELECTRICAL CHARACTERISTICS(1)(2)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to 85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
V_{OH}		I_{OH} = –100 µA	$V_I = V_{IH}$	1.1 V to 3.6 V	1.1 V to 3.6 V				V_{CCO} – 0.2		V
		I_{OH} = –2 mA		1.1 V	1.1 V				0.9		
		I_{OH} = –6 mA		1.4 V	1.4 V				1		
		I_{OH} = –8 mA		1.65 V	1.65 V				1.2		
		I_{OH} = –9 mA		2.3 V	2.3 V				1.75		
		I_{OH} = –12 mA		3 V	3 V				2.3		
V_{OL}		I_{OL} = 100 µA	$V_I = V_{IL}$	1.1 V to 3.6 V	1.1 V to 3.6 V					0.2	V
		I_{OL} = 3 mA		1.1 V	1.1 V					0.3	
		I_{OL} = 6 mA		1.4 V	1.4 V					0.35	
		I_{OL} = 8 mA		1.65 V	1.65 V					0.45	
		I_{OL} = 9 mA		2.3 V	2.3 V					0.55	
		I_{OL} = 12 mA		3 V	3 V					0.7	
I_I	Control inputs	$V_I = V_{CCA}$ or GND		1.1 V to 3.6 V	1.1 V to 3.6 V		±0.025	±0.25		±1	µA
I_{off}	A port	V_I or V_O = 0 to 3.6 V		0 V	0 V to 3.6 V		±0.02	±2.5		±5	µA
I_{OZ}	A port	DIR_POL = Low, PD_EN = Low, $V_I = V_{CCI}$ to GND,	DIR = Low	3.6 V	3.6 V		±0.01	±2.5		±5	µA
	B port		DIR = High	3.6 V	3.6 V		±0.14	±5		±15	
I_{CCA}		$V_I = V_{CCI}$ or GND, I_O = 0		1.1 V to 3.6 V	1.1 V to 3.6 V		0.02			10	µA
				0 V	0 V to 3.6 V					–2	
				0 V to 3.6 V	0 V		0.01			10	
I_{CCB}		$V_I = V_{CCI}$ or GND, I_O = 0		1.1 V to 3.6 V	1.1 V to 3.6 V		0.13			30	µA
				0 V	0 V to 3.6 V		0.07			15	
				0 V to 3.6 V	0 V					–2	
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, I_O = 0		1.1 V to 3.6 V	1.1 V to 3.6 V		0.15			40	µA
C_i	Control inputs	V_I = 3.3 V or GND		3.6 V	3.6 V		1.5			2	pF
C_{io}	A port	V_O = 3.3 V or GND		3.6 V	3.6 V		5.5			7	pF
	B port						27			32.5	
$R_{pd(+)}$, $R_{pd(–)}$		DIR_POL = Low, DIR = High, PD_EN = High		3.6 V	3.6 V		118		80	150	kΩ

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 1.2 V ± 0.1 V, PD_EN = 0 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V ± 0.1 V		V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay	D+(A) to D+(B) or D–(A) to D–(B)			22		16		14		12		11	ns
t_{PHL}					22		16		14		12		11	
t_{PLH}		D+(B) to D+(A) or D–(B) to D–(A)			19		17		17		16		15	ns
t_{PHL}					19		17		17		16		15	
t_r	Output rise time				14		14		14		14		14	ns
t_f	Output fall time				14		14		14		14		14	ns
t_{PHZ}	Disable time	DIR or DIR_POL	D+(A) or D–(A)		24		24		24		24		24	ns
t_{PLZ}					24		24		24		24		24	
t_{PHZ}		DIR or DIR_POL	D+(B) or D–(B)		28		22		19		15		14	ns
t_{PLZ}					28		22		19		15		14	
t_{PZH}	Enable time(1)	DIR or DIR_POL	D+(A) or D–(A)		47		39		36		31		29	ns
t_{PZL}					47		39		36		31		29	
t_{PZH}		DIR or DIR_POL	D+(B) or D–(B)		46		40		38		36		35	ns
t_{PZL}					46		40		38		36		35	
F_{max}	Max data rate			12		12		12		12		12		Mbps

(1) The enable time is a calculated value derived using the formula shown in the enable times section.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V, PD_EN = 0 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V ± 0.1 V		V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay	D+(A) to D+(B) or D–(A) to D–(B)			18	0.7	13.3	0.5	11.3	0.4	8.9	0.3	7.7	ns
t_{PH}					18	0.7	11.8	0.5	10.2	0.4	8.2	0.3	7.5	
t_{PLH}		D+(B) to D+(A) or D–(B) to D–(A)			13	0.8	11.2	0.7	10.5	0.6	9.7	0.5	9.3	ns
t_{PHL}					13	0.8	10.9	0.7	10.2	0.6	9.4	0.5	9.1	
t_r	Output rise time				14		10		10		10		10	ns
t_f	Output fall time				14		10		10		10		10	ns
t_{PHZ}	Disable time	DIR or DIR_POL	D+(A) or D–(A)		17	1.3	14.2	1.3	13.4	1	11.8	1	11.1	ns
t_{PLZ}					17	1.3	14.2	1.3	14.3	1	14.4	1	14.4	
t_{PHZ}		DIR or DIR_POL	D+(B) or D–(B)		22	1.1	14.5	1.4	13.3	1.2	10.6	1.7	10.1	ns
t_{PLZ}					22	1.1	16.8	1.4	13.5	1.2	9.8	1.7	9.3	
t_{PZH}	Enable time(1)	DIR or DIR_POL	D+(A) or D–(A)		35		28		24		19.5		18.5	ns
t_{PZL}					35		25.3		23.5		20		19.2	
t_{PZH}		DIR or DIR_POL	D+(B) or D–(B)		35		27.5		25.5		23.2		22.1	ns
t_{PZL}					35		26.1		23.6		20		18.6	
F_{max}	Max data rate			12		12		12		12		12		Mbps

(1) The enable time is a calculated value derived using the formula shown in the enable times section.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V, PD_EN = 0 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V ± 0.1 V		V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay	D+(A) to D+(B) or D–(A) to D–(B)			17	0.7	12.6	0.4	10.5	0.2	8.1	0.2	6.9	ns
t_{PHL}					17	0.7	11.2	0.4	9.5	0.2	7.4	0.2	6.7	
t_{PLH}		D+(B) to D+(A) or D–(B) to D–(A)			11	0.5	9.5	0.4	8.8	0.5	7.9	0.4	7.5	ns
t_{PHL}					11	0.5	9.3	0.4	8.7	0.5	7.9	0.4	7.6	
t_r	Output rise time				14		10		10		10		10	ns
t_f	Output fall time				14		10		10		10		10	ns
t_{PHZ}	Disable time	DIR or DIR_POL	D+(A) or D–(A)		13	1.1	11.4	1	10.8	0.5	9.8	0.5	9	ns
t_{PLZ}					13	1.1	10.7	1	10.8	0.5	10.8	0.5	10.9	
t_{PHZ}		DIR or DIR_POL	D+(B) or D–(B)		21	1.1	10.7	1.3	10.6	0.8	9	0.5	9	ns
t_{PLZ}					21	1.1	15.7	1.3	12.5	0.8	8.8	0.5	8.3	
t_{PZH}	Enable Time(1)	DIR or DIR_POL	D+(A) or D–(A)		32		25.2		21.3		16.7		15.8	ns
t_{PZL}					32		20.1		19.2		16.9		16.6	
t_{PZH}		DIR or DIR_POL	D+(B) or D–(B)		30		23.3		21.3		18.9		17.7	ns
t_{PZL}					30		22.7		20.3		17.2		15.8	
F_{max}	Max data rate			12		12		12		12		12		Mbps

(1) The enable time is a calculated value derived using the formula shown in the enable times section.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V, PD_EN = 0 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V ± 0.1 V		V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay	D+(A) to D+(B) or D–(A) to D–(B)			16	0.5	11.7	0.2	9.7	0.2	7.2	0.2	6	ns
t_{PHL}					16	0.5	10.5	0.2	8.7	0.2	7.2	0.2	5.8	
t_{PLH}		D+(B) to D+(A) or D–(B) to D–(A)			9	0.4	7.5	0.5	6.8	0.4	5.9	0.3	5.6	ns
t_{PHL}					9	0.4	7.5	0.5	6.8	0.4	6	0.3	5.6	
t_r	Output rise time				14		10		10		10		10	ns
t_f	Output fall time				14		10		10		10		10	ns
t_{PHZ}	Disable time	DIR or DIR_POL	D+(A) or D–(A)		11	0.7	7.8	0.7	7.5	0.7	6.9	0.5	6.4	ns
t_{PLZ}					11	0.7	6.8	0.7	6.8	0.7	6.8	0.5	6.8	
t_{PHZ}		DIR or DIR_POL	D+(B) or D–(B)		19	0.6	8.4	0.5	7.4	0.5	6.3	1	7.2	ns
t_{PLZ}					19	0.6	14.4	0.5	11	0.5	7.4	1	6.9	
t_{PZH}	Enable time[1]	DIR or DIR_POL	D+(A) or D–(A)		29		21.9		17.8		13.3		12.5	ns
t_{PZL}					29		15.9		14.2		12.2		12.8	
t_{PZH}		DIR or DIR_POL	D+(B) or D–(B)		27		18.5		16.4		14		12.8	ns
t_{PZL}					27		18.2		16.2		14.1		12.2	
F_{max}	Max data rate			12		12		12		12		12		Mbps

(1) The enable time is a calculated value derived using the formula shown in the enable times section.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V, PD_EN = 0 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V ± 0.1 V		V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay	D+(A) to D+(B) or D–(A) to D–(B)			15	0.6	11.3	0.4	9.2	0.3	6.8	0.3	5.6	ns
t_{PHL}					15	0.6	10.2	0.4	8.4	0.3	6.2	0.3	5.5	
t_{PLH}		D+(B) to D+(A) or D–(B) to D–(A)			9	0.3	6.6	0.2	5.8	0.2	4.9	0.2	4.5	ns
t_{PHL}					9	0.3	7	0.2	6.2	0.2	5.3	0.2	4.9	
t_r	Output rise time				14		10		10		10		10	ns
t_f	Output fall time				14		10		10		10		10	ns
t_{PHZ}	Disable time	DIR or DIR_POL	D+(A) or D–(A)		9	1	6.6	1	6.5	1	6.1	1	5.8	ns
t_{PLZ}					9	1	5.7	1	5.7	1	5.7	1	5.7	
t_{PHZ}		DIR or DIR_POL	D+(B) or D–(B)		19	0.5	7.4	0.3	6.5	0.3	5.2	0.3	5.3	ns
t_{PLZ}					19	0.5	13.8	0.3	10.6	0.3	7	0.3	6.4	
t_{PZH}	Enable time(1)	DIR or DIR_POL	D+(A) or D–(A)		28		20.4		16.4		11.9		10.9	ns
t_{PZL}					28		14.4		12.7		10.4		10.2	
t_{PZH}		DIR or DIR_POL	D+(B) or D–(B)		24		17		14.9		12.5		11.3	ns
t_{PZL}					24		16.7		14.9		12.3		11.3	
F_{max}	Max data rate			12		12		12		12		12		Mbps

(1) The enable time is a calculated value derived using the formula shown in the enable times section.

IC-USB INTERFACE CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V, PD_EN = 0 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	
t_{sko}	Output crossover skew	D+(A) to D–(A)	Opposite Transitions		1		1	ns
		D+(B) to D–(B)			1		1	
t_{jitter_c}	Consecutive transitions jitter				2		2	ns
t_{jitter_p}	Paired transitions jitter				1		1	
F_{max}	Max data rate			12		12		Mbps

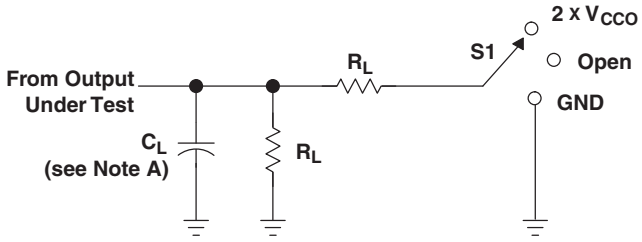
OPERATING CHARACTERISTICS

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.2 V	V_{CCA} = V_{CCB} = 1.5 V	V_{CCA} = V_{CCB} = 1.8 V	V_{CCA} = V_{CCB} = 2.5 V	V_{CCA} = V_{CCB} = 3.3 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
C_{pdA} (1)	A-port input, B-port output	C_L = 0, f = 10 MHz, $t_r = t_f$ = 1 ns	1	1	1	1	2	pF
	B-port input, A-port output		14	14	14	16	20	
C_{pdB} (1)	A-port input, B-port output	C_L = 0, f = 10 MHz, $t_r = t_f$ = 1 ns	28	27	27	27	27	pF
	B-port input, A-port output		1	1	1	1	2	

(1) Power dissipation capacitance per transceiver

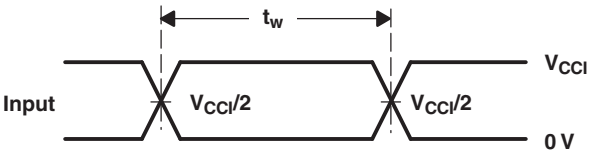
PARAMETER MEASURMENT INFORMATION



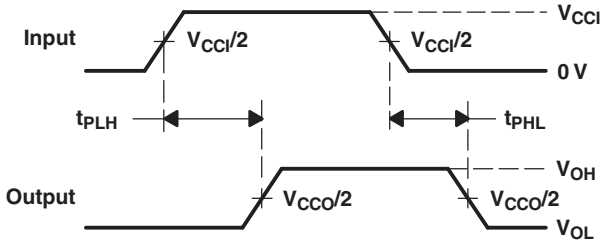
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CCO}
t_{PHZ}/t_{PZH}	GND

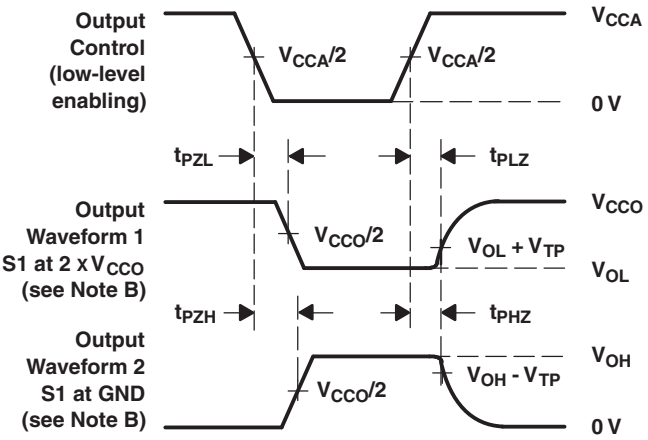
V_{CCO}	C_L	R_L	V_{TP}
1.2 V	18 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	18 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	18 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	18 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	18 pF	2 kΩ	0.3 V



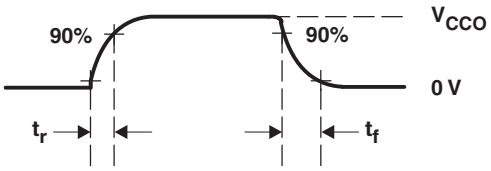
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



OUTPUT RISE AND FALL TIMES

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 W, dv/dt ≥ 1 V/ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}. For the SN74AVC2T872, these delays are calculated per the Enable Times forumulas shown in Table 1.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

H. V_{CCI} is the V_{CC} associated with the input port.

I. V_{CCO} is the V_{CC} associated with the output port.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASURMENT INFORMATION (continued)

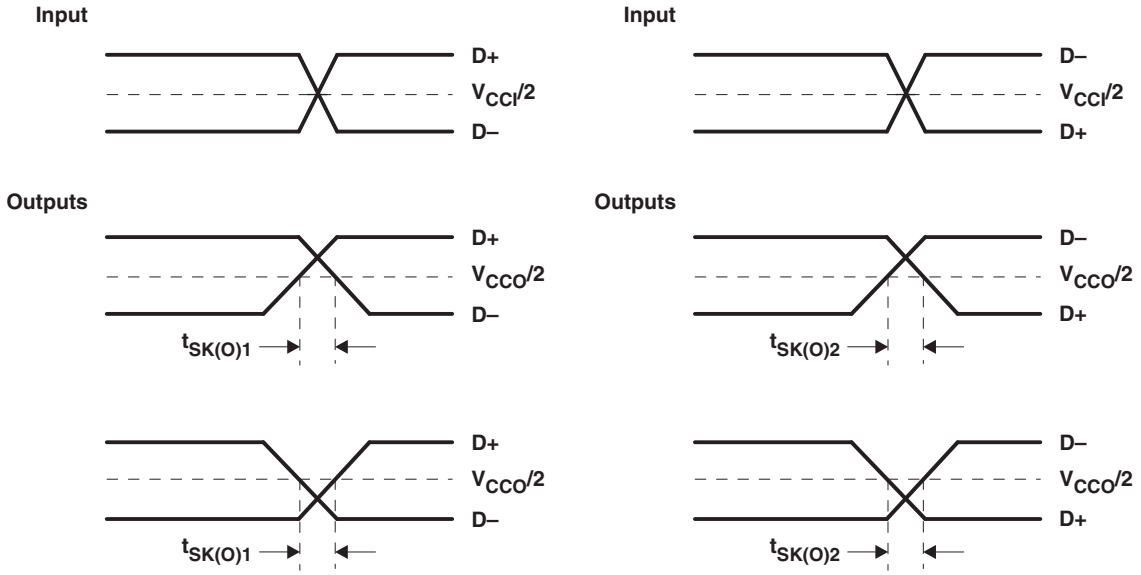


Figure 2. Output Crossover Skew

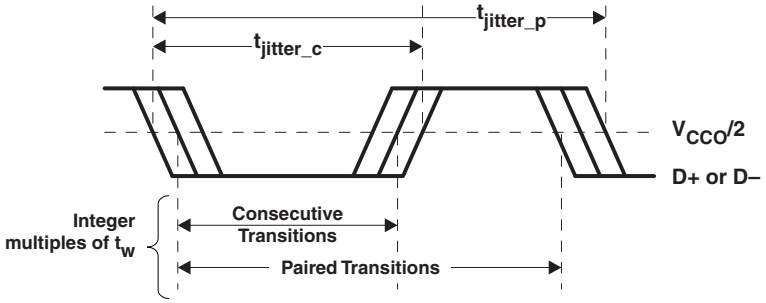


Figure 3. Output Jitter

APPLICATION INFORMATION

Enable Times

Calculate the enable times for the SN74AVC2T872 using the following formulas shown in Table 1.

Table 1. Enable Times

t_{PZH} (DIR to A) = t_{PLZ} (DIR to B) + t_{PLH} (B to A)
t_{PZL} (DIR to A) = t_{PHZ} (DIR to B) + t_{PHL} (B to A)
t_{PZH} (DIR to B) = t_{PLZ} (DIR to A) + t_{PLH} (A to B)
t_{PZL} (DIR to B) = t_{PHZ} (DIR to A) + t_{PHL} (A to B)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74AVC2T872 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AVC2T872YFPR	ACTIVE	DSBGA	YFP	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(TU2 ~ TUN)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

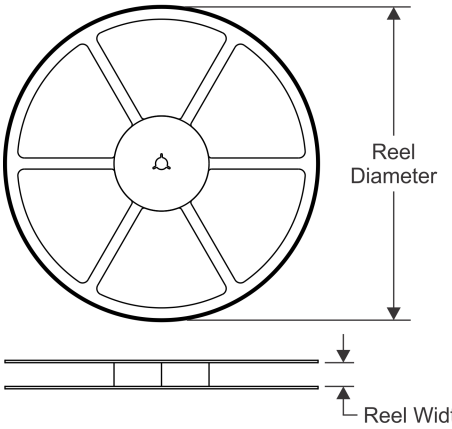
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

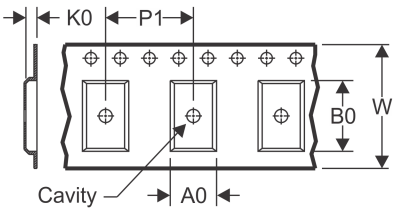
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

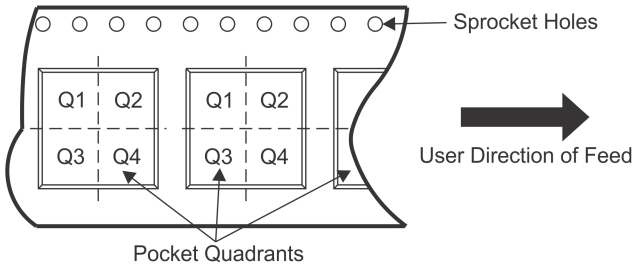


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

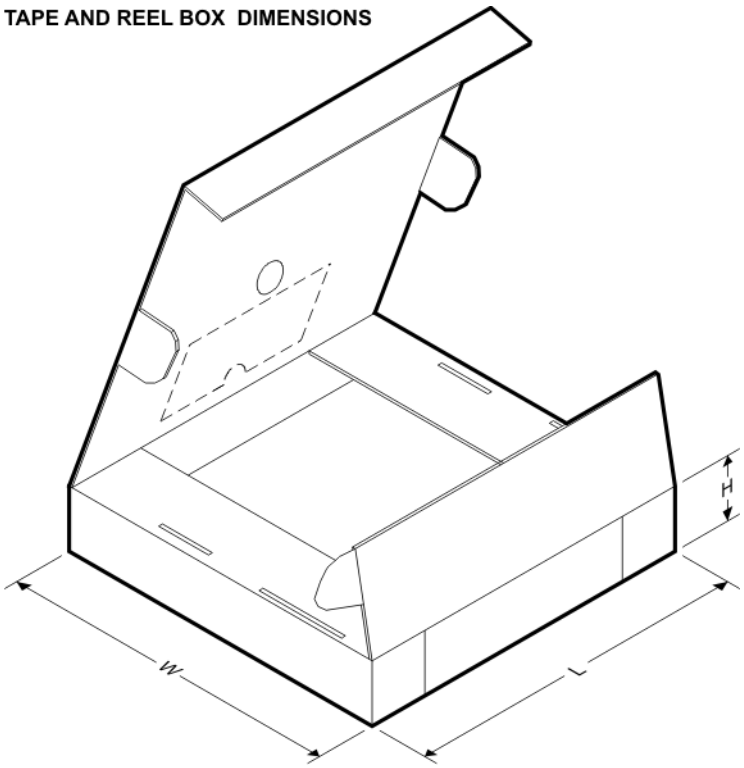
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC2T872YFPR	DSBGA	YFP	12	3000	178.0	9.2	1.28	1.68	0.62	4.0	8.0	Q1

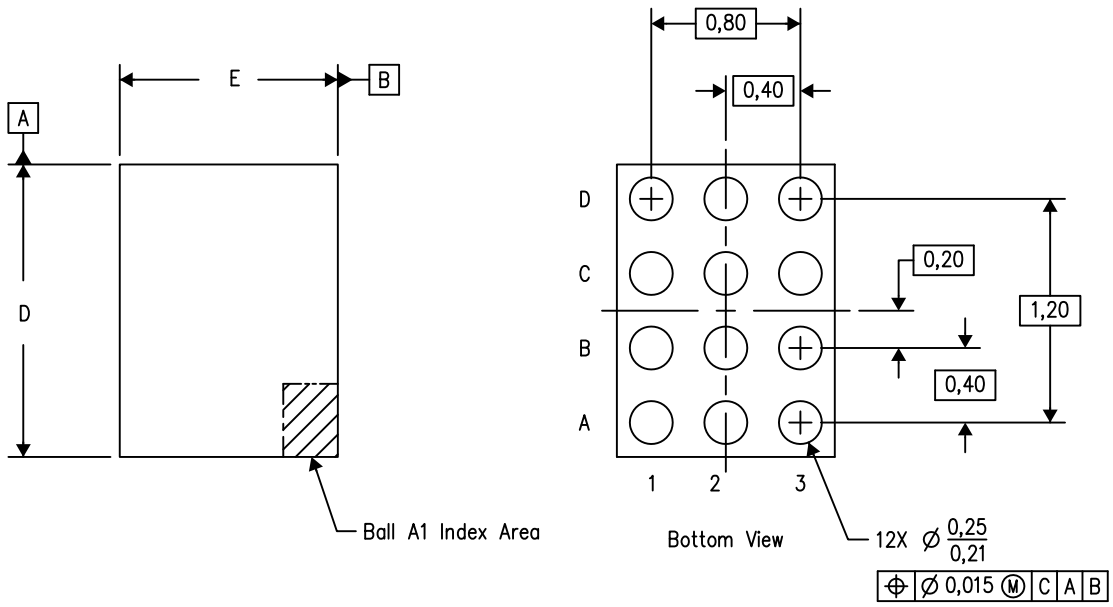
TAPE AND REEL BOX DIMENSIONS

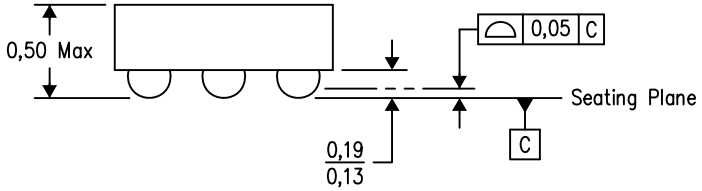


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC2T872YFPR	DSBGA	YFP	12	3000	220.0	220.0	35.0

YFP (R–XBGA–N12) DIE–SIZE BALL GRID ARRAY





D: Max = 1.59 mm, Min = 1.53 mm

E: Max = 1.19 mm, Min = 1.13 mm

4206986–7/T 05/13

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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