- Member of the Texas Instruments Widebus+™ Family
- High-Bandwidth Data Path (Up to 500 MHz†)
- 5-V-Tolerant I/Os with Device Powered Up or Powered Down
- Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range (r_{on} = 5 Ω Typical)
- Rail-to-Rail Switching on Data I/O Ports
  – 0- to 5-V Switching With 3.3-V V_{CC}
  – 0- to 3.3-V Switching With 2.5-V V_{CC}
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 4 pF Typical)
- Fast Switching Frequency ($f_{\overline{OE}}$ = 20 MHz Max)

  † For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number SCDA008.

- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption (I_{CC} = 2 mA Typical)
- V_{CC} Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  – 2000-V Human-Body Model (A114-B, Class II)
  – 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: PCI Interface, Differential Signal Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating

description/ordering information

The SN74CB3Q32245 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q32245 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q32245 is organized as four 8-bit bus switches with separate output-enable ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$) inputs. It can be used as four 8-bit bus switches, two 16-bit bus switches, or as one 32-bit bus switch. When $\overline{OE}$ is low, the associated 8-bit bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 8-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

ORDERING INFORMATION

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	LFBGA – GKE	Tape and reel	SN74CB3Q32245GKER	BZ245
	LFBGA – ZKE (Pb-free)	Tape and reel	SN74CB3Q32245ZKER	

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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TEXAS INSTRUMENTS

description/ordering information (continued)

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each 8-bit bus switch)

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

GKE PACKAGE
(TOP VIEW)
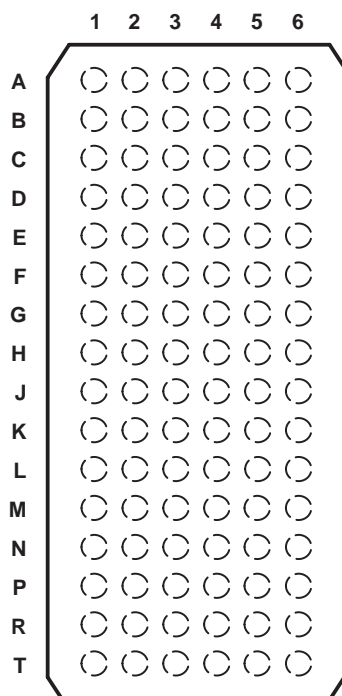
terminal assignments

	1	2	3	4	5	6
A	1B2	1B1	NC	1$\overline{OE}$	1A1	1A2
B	1B4	1B3	GND	GND	1A3	1A4
C	1B6	1B5	V_{CC}	V_{CC}	1A5	1A6
D	1B8	1B7	GND	GND	1A7	1A8
E	2B2	2B1	GND	GND	2A1	2A2
F	2B4	2B3	V_{CC}	V_{CC}	2A3	2A4
G	2B6	2B5	GND	GND	2A5	2A6
H	2B7	2B8	NC	2$\overline{OE}$	2A8	2A7
J	3B2	3B1	NC	3$\overline{OE}$	3A1	3A2
K	3B4	3B3	GND	GND	3A3	3A4
L	3B6	3B5	V_{CC}	V_{CC}	3A5	3A6
M	3B8	3B7	GND	GND	3A7	3A8
N	4B2	4B1	GND	GND	4A1	4A2
P	4B4	4B3	V_{CC}	V_{CC}	4A3	4A4
R	4B6	4B5	GND	GND	4A5	4A6
T	4B7	4B8	NC	4$\overline{OE}$	4A8	4A7

NC – No internal connection

logic diagram (positive logic)
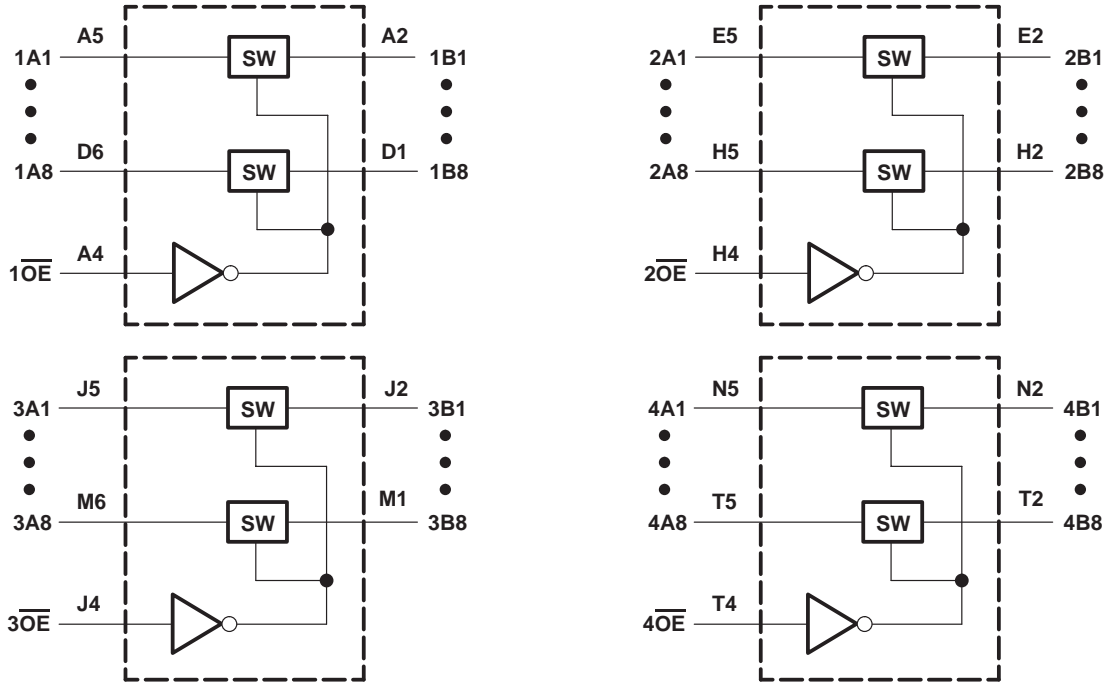
simplified schematic, each FET switch (SW)
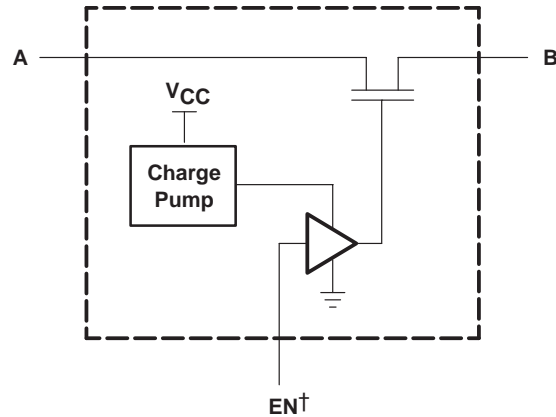
† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . –0.5 V to 4.6 V

Control input voltage range, V_{IN} (see Notes 1 and 2) . . . . –0.5 V to 7 V

Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) . . . . –0.5 V to 7 V

Control input clamp current, I_{IK} ($V_{IN} < 0$) . . . . –50 mA

I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$) . . . . –50 mA

ON-state switch current, $I_{I/O}$ (see Note 4) . . . . ±64 mA

Continuous current through V_{CC} or GND terminals . . . . ±100 mA

Package thermal impedance, θ_{JA} (see Note 5) . . . . 40°C/W

Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground, unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		–40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report,
Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V,	I_I = −18 mA				−1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6 V,	V_{IN} = 0 to 5.5 V				±1	µA
I_{OZ}‡		V_{CC} = 3.6 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±1	µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			1	µA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND		2	4	mA
ΔI_{CC}§	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			30	µA
I_{CCD}¶	Per control input	V_{CC} = 3.6 V, A and B ports open, Control input switching at 50% duty cycle				0.15	0.25	mA/ MHz
C_{in}	Control inputs	V_{CC} = 3.3 V,	V_{IN} = 5.5 V, 3.3 V, or 0			3.5	5	pF
$C_{io(OFF)}$		V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		4	6	pF
$C_{io(ON)}$		V_{CC} = 3.3 V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		10	13	pF
r_{on}#		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0,	I_O = 30 mA		6	8	Ω
			V_I = 1.7 V,	I_O = −15 mA		5	10	
		V_{CC} = 3 V	V_I = 0,	I_O = 30 mA		6	8	
			V_I = 2.4 V,	I_O = −15 mA		5	9	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

¶ This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
$f_{\overline{OE}}$‖	$\overline{OE}$	A or B		10		20	MHz
t_{pd}☆	A or B	B or A		0.18		0.3	ns
t_{en}	$\overline{OE}$	A or B	1.5	8	1.5	7	ns
t_{dis}	$\overline{OE}$	A or B	1	8	1	7	ns

‖ Maximum switching frequency for control input (V_O > V_{CC}, V_I = 5 V, R_L ≥ 1 MΩ, C_L = 0)

☆ The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
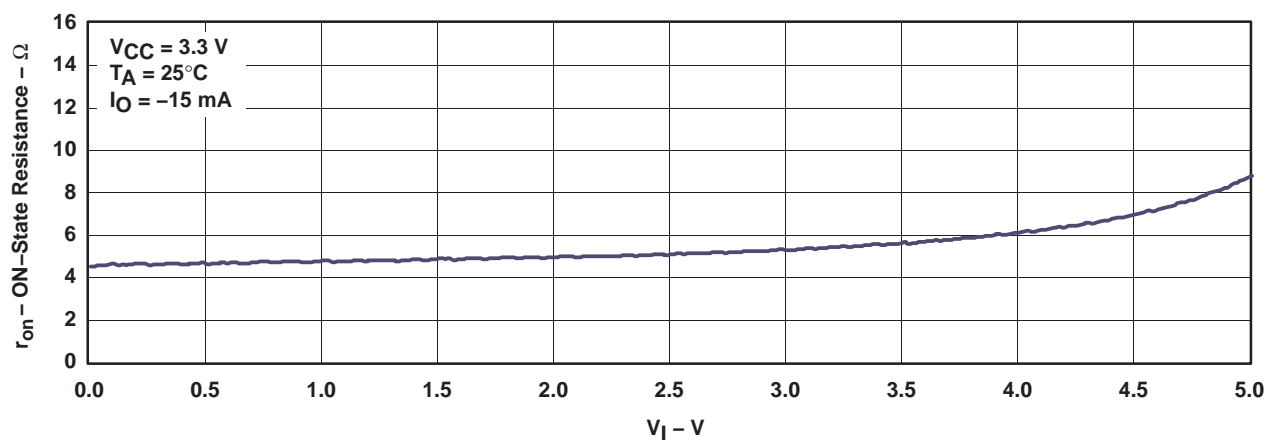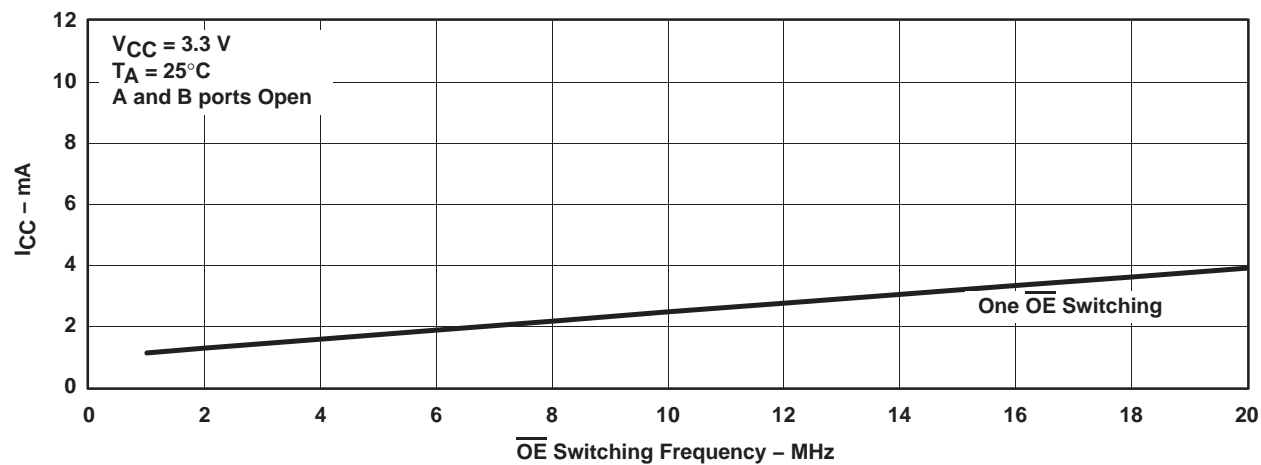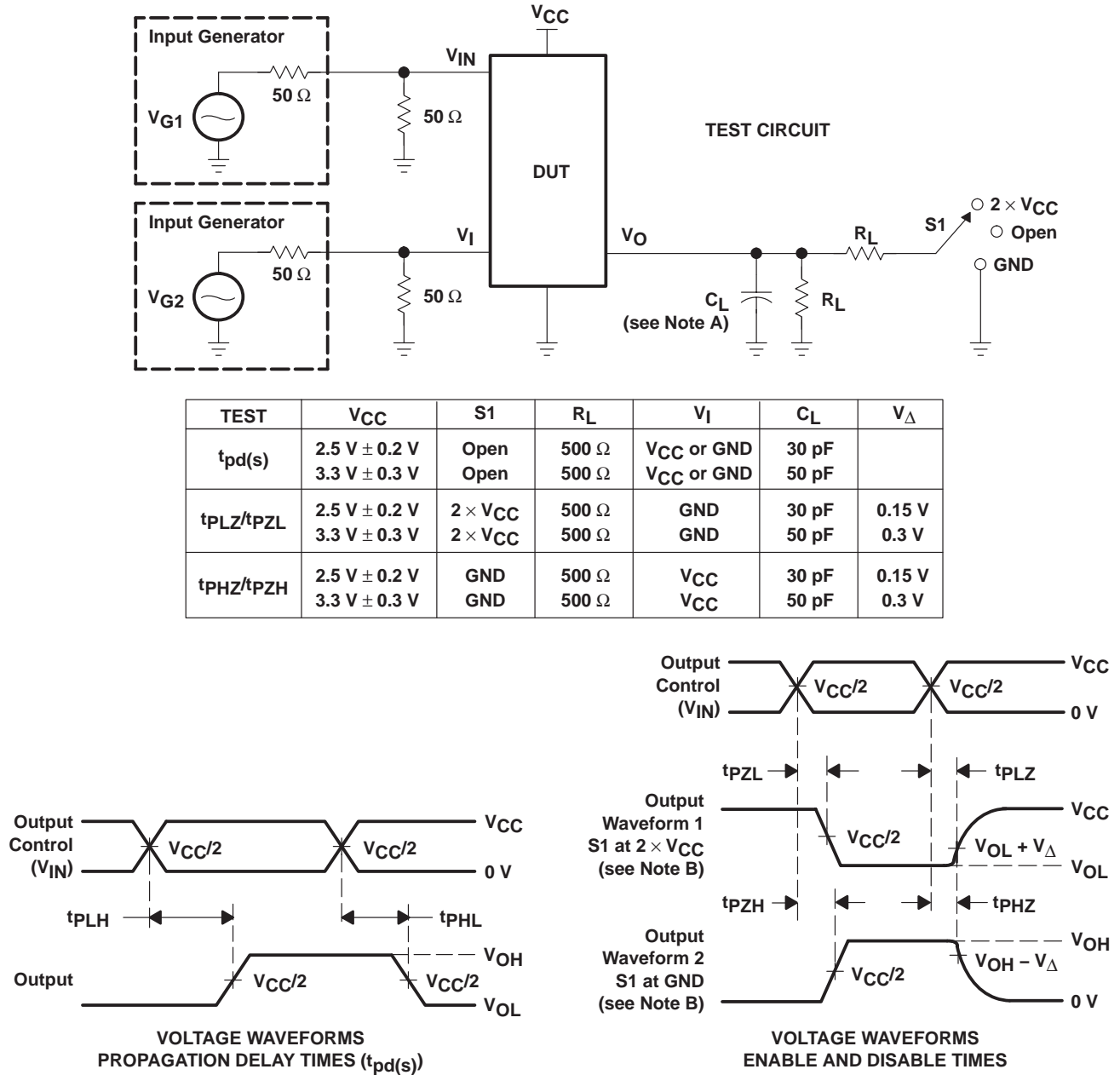
Figure 1. Typical r$_{on}$ vs V$_I$

Figure 2. Typical I$_{CC}$ vs $\overline{\text{OE}}$ Switching Frequency

TEXAS INSTRUMENTS

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PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V	Open	500 Ω	V_{CC} or GND	30 pF	
	3.3 V ± 0.3 V	Open	500 Ω	V_{CC} or GND	50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V	2 × V_{CC}	500 Ω	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 × V_{CC}	500 Ω	GND	50 pF	0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V	GND	500 Ω	V_{CC}	30 pF	0.15 V
	3.3 V ± 0.3 V	GND	500 Ω	V_{CC}	50 pF	0.3 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50$ Ω, $t_r ≤ 2.5$ ns, $t_f ≤ 2.5$ ns.
   D. The outputs are measured one at a time, with one transition per measurement.
   E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
   F. t_{PZL} and t_{PZH} are the same as t_{en}.
   G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state
      resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
   H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CB3Q32245ZKER	OBSOLETE	LFBGA	ZKE	96		TBD	Call TI	Call TI		BZ245	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
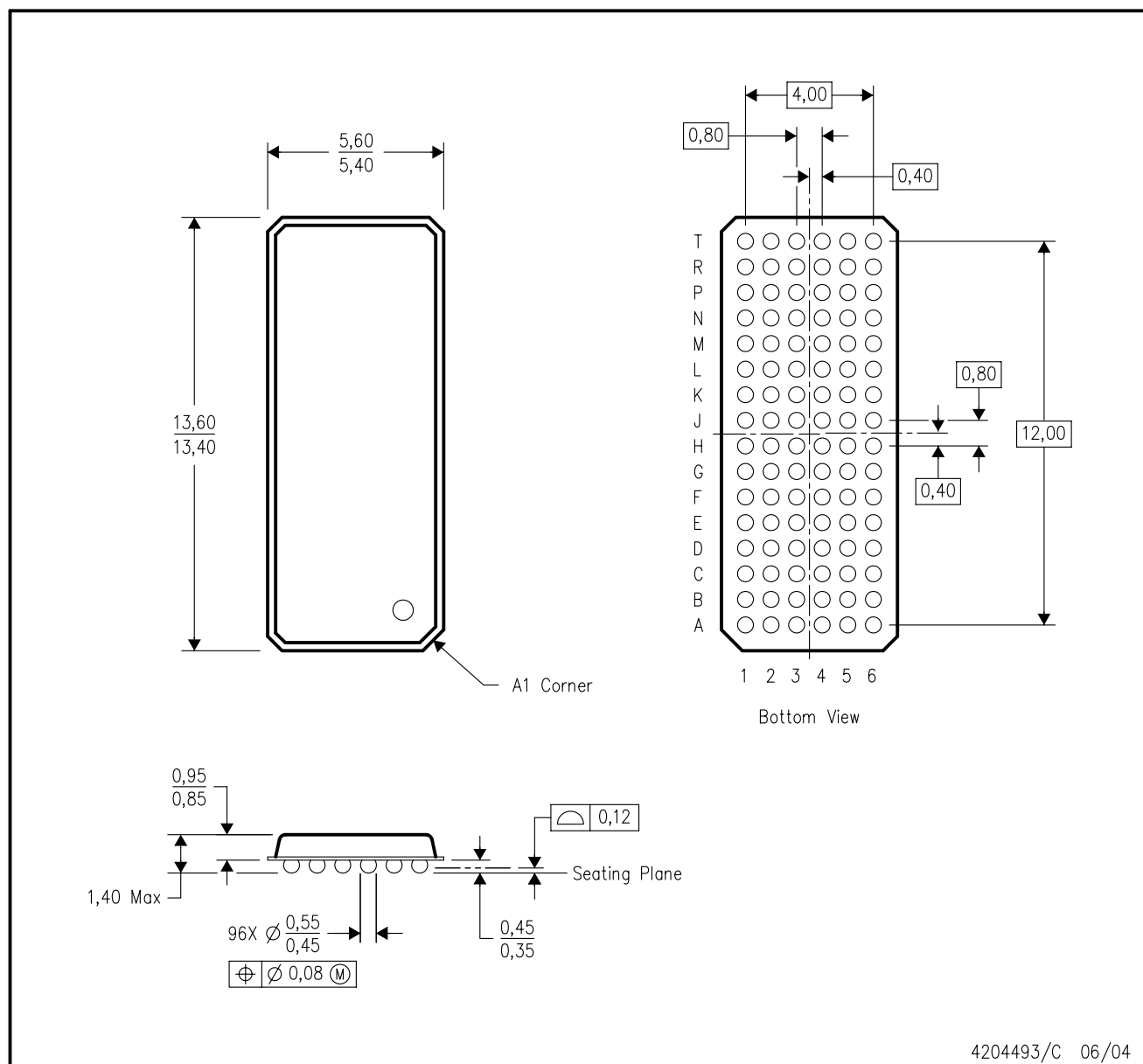
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ZKE (R−PBGA−N96)   PLASTIC BALL GRID ARRAY

5,60
5,40

13,60
13,40

A1 Corner

4,00

0,80

0,40

T
R
P
N
M
L
K
J
H
G
F
E
D
C
B
A

0,80

12,00

0,40

1 2 3 4 5 6

Bottom View

0,95
0,85

1,40 Max

96X Ø 0,55
       0,45

⊕ Ø 0,08 Ⓜ

0,12

Seating Plane

0,45
0,35

4204493/C 06/04

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MO−205 variation CC.
         D.   This package is lead−free. Refer to the 96 GKE package (drawing 4188953) for tin−lead (SnPb).

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