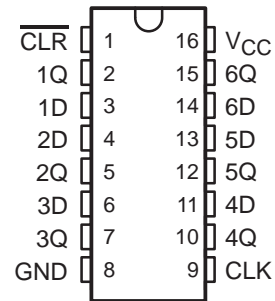


# SN74F174A HEX D-TYPE FLIP-FLOP WITH CLEAR

SDFS029B – D2932, MARCH 1987 – REVISED OCTOBER 1993

- Contains Six Flip-Flops With Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators
- Fully Buffered Outputs for Maximum Isolation From External Disturbances
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

D OR N PACKAGE  
(TOP VIEW)



## description

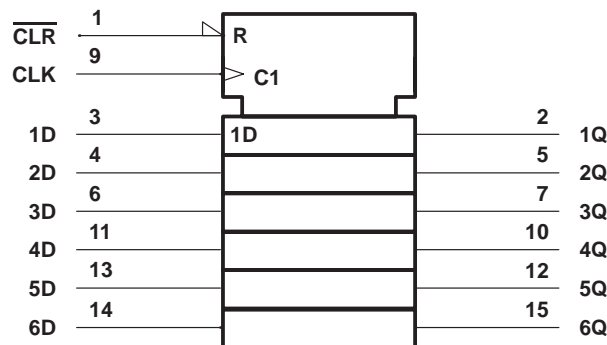
This monolithic, positive-edge-triggered flip-flop utilizes TTL circuitry to implement D-type flip-flop logic with a direct clear (CLR) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

The SN74F174A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT
$\overline{\text{CLR}}$	CLK	D	Q
H	L	X	$Q_0$
H	↑	H	H
H	↑	L	L
L	X	X	L

## logic symbol†

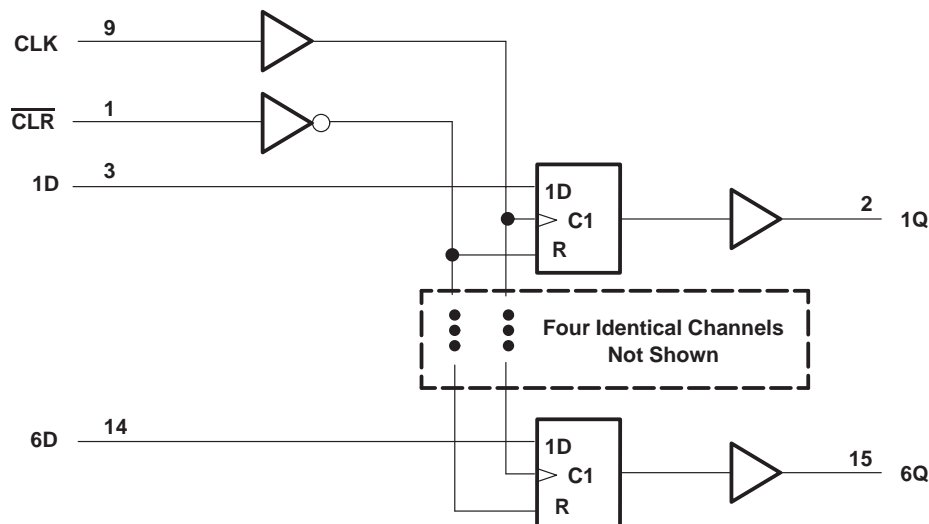


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# SN74F174A HEX D-TYPE FLIP-FLOP WITH CLEAR

SDFS029B – D2932, MARCH 1987 – REVISED OCTOBER 1993

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-1.2 V to 7 V
Input current range .....	-30 mA to 5 mA
Voltage applied to any output in the high state .....	-0.5 V to $V_{CC}$
Current into any output in the low state .....	40 mA
Operating free-air temperature range .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

## recommended operating conditions

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-1	mA
$I_{OL}$	Low-level output current			20	mA
$T_A$	Operating free-air temperature	0		70	°C

# SN74F174A HEX D-TYPE FLIP-FLOP WITH CLEAR

SDFS029B – D2932, MARCH 1987 – REVISED OCTOBER 1993

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2	V
$V_{OH}$	$V_{CC} = 4.5\text{ V}$ ,	$I_{OH} = -1\text{ mA}$	2.5	3.4		V
	$V_{CC} = 4.75\text{ V}$ ,	$I_{OH} = -1\text{ mA}$	2.7			
$V_{OL}$	$V_{CC} = 4.5\text{ V}$ ,	$I_{OL} = 20\text{ mA}$		0.3	0.5	V
$I_I$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 7\text{ V}$			0.1	mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$			20	$\mu\text{A}$
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.5\text{ V}$			-0.6	mA
$I_{OS}‡$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0$	-60		-150	mA
$I_{CCH}$	$V_{CC} = 5.5\text{ V}$ ,	See Note 2		30	45	mA
$I_{CCL}$	$V_{CC} = 5.5\text{ V}$ ,	See Note 3		39	55	mA

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

- NOTES: 2.  $I_{CCH}$  is measured with all outputs open, all data inputs and enable input at 4.5 V, and the clock input at 4.5 V after being momentarily grounded.
3.  $I_{CCL}$  is measured with all outputs open, all data inputs and enable input at 0 V, and the clock input at 4.5 V after being momentarily grounded.

## timing requirements

		$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $T_A = \text{MIN to MAX}§$		UNIT
		MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	0	100	0	80	MHz
$t_w$	Pulse duration	CLK high	4	4		ns
		CLK low	6	6		
		$\overline{\text{CLR}}$ low	5	5		
$t_{\text{su}}$	Setup time before $\text{CLK}\uparrow$	Data high or low	4.5	4.5		ns
		$\overline{\text{CLR}}$ high¶	5	5		
$t_h$	Hold time after $\text{CLK}\uparrow$	Data high or low	0.5	1		ns

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

¶ Inactive-state setup time is also referred to as recovery time.

## switching characteristics (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = 500\ \Omega$ , $T_A = 25^\circ\text{C}$			$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = 500\ \Omega$ , $T_A = \text{MIN to MAX}§$		UNIT
			MIN	TYP	MAX	MIN	MAX	
$f_{\text{max}}$			100	140		80		MHz
$t_{\text{PLH}}$	CLK	Any Q	2.7	4.5	8	2.7	9	ns
$t_{\text{PHL}}$			3.4	4.2	10	3.3	11	
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Any Q	4.2	6.3	14	4.2	15	ns

NOTE 4: Load circuits and waveforms are shown in Section 1.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74F174AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	F174A	<a href="#">Samples</a>
SN74F174ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	F174A	<a href="#">Samples</a>
SN74F174ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	F174A	<a href="#">Samples</a>
SN74F174AN	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN74F174AN	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F174ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F174ADR	SOIC	D	16	2500	333.2	345.9	28.6

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2020, Texas Instruments Incorporated