

## Dual 2-Line To 4-Line Decoders/Demultiplexers

### 1 Features

- Operating voltage range of 4.5 V to 5.5 V
- Outputs can drive up to 10 LSTTL loads
- Low power consumption, 80- $\mu$ A max  $I_{CC}$
- Typical  $t_{pd} = 10$  ns
- $\pm 4$ -mA output drive at 5 V
- Low input current of 1  $\mu$ A max
- Inputs are TTL-voltage compatible
- Designed specifically for high-speed memory decoders and data-transmission systems
- Incorporate two enable inputs to simplify cascading and/or data reception

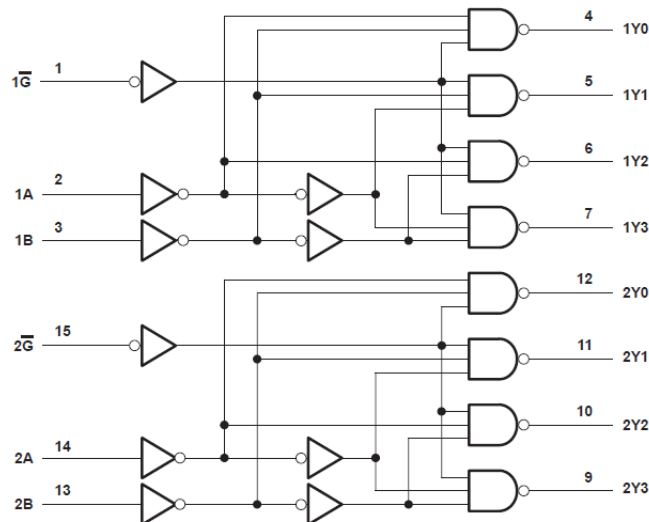
### 2 Description

The 'HCT139 devices are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times.

#### Device Information<sup>(1)</sup>

ORDERABLE PART NUMBER	PACKAGE†	BODY SIZE (NOM)
SN74HCT139	N (PDIP, 16)	19.31 mm × 6.35 mm
	D (SOIC, 16)	9.90 mm × 3.90 mm
	DB (SSOP, 16)	6.2 mm × 5.3 mm
	PW (TSSOP, 16)	5.00 mm × 4.40 mm
SNJ54HCT139	J (CDIP, 16)	24.38 mm × 6.92 mm
	W (CFP, 16)	10.3 mm × 1.65 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



A. Pin numbers shown are for the D, DB, J, N, PW, and W packages.

#### Logic Diagram (Positive Logic)

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### 3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

#### Changes from Revision D (September 2003) to Revision E (August 2022)

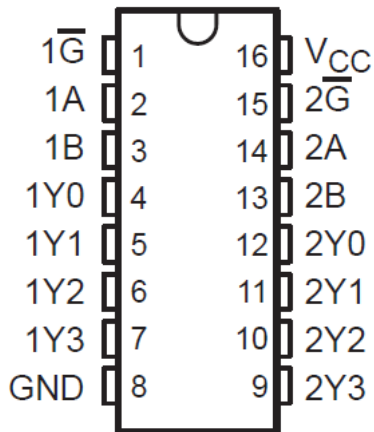
Page

- Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards..... 1

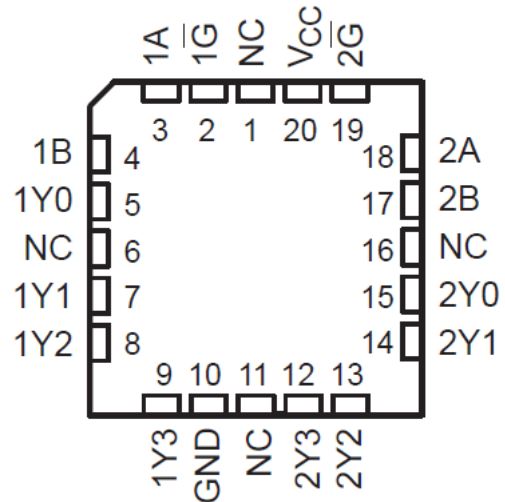
#### 4 Description (continued)

The 'HCT139 devices comprise two individual 2-line to 4-line decoders in a single package. The active-low enable (G) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

#### 5 Pin Configuration and Functions



**Figure 5-1. SN54HCT139 J or W Package  
SN74HCT139 D, DB, N, or PW Package  
Top View**



A. NC - No internal connection

**Figure 5-2. SN54HCT139 FK Package  
Top View**

## 6 Specifications

### 6.1 Absolute Maximum Rating

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub>	±20	mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>	±20	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>	±25	mA
	Continuous current through V <sub>CC</sub> or GND		±50	mA
T <sub>J</sub>	Junction Temperature		150	°C
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 Recommended Operating Conditions<sup>(1)</sup>

		SN54HCT139			SN74HCT139			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V		2	2		V	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V		0.8	0.8		V	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
t <sub>t</sub>	Input transition (rise and fall) time	500		500		ns		
T <sub>A</sub>	Operating free-air temperature	-55	125		-40	85		°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

### 6.3 Thermal Information

THERMAL METRIC <sup>(1)</sup>		D (SOIC)	DB (SSOP)	N (PDIP)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	
R <sub>θJA</sub>	Package thermal impedance	73	82	67	108	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 6.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCT139		SN74HCT139		UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
V <sub>OH</sub> High level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	4.5 V	I <sub>OH</sub> = -20 μA	4.4	4.499		4.4		4.4	V	
			I <sub>OH</sub> = -4 mA	3.98	4.3		3.7		3.84		
V <sub>OL</sub> Low level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	4 V	I <sub>OL</sub> = 20 μA		0.001	0.1		0.1		0.1	V
			I <sub>OL</sub> = 4 mA		0.17	0.26		0.4		0.33	
I <sub>I</sub> Input leakage current V	V <sub>I</sub> = V <sub>CC</sub> or 0	5.5 V		±0.1	±100		±1000		±1000	nA	
I <sub>CC</sub> Supply current	V <sub>I</sub> = V <sub>CC</sub> or 0 I <sub>O</sub> = 0	5.5 V			8		160		80	μA	
ΔI <sub>CC</sub> (1) Supply-Current Change	One input at 0.5 V or 2.4 V, Other inputs at 0 or V <sub>CC</sub>	5.5 V		1.4	2.4		3		2.9	mA	
C <sub>i</sub> Input Capacitance		4.5 V to 5.5 V		3	10		10		10	pF	

(1) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## 6.5 Switching Characteristics

over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see [Figure 7-1](#))

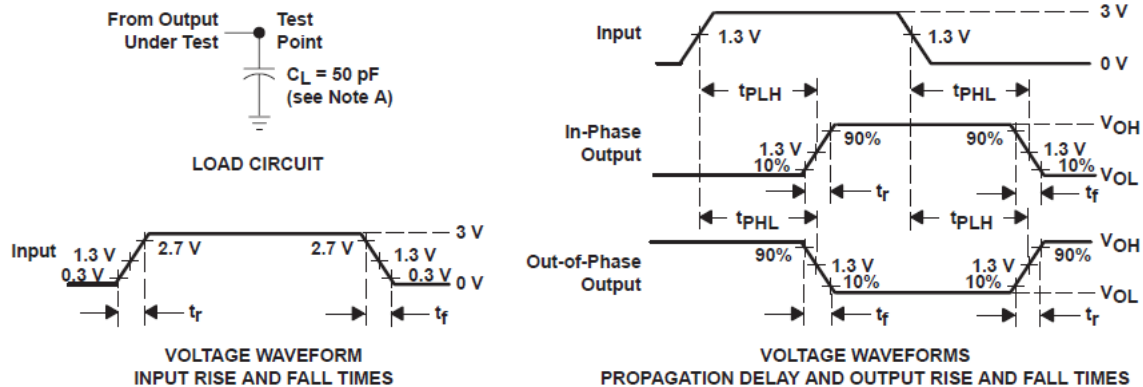
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCT139		SN74HCT139		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	Y	4.5 V		14	34		51		43	ns
			5.5 V		12	30		50		40	
	G	Y	4.5 V		11	34		51		43	
			5.5 V		10	30		50		40	
t <sub>t</sub>		Y	4.5 V		8	15		22		19	ns
			5.5 V		6	14		21		17	

## 6.6 Operating Characteristics

T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per decoder	25	pF

## 7 Parameter Measurement Information



- A.  $C_L$  includes probe and test-fixtue capacitance.
- B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
- C. The outputs are measured one at a time with one input transition per measurement.
- D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 7-1. Load Circuit and Voltage Waveforms**

## 8 Detailed Description

### 8.1 Overview

The 'HCT139 devices are designed for high performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay time of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

### 8.2 Functional Block Diagram

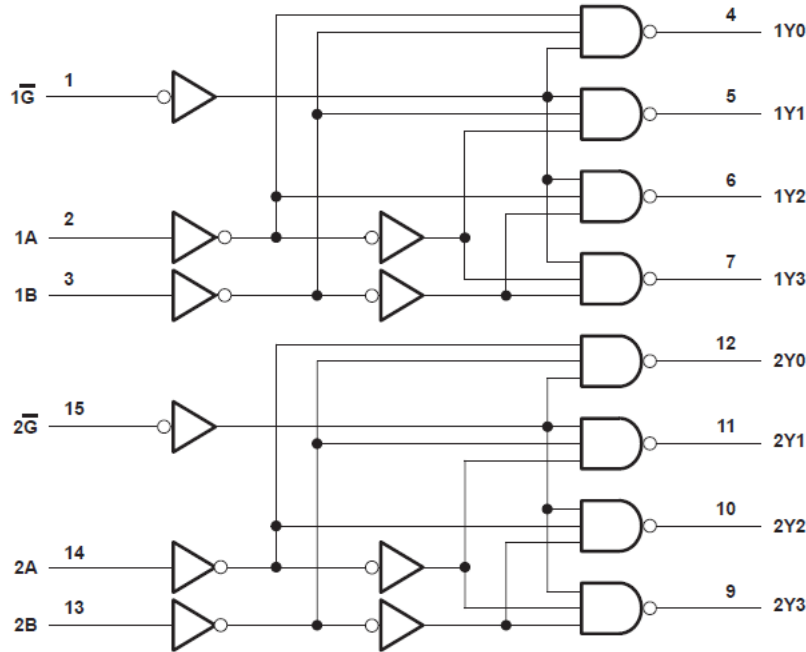


Figure 8-1. Function Diagram

### 8.3 Device Functional Modes

Table 8-1. Function Table

INPUTS <sup>(1)</sup>			OUTPUTS <sup>(2)</sup>			
$\bar{G}$	SELECT		Y0	Y1	Y2	Y3
	B	A				
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

## 9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu\text{F}$  and 1- $\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 10 Layout

### 10.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.



## 11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 11.4 Trademarks

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### 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCT139DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT139	<a href="#">Samples</a>
SN74HCT139DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	HCT139	<a href="#">Samples</a>
SN74HCT139N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT139N	<a href="#">Samples</a>
SN74HCT139PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT139	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT139DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74HCT139DR	SOIC	D	16	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
SN74HCT139DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HCT139PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCT139PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT139DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74HCT139DR	SOIC	D	16	2500	366.0	364.0	50.0
SN74HCT139DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74HCT139PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HCT139PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal



Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74HCT139N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HCT139N	N	PDIP	16	25	506	13.97	11230	4.32

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

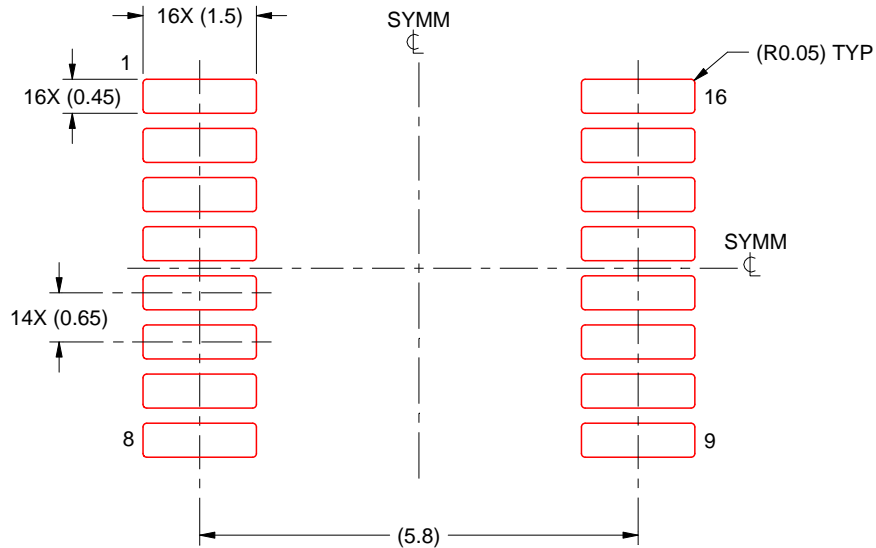
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DB0016A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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