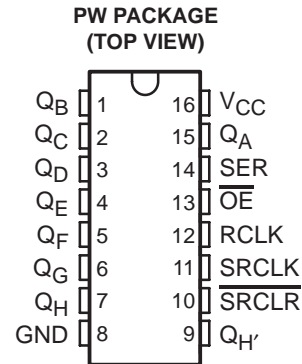


- **Controlled Baseline**
  - One Assembly/Test Site, One Fabrication Site
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **2-V to 5.5-V  $V_{CC}$  Operation**
- **Max  $t_{pd}$  of 7.4 ns at 5 V**
- **Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$**
- **Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2.3$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$**
- **Supports Mixed-Mode Voltage Operation on All Ports**
- **8-Bit Serial-In, Parallel-Out Shift**
- **$I_{off}$  Supports Partial-Power-Down Mode Operation**
- **Shift Register Has Direct Clear**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.



## description/ordering information

The SN74LV595A is an 8-bit shift register designed for 2-V to 5.5-V  $V_{CC}$  operation.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear ( $\overline{\text{SRCLR}}$ ) input, serial (SER) input, and a serial output for cascading. When the output-enable ( $\overline{\text{OE}}$ ) input is high, all outputs except  $Q_{H'}$  are in the high-impedance state.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-40^\circ\text{C}$ to $85^\circ\text{C}$	TSSOP – PW	Reel of 2000	SN74LV595AIPWREP	LV595EP

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2004, Texas Instruments Incorporated

# SN74LV595A-EP

## 8-BIT SHIFT REGISTER

### WITH 3-STATE OUTPUT REGISTERS

SCLS568B – JANUARY 2004 – REVISED MAY 2004

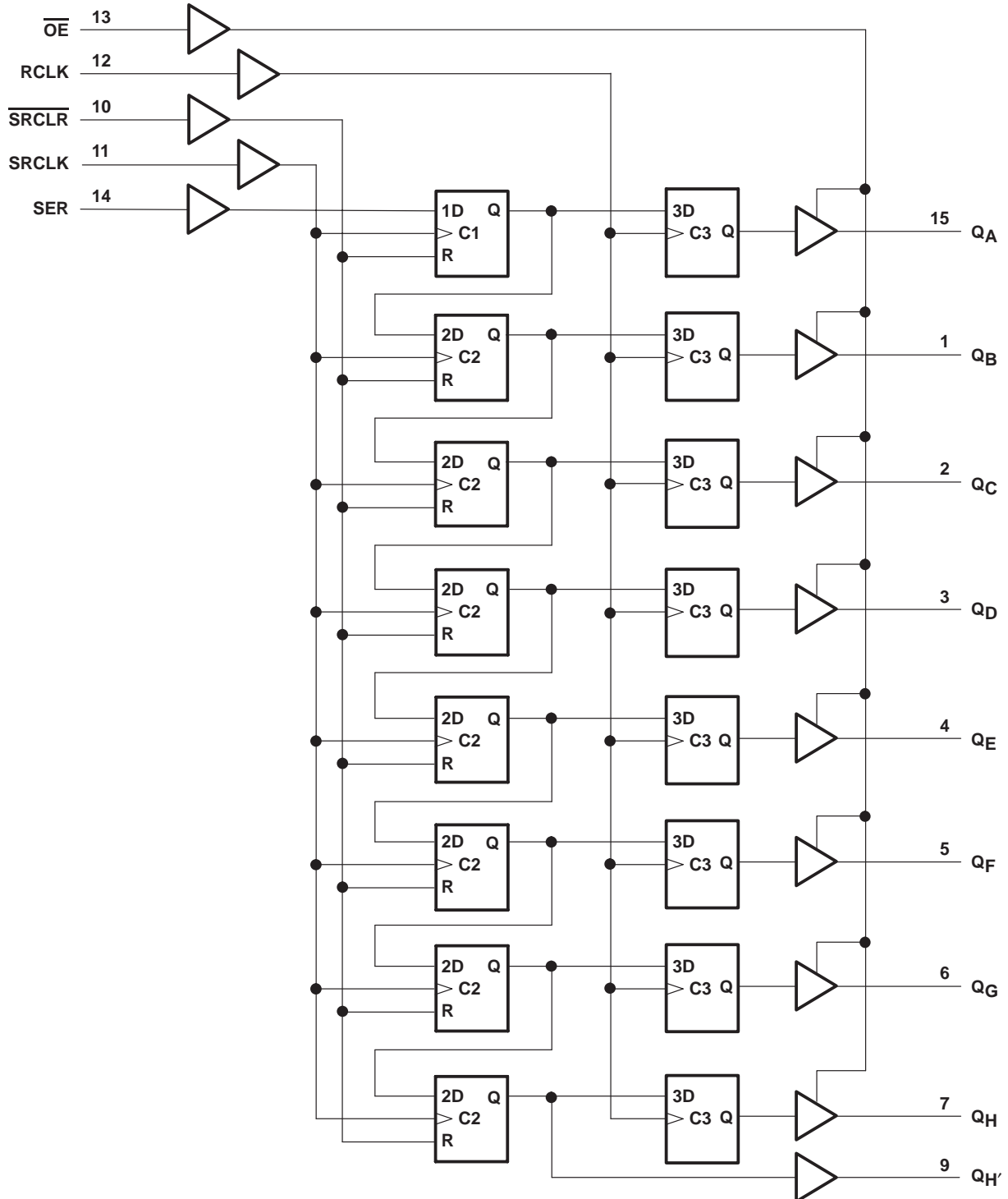
FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{OE}}$	
X	X	X	X	H	Outputs $Q_A$ – $Q_H$ are disabled.
X	X	X	X	L	Outputs $Q_A$ – $Q_H$ are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	↓	H	X	X	Shift-register state is not changed.
X	X	X	↑	X	Shift-register data is stored in the storage register.
X	X	X	↓	X	Storage-register state is not changed.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

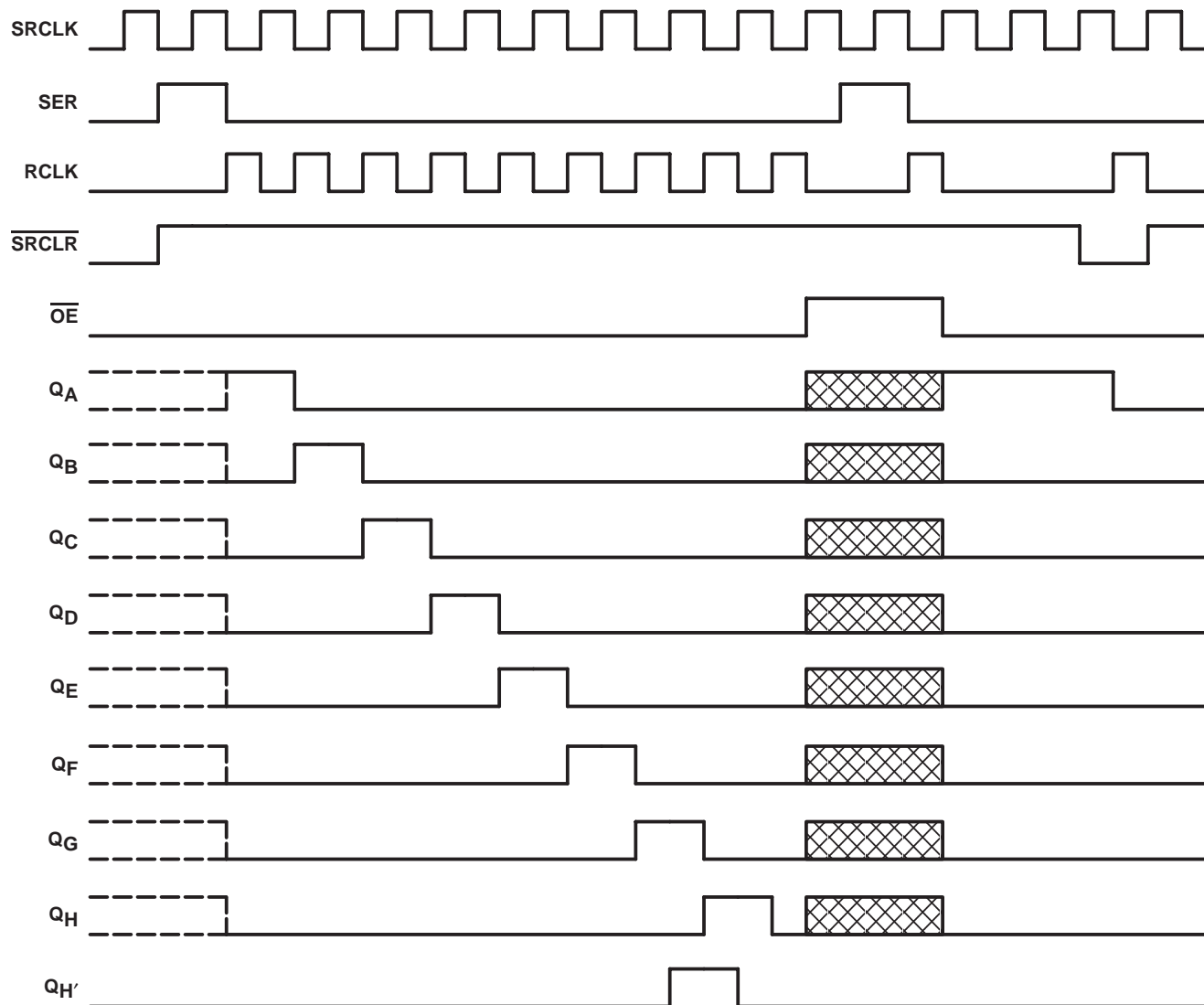
logic diagram (positive logic)



**SN74LV595A-EP**  
**8-BIT SHIFT REGISTER**  
**WITH 3-STATE OUTPUT REGISTERS**

SCLS568B – JANUARY 2004 – REVISED MAY 2004

**timing diagram**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1)	–0.5 V to 7 V
Output voltage range applied in the high or low state, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±35 mA
Continuous current through $V_{CC}$ or GND	±70 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3)	108°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.  
2. This value is limited to 5.5 V maximum.  
3. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 4)**

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5		V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.7$		
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.7$		
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.7$		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V		0.5	V
		$V_{CC} = 2.3$ V to 2.7 V		$V_{CC} \times 0.3$	
		$V_{CC} = 3$ V to 3.6 V		$V_{CC} \times 0.3$	
		$V_{CC} = 4.5$ V to 5.5 V		$V_{CC} \times 0.3$	
$V_I$	Input voltage		0	5.5	V
$V_O$	Output voltage	High or low state	0	$V_{CC}$	V
		3-state	0	5.5	
$I_{OH}$	High-level output current	$V_{CC} = 2$ V		–50	µA
		$V_{CC} = 2.3$ V to 2.7 V		–2	mA
		$V_{CC} = 3$ V to 3.6 V		–8	
		$V_{CC} = 4.5$ V to 5.5 V		–16	
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V		50	µA
		$V_{CC} = 2.3$ V to 2.7 V		2	mA
		$V_{CC} = 3$ V to 3.6 V		8	
		$V_{CC} = 4.5$ V to 5.5 V		16	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3$ V to 2.7 V		200	ns/V
		$V_{CC} = 3$ V to 3.6 V		100	
		$V_{CC} = 4.5$ V to 5.5 V		20	
$T_A$	Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74LV595A-EP

## 8-BIT SHIFT REGISTER

### WITH 3-STATE OUTPUT REGISTERS

SCLS568B – JANUARY 2004 – REVISED MAY 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	2 V to 5.5 V	V <sub>CC</sub> -0.1			V
	I <sub>OH</sub> = -2 mA	2.3 V	2			
	Q <sub>H</sub> '	3 V	2.48			
	Q <sub>A</sub> -Q <sub>H</sub>		2.48			
	Q <sub>H</sub> '	4.5 V	3.8			
	Q <sub>A</sub> -Q <sub>H</sub>		3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	2 V to 5.5 V			0.1	V
	I <sub>OL</sub> = 2 mA	2.3 V			0.4	
	Q <sub>H</sub> '	3 V			0.44	
	Q <sub>A</sub> -Q <sub>H</sub>				0.44	
	Q <sub>H</sub> '	4.5 V			0.55	
	Q <sub>A</sub> -Q <sub>H</sub>				0.55	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±1	µA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±5	µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			20	µA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0			5	µA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		3.5		pF

timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

		T <sub>A</sub> = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t <sub>w</sub>	Pulse duration	SRCLK high or low		7	7.5	ns
		RCLK high or low		7	7.5	
		SRCLR low		6	6.5	
t <sub>su</sub>	Setup time	SER before SRCLK↑		5.5	5.5	ns
		SRCLK↑ before RCLK↑†		8	9	
		SRCLR low before RCLK↑		8.5	9.5	
		SRCLR high (inactive) before SRCLK↑		4	4	
t <sub>h</sub>	Hold time	SER after SRCLK↑		1.5	1.5	ns

† This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
$t_w$	Pulse duration	SRCLK high or low	5.5	5.5	ns	
		RCLK high or low	5.5	5.5		
		$\overline{\text{SRCLR}}$ low	5	5		
$t_{su}$	Setup time	SER before SRCLK $\uparrow$	3.5	3.5	ns	
		SRCLK $\uparrow$ before RCLK $\uparrow$ $\dagger$	8	8.5		
		$\overline{\text{SRCLR}}$ low before RCLK $\uparrow$	8	9		
		$\overline{\text{SRCLR}}$ high (inactive) before SRCLK $\uparrow$	3	3		
$t_h$	Hold time	SER after SRCLK $\uparrow$	1.5	1.5	ns	

$\dagger$  This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
$t_w$	Pulse duration	SRCLK high or low	5	5	ns	
		RCLK high or low	5	5		
		$\overline{\text{SRCLR}}$ low	5.2	5.2		
$t_{su}$	Setup time	SER before SRCLK $\uparrow$	3	3	ns	
		SRCLK $\uparrow$ before RCLK $\uparrow$ $\dagger$	5	5		
		$\overline{\text{SRCLR}}$ low before RCLK $\uparrow$	5	5		
		$\overline{\text{SRCLR}}$ high (inactive) before SRCLK $\uparrow$	2.5	2.5		
$t_h$	Hold time	SER after SRCLK $\uparrow$	2	2	ns	

$\dagger$  This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

# SN74LV595A-EP

## 8-BIT SHIFT REGISTER

### WITH 3-STATE OUTPUT REGISTERS

SCLS568B – JANUARY 2004 – REVISED MAY 2004

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f <sub>max</sub>			C <sub>L</sub> = 15 pF	65	80		45		MHz
			C <sub>L</sub> = 50 pF	60	70		40		
t <sub>PLH</sub>	RCLK	Q <sub>A</sub> –Q <sub>H</sub>	C <sub>L</sub> = 15 pF		8.4	14.2	1	15.8	ns
t <sub>PHL</sub>					8.4	14.2	1	15.8	
t <sub>PLH</sub>	SRCLK	Q <sub>H</sub> '			9.4	19.6	1	22.2	
t <sub>PHL</sub>					9.4	19.6	1	22.2	
t <sub>PHL</sub>	$\overline{\text{SRCLR}}$	Q <sub>H</sub> '			8.7	14.6	1	16.3	
t <sub>PZH</sub>	$\overline{\text{OE}}$	Q <sub>A</sub> –Q <sub>H</sub>			8.2	13.9	1	15	
t <sub>PZL</sub>					10.9	18.1	1	20.3	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Q <sub>A</sub> –Q <sub>H</sub>			8.3	13.7	1	15.6	
t <sub>PLZ</sub>					9.2	15.2	1	16.7	
t <sub>PLH</sub>	RCLK	Q <sub>A</sub> –Q <sub>H</sub>	C <sub>L</sub> = 50 pF		11.2	17.2	1	19.3	ns
t <sub>PHL</sub>					11.2	17.2	1	19.3	
t <sub>PLH</sub>	SRCLK	Q <sub>H</sub> '			13.1	22.5	1	25.5	
t <sub>PHL</sub>					13.1	22.5	1	25.5	
t <sub>PHL</sub>	$\overline{\text{SRCLR}}$	Q <sub>H</sub> '			12.4	18.8	1	21.1	
t <sub>PZH</sub>	$\overline{\text{OE}}$	Q <sub>A</sub> –Q <sub>H</sub>			10.8	17	1	18.3	
t <sub>PZL</sub>					13.4	21	1	23	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Q <sub>A</sub> –Q <sub>H</sub>			12.2	18.3	1	19.5	
t <sub>PLZ</sub>					14	20.9	1	22.6	



**SN74LV595A-EP**  
**8-BIT SHIFT REGISTER**  
**WITH 3-STATE OUTPUT REGISTERS**  
SCLS568B – JANUARY 2004 – REVISED MAY 2004

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f <sub>max</sub>			C <sub>L</sub> = 15 pF	80	120		70		MHz
			C <sub>L</sub> = 50 pF	55	105		50		
t <sub>PLH</sub>	RCLK	Q <sub>A</sub> –Q <sub>H</sub>	C <sub>L</sub> = 15 pF	6	11.9		1	13.5	ns
t <sub>PHL</sub>				6	11.9		1	13.5	
t <sub>PLH</sub>	SRCLK	Q <sub>H</sub> '		6.6	13		1	15	
t <sub>PHL</sub>				6.6	13		1	15	
t <sub>PHL</sub>	$\overline{\text{SRCLR}}$	Q <sub>H</sub> '		6.2	12.8		1	13.7	
t <sub>PZH</sub>	$\overline{\text{OE}}$	Q <sub>A</sub> –Q <sub>H</sub>		6	11.5		1	13.5	
t <sub>PZL</sub>				7.8	11.5		1	13.5	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Q <sub>A</sub> –Q <sub>H</sub>		6.1	14.7		1	15.2	
t <sub>PLZ</sub>				6.3	14.7		1	15.2	
t <sub>PLH</sub>	RCLK	Q <sub>A</sub> –Q <sub>H</sub>	C <sub>L</sub> = 50 pF	7.9	15.4		1	17	ns
t <sub>PHL</sub>				7.9	15.4		1	17	
t <sub>PLH</sub>	SRCLK	Q <sub>H</sub> '		9.2	16.5		1	18.5	
t <sub>PHL</sub>				9.2	16.5		1	18.5	
t <sub>PHL</sub>	$\overline{\text{SRCLR}}$	Q <sub>H</sub> '		9	16.3		1	17.2	
t <sub>PZH</sub>	$\overline{\text{OE}}$	Q <sub>A</sub> –Q <sub>H</sub>		7.8	15		1	17	
t <sub>PZL</sub>				9.6	15		1	17	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Q <sub>A</sub> –Q <sub>H</sub>		8.1	15.7		1	16.2	
t <sub>PLZ</sub>				9.3	15.7		1	16.2	

# SN74LV595A-EP

## 8-BIT SHIFT REGISTER

### WITH 3-STATE OUTPUT REGISTERS

SCLS568B – JANUARY 2004 – REVISED MAY 2004

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f <sub>max</sub>			C <sub>L</sub> = 15 pF	135	170		115		MHz
			C <sub>L</sub> = 50 pF	120	140		95		
t <sub>PLH</sub>	RCLK	Q <sub>A</sub> –Q <sub>H</sub>	C <sub>L</sub> = 15 pF		4.3	7.4	1	8.5	ns
t <sub>PHL</sub>					4.3	7.4	1	8.5	
t <sub>PLH</sub>	SRCLK	Q <sub>H</sub> '			4.5	8.2	1	9.4	
t <sub>PHL</sub>					4.5	8.2	1	9.4	
t <sub>PHL</sub>	$\overline{\text{SRCLR}}$	Q <sub>H</sub> '			4.5	8	1	9.1	
t <sub>PZH</sub>	$\overline{\text{OE}}$	Q <sub>A</sub> –Q <sub>H</sub>			4.3	8.6	1	10	
t <sub>PZL</sub>					5.4	8.6	1	10	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Q <sub>A</sub> –Q <sub>H</sub>			2.4	6	1	7.1	
t <sub>PLZ</sub>					2.7	5.1	1	7.2	
t <sub>PLH</sub>	RCLK	Q <sub>A</sub> –Q <sub>H</sub>	C <sub>L</sub> = 50 pF		5.6	9.4	1	10.5	ns
t <sub>PHL</sub>					5.6	9.4	1	10.5	
t <sub>PLH</sub>	SRCLK	Q <sub>H</sub> '			6.4	10.2	1	11.4	
t <sub>PHL</sub>					6.4	10.2	1	11.4	
t <sub>PHL</sub>	$\overline{\text{SRCLR}}$	Q <sub>H</sub> '			6.4	10	1	11.1	
t <sub>PZH</sub>	$\overline{\text{OE}}$	Q <sub>A</sub> –Q <sub>H</sub>			5.7	10.6	1	12	
t <sub>PZL</sub>					6.8	10.6	1	12	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Q <sub>A</sub> –Q <sub>H</sub>			3.5	10.3	1	11	
t <sub>PLZ</sub>					3.4	10.3	1	11	

noise characteristics,  $V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.3		V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.2		V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		2.8		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage		0.99		V

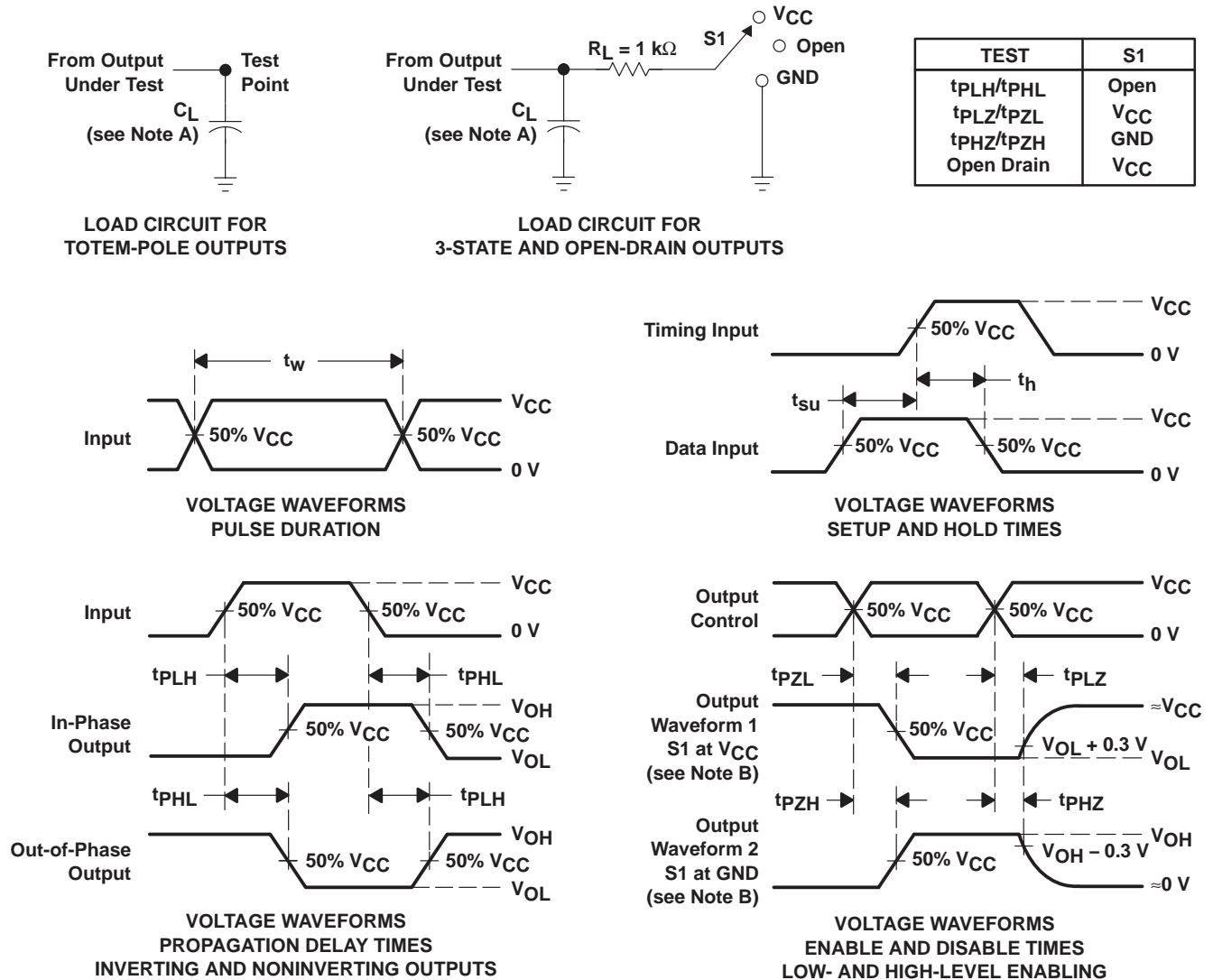
NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$	3.3 V	111	pF
			5 V	114	



## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - D. The outputs are measured one at a time, with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV595AIPWREP	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV595EP	<a href="#">Samples</a>
V62/04696-01XE	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV595EP	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LV595A-EP :**

- Catalog: [SN74LV595A](#)
- Automotive: [SN74LV595A-Q1](#)

**NOTE:** Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV595AIPWREP	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV595AIPWREP	TSSOP	PW	16	2000	367.0	367.0	35.0



4220204/A 02/2017

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2020, Texas Instruments Incorporated