# SN74LVC2G00 Dual 2-Input Positive-NAND Gate

## 1 Features

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V $V_{CC}$ Operation
- Inputs Accept Voltages to 5.5 V
- Max $t_{pd}$ of 4.3 ns at 3.3 V
- Low Power Consumption, 10-μA Max $I_{CC}$
- ±24-mA Output Drive at 3.3 V
- Typical $V_{OLP}$ (Output Ground Bounce) $< 0.8$ V at $V_{CC} = 3.3$ V, $T_A = 25°C$
- Typical $V_{OHV}$ (Output $V_{OH}$ Undershoot) $> 2$ V at $V_{CC} = 3.3$ V, $T_A = 25°C$
- $I_{off}$ Supports Live Insertion, Partial Power Down Mode, and Back Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 1000-V Charged-Device Model

## 2 Applications

- IP Phones: Wired and Wireless
- Optical Modules
- Optical Networking: EPON and Video Over Fiber
- Point-to-Point Microwave Backhaul
- Power: Telecom DC/DC Module: Analog and Digital
- Private Branch Exchanges (PBX)
- TETRA Base Exchanges
- Telecom Base Band Units
- Telecom Shelters: Power Distribution Units (PDU), Power Monitoring Units (PMU), Wireless Battery Monitoring, Remote Electrical Tilt Units (RET), Remote Radio Units (RRU), Tower Mounted Amplifiers (TMA)
- Vector Signal Analyzers and Generators
- Video Conferencing: IP-Based HD
- WiMAX and Wireless Infrastructure Equipment
- Wireless Communications Testers and Wireless Repeaters
- xDSL Modems and DSLAM

## 3 Description

This dual 2-input positive-NAND gate is designed for 1.65-V to 5.5-V $V_{CC}$ operation.

The SN74LVC2G00 device performs the Boolean function $Y = \overline{A \times B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

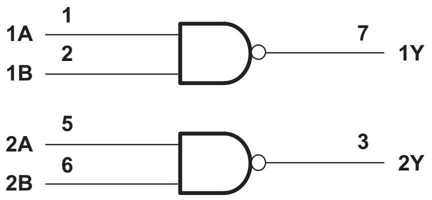
This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**Device Information**[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN74LVC2G00 | SM8 (8) | 2.95 mm × 2.80 mm |
| | US8 (8) | 2.30 mm × 2.00 mm |
| | DSBGA (8) | 1.91 mm × 0.91 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

## 4 Simplified Schematic



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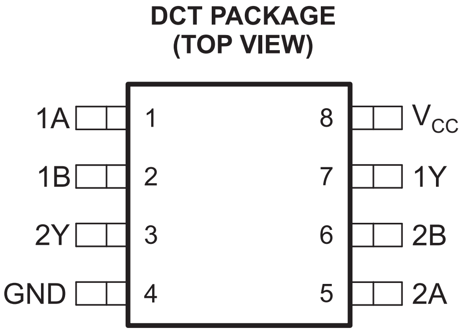
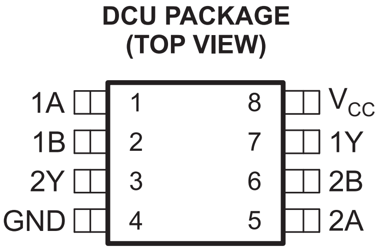
## 5 Revision History

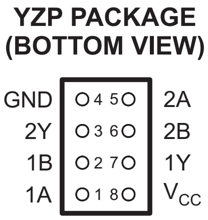
| **Changes from Revision M (November 2013) to Revision N** | **Page** |
|---|---|
| • Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. | 1 |
| • Deleted *Ordering Information* table. | 1 |

| **Changes from Revision L (January 2007) to Revision M** | **Page** |
|---|---|
| • Updated document to new TI data sheet format. | 1 |
| • Updated operating temperature range in *Recommended Operating Conditions* table. | 5 |
| • Added ESD warning. | 12 |

# 6 Pin Configuration and Functions







See mechanical drawings for dimensions.

**Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | DCT, DCU, YZP | | |
| 1A | 1 | I | A input for gate 1 |
| 1B | 2 | I | B input for gate 1 |
| 2Y | 3 | O | Output for gate 2 |
| GND | 4 | — | Ground |
| 2A | 5 | I | A input for gate 2 |
| 2B | 6 | I | B input for gate 2 |
| 1Y | 7 | O | Output for gate 1 |
| $V_{CC}$ | 8 | I | Power input. |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 6.5 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 6.5 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state(2) | | –0.5 | 6.5 | V |
| $V_O$ | Voltage range applied to any output in the high or low state(2)(3) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I < 0$ | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O < 0$ | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The value of $V_{CC}$ is provided in the *Recommended Operating Conditions* table.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | 2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | 1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Operating | 1.65 | 5.5 | V |
| | | Data retention only | 1.5 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | 0.65 × $V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | 2 | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 0.7 × $V_{CC}$ | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | 0.8 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 0.3 × $V_{CC}$ | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | –4 | mA |
| | | $V_{CC}$ = 2.3 V | | –8 | |
| | | $V_{CC}$ = 3 V | | –16 | |
| | | | | –24 | |
| | | $V_{CC}$ = 4.5 V | | –32 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | 8 | |
| | | $V_{CC}$ = 3 V | | 16 | |
| | | | | 24 | |
| | | $V_{CC}$ = 4.5 V | | 32 | |
| Δt/Δv | Input transition rise or fall rate | $V_{CC}$ = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V | | 20 | ns/V |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 10 | |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 5 | |
| $T_A$ | Operating free-air temperature | | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## 7.4 Thermal Information

| THERMAL METRIC(1) | | SN74LVC1G00 | | | UNIT |
|---|---|---|---|---|---|
| | | DCT | DCU | YZP | |
| | | 5 PINS | 5 PINS | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 220 | 227 | 102 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | –40°C to 85°C | | | –40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP (1) | MAX | MIN | TYP (1) | MAX | |
| $V_{OH}$ | $I_{OH}$ = –100 µA | 1.65 V to 5.5 V | $V_{CC}$ – 0.1 | | | $V_{CC}$ – 0.1 | | | V |
| | $I_{OH}$ = –4 mA | 1.65 V | 1.2 | | | 1.2 | | | |
| | $I_{OH}$ = –8 mA | 2.3 V | 1.9 | | | 1.9 | | | |
| | $I_{OH}$ = –16 mA | 3 V | 2.4 | | | 2.4 | | | |
| | $I_{OH}$ = –24 mA | | 2.3 | | | 2.3 | | | |
| | $I_{OH}$ = –32 mA | 4.5 V | 3.8 | | | 3.8 | | | |
| $V_{OL}$ | $I_{OL}$ = 100 µA | 1.65 V to 5.5 V | | | 0.1 | | | 0.1 | V |
| | $I_{OL}$ = 4 mA | 1.65 V | | | 0.45 | | | 0.45 | |
| | $I_{OL}$ = 8 mA | 2.3 V | | | 0.3 | | | 0.3 | |
| | $I_{OL}$ = 16 mA | 3 V | | | 0.4 | | | 0.4 | |
| | $I_{OL}$ = 24 mA | | | | 0.55 | | | 0.55 | |
| | $I_{OL}$ = 32 mA | 4.5 V | | | 0.55 | | | 0.55 | |
| $I_I$ A or B inputs | $V_I$ = 5.5 V or GND | 0 to 5.5 V | | | ±5 | | | ±5 | µA |
| $I_{off}$ | $V_I$ or $V_O$ = 5.5 V | 0 | | | ±10 | | | ±10 | µA |
| $I_{CC}$ | $V_I$ = 5.5 V or GND, $I_O$ = 0 | 1.65 V to 5.5 V | | | 10 | | | 10 | µA |
| $\Delta I_{CC}$ | One input at $V_{CC}$ – 0.6 V,<br>Other inputs at $V_{CC}$ or GND | 3 V to 5.5 V | | | 500 | | | 500 | µA |
| $C_I$ | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 5 | | | | | pF |

(1) All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.

## 7.6 Electrical Characteristics (Continued)

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | $V_{CC}$ = 5 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | TYP | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | f = 10 MHz | 19 | 19 | 20 | 22 | pF |

## 7.7 Switching Characteristics, -40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | –40°C to 85°C | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 5 V ± 0.5 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A or B | Y | 3.7 | 8.6 | 1.6 | 4.8 | 1.1 | 4.3 | 1 | 3.3 | ns |

## 7.8 Switching Characteristics, -40°C to 125°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | –40°C to 125°C | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 5 V ± 0.5 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A or B | Y | 3.7 | 9.4 | 1.6 | 5.5 | 1.1 | 4.9 | 1 | 3.8 | ns |

## 7.9 Typical Characteristics

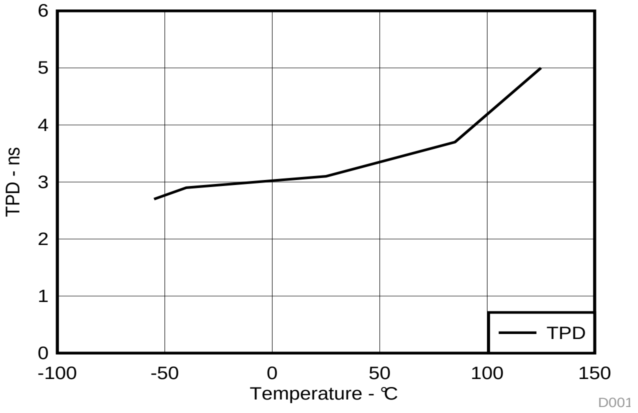


**Figure 1. TPD vs Temperature at 3.3-V $V_{CC}$**

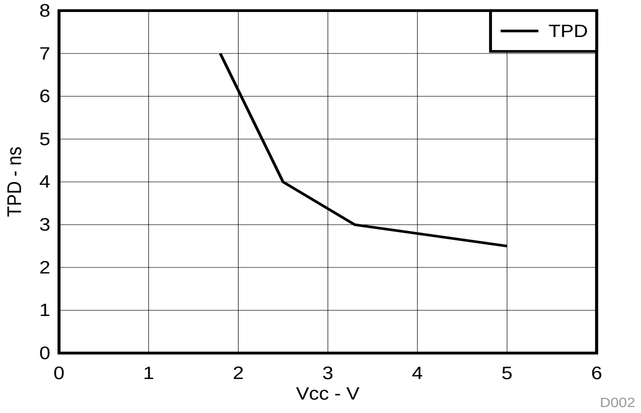
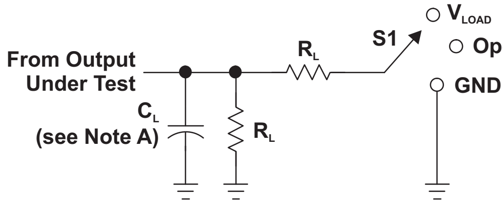


**Figure 2. TPD vs $V_{CC}$ at 25°C**

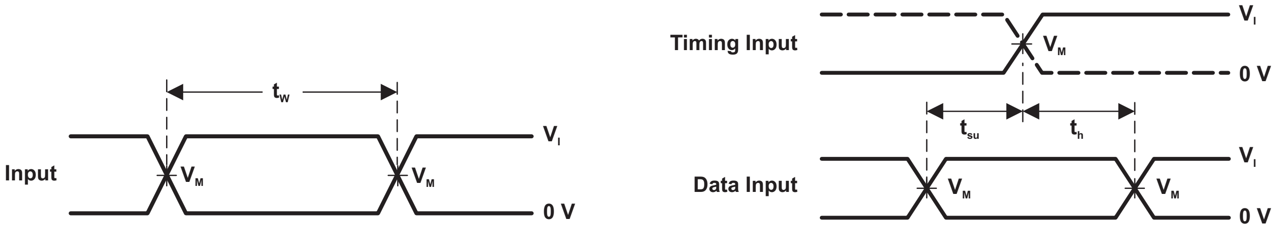
## 8 Parameter Measurement Information



LOAD CIRCUIT

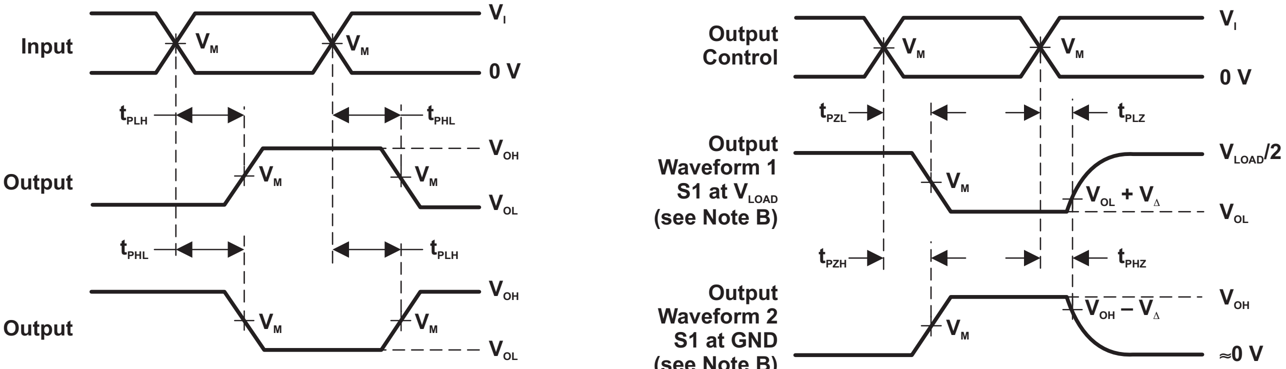
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 3.3 V ± 0.3 V | 3 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 5 V ± 0.5 V | $V_{CC}$ | ≤2.5 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. $C_L$ includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
- F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
- G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
- H. All parameters and waveforms are not applicable to all devices.

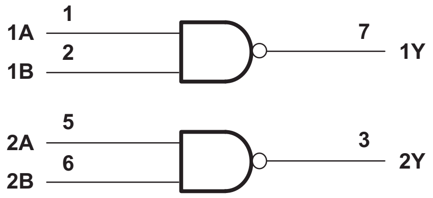
**Figure 3. Load Circuit and Voltage Waveforms**

# 9 Detailed Description

## 9.1 Overview

The SN74LVC2G00 device contains two 2-input positive-NAND gates and performs the Boolean function $Y = \overline{A \times B}$ or $Y = \overline{A} + \overline{B}$ on each gate. This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## 9.2 Functional Block Diagram



## 9.3 Feature Description

- Wide operating voltage range.
  - Operates from 1.65 V to 5.5 V
- Allows down voltage translation
  - Inputs accept voltages to 5.5 V
- $I_{off}$ feature
  - Allows voltages on the inputs and outputs, when $V_{CC}$ is 0 V

## 9.4 Device Functional Modes

**Table 1. Function Table (Each Gate)**

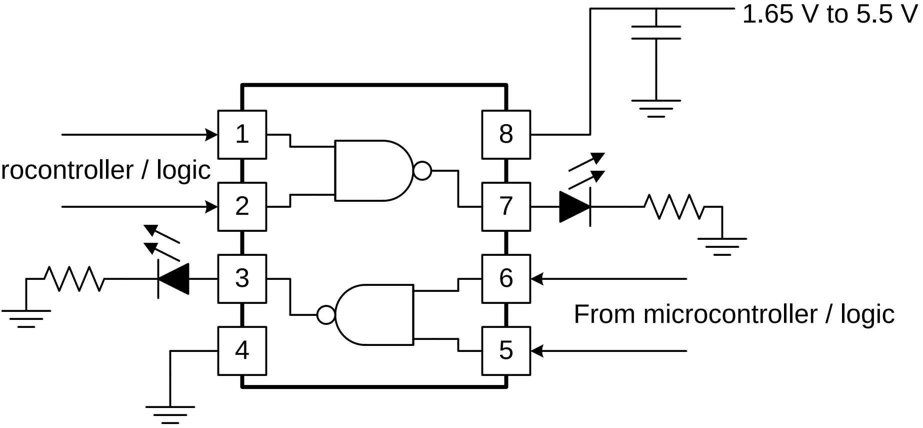
| INPUTS | | OUTPUT |
|---|---|---|
| **A** | **B** | **Y** |
| H | H | L |
| L | X | H |
| X | L | H |

# 10 Application and Implementation

## 10.1 Application Information

SN74LVC2G00 is a high-drive CMOS device that can be used for implementing NAND logic with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V, making it Ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5-V tolerant, allowing it to translate down to $V_{CC}$.

## 10.2 Typical Application



### 10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

### 10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - For rise time and fall time specifications, see (Δt/ΔV) in the *Recommended Operating Conditions* table.
   - For specified high and low levels, see ($V_{IH}$ and $V_{IL}$) in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as ($V_I$ max) in the *Recommended Operating Conditions* table at any valid $V_{CC}$.
2. Recommend Output Conditions
   - Load currents should not exceed ($I_O$ max) per output and should not exceed total current (continuous current through $V_{CC}$ or GND) for the part. These limits are located in the *Absolute Maximum Ratings* table.
   - Outputs should not be pulled above $V_{CC}$.

## Typical Application (continued)

### 10.2.3 Application Curves

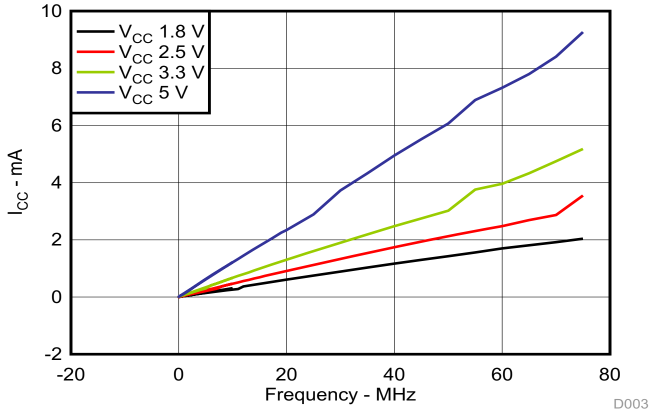


**Figure 4. $I_{CC}$ vs Frequency (Each Gate)**

## 11 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the *Recommended Operating Conditions* table.

Each $V_{CC}$ pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply a 0.1-μF capacitor is recommended and if there are multiple $V_{CC}$ pins then a 0.01-μF or 0.022-μF capacitor is recommended for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

# 12 Layout

## 12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 5 are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$, whichever makes more sense or is more convenient.

## 12.2 Layout Example

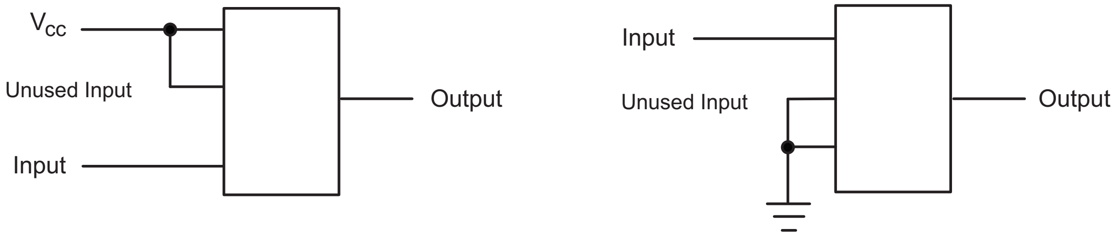


**Figure 5. Layout Diagram**

# 13 Device and Documentation Support

## 13.1 Trademarks

NanoFree is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

# 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC2G00DCT3 | ACTIVE | SM8 | DCT | 8 | 3000 | Pb-Free (RoHS) | CU SNBI | Level-1-260C-UNLIM | -40 to 125 | C00<br>Z | Samples |
| SN74LVC2G00DCTR | ACTIVE | SM8 | DCT | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C00<br>(R, Z) | Samples |
| SN74LVC2G00DCTRE4 | ACTIVE | SM8 | DCT | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C00<br>(R, Z) | Samples |
| SN74LVC2G00DCUR | ACTIVE | VSSOP | DCU | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU SN | Level-1-260C-UNLIM | -40 to 125 | (C00Q, C00R) | Samples |
| SN74LVC2G00DCUT | ACTIVE | VSSOP | DCU | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU SN | Level-1-260C-UNLIM | -40 to 125 | (C00Q, C00R) | Samples |
| SN74LVC2G00DCUTG4 | ACTIVE | VSSOP | DCU | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C00R | Samples |
| SN74LVC2G00YZPR | ACTIVE | DSBGA | YZP | 8 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | CAN | Samples |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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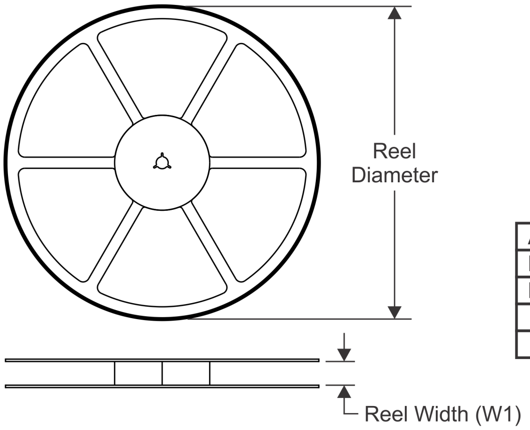
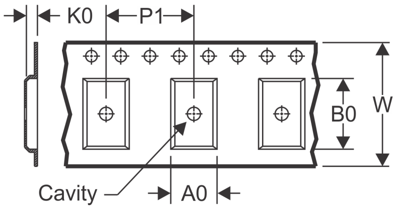
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

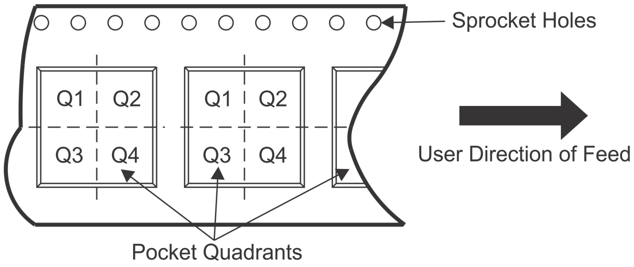


**TAPE DIMENSIONS**



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

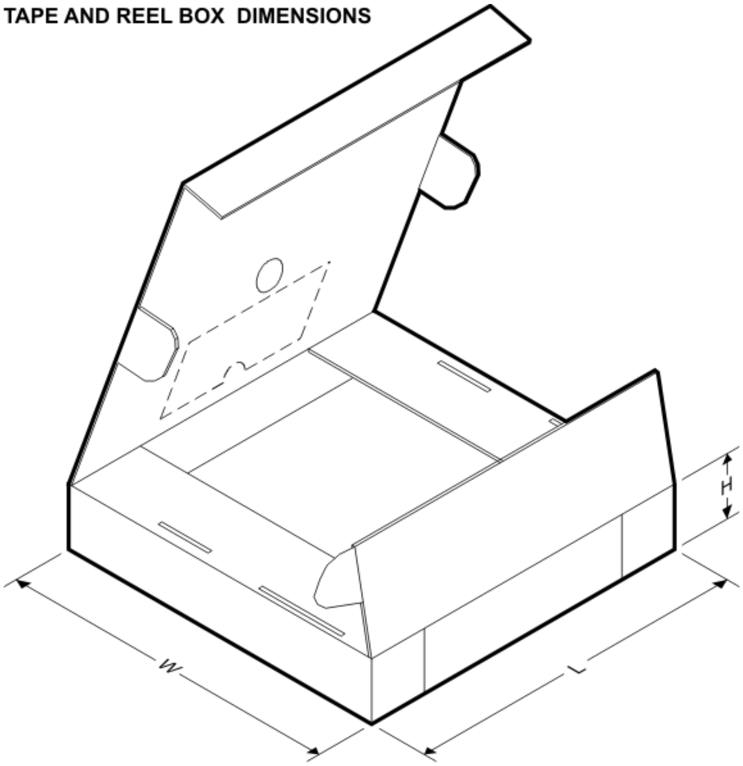
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC2G00DCT3 | SM8 | DCT | 8 | 3000 | 180.0 | 13.0 | 3.35 | 4.5 | 1.55 | 4.0 | 12.0 | Q3 |
| SN74LVC2G00DCTR | SM8 | DCT | 8 | 3000 | 180.0 | 13.0 | 3.35 | 4.5 | 1.55 | 4.0 | 12.0 | Q3 |
| SN74LVC2G00DCUR | VSSOP | DCU | 8 | 3000 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74LVC2G00DCUR | VSSOP | DCU | 8 | 3000 | 178.0 | 9.5 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74LVC2G00DCUT | VSSOP | DCU | 8 | 250 | 178.0 | 9.5 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74LVC2G00DCUTG4 | VSSOP | DCU | 8 | 250 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74LVC2G00YZPR | DSBGA | YZP | 8 | 3000 | 178.0 | 9.2 | 1.02 | 2.02 | 0.63 | 4.0 | 8.0 | Q1 |

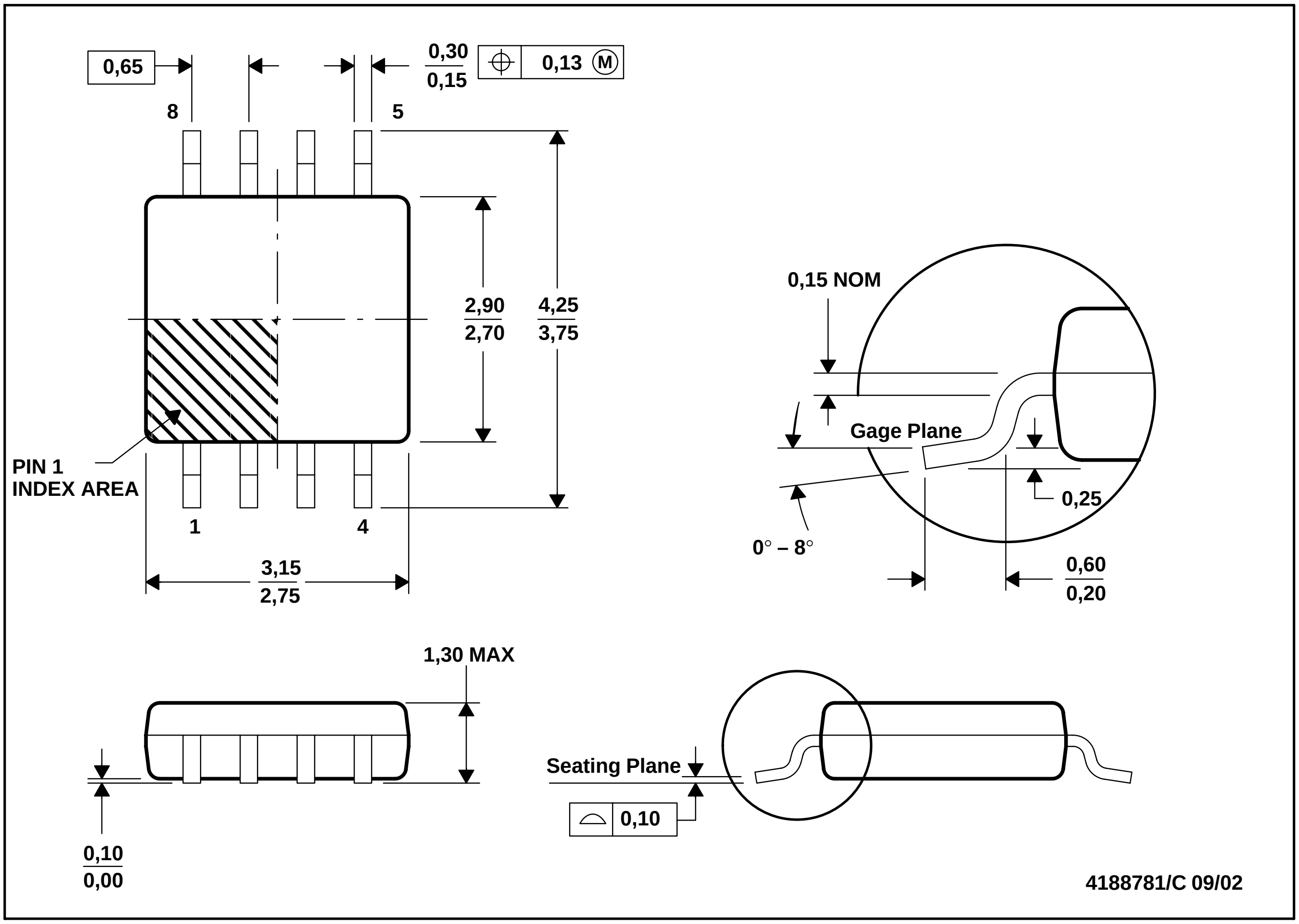
## TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

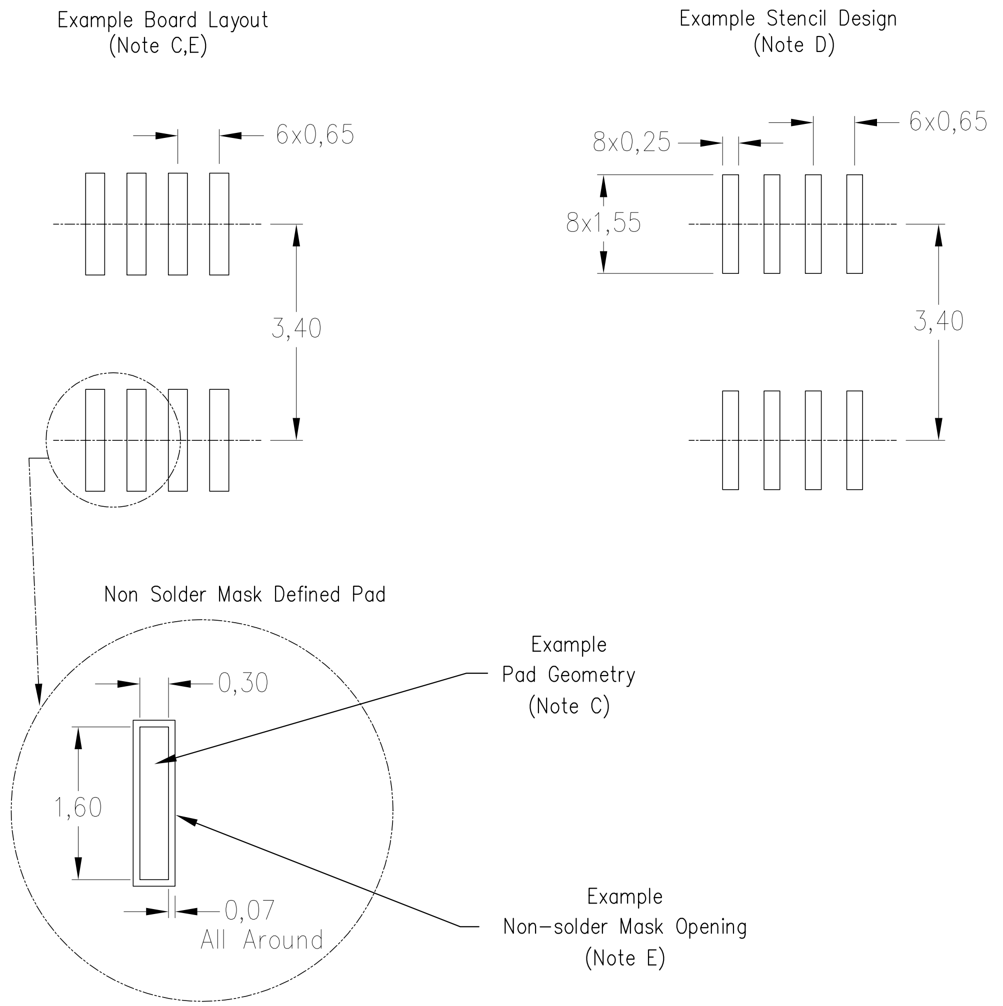
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LVC2G00DCT3 | SM8 | DCT | 8 | 3000 | 182.0 | 182.0 | 20.0 |
| SN74LVC2G00DCTR | SM8 | DCT | 8 | 3000 | 182.0 | 182.0 | 20.0 |
| SN74LVC2G00DCUR | VSSOP | DCU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC2G00DCUR | VSSOP | DCU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC2G00DCUT | VSSOP | DCU | 8 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC2G00DCUTG4 | VSSOP | DCU | 8 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC2G00YZPR | DSBGA | YZP | 8 | 3000 | 220.0 | 220.0 | 35.0 |

## DCT (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- D. Falls within JEDEC MO-187 variation DA.

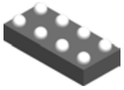
## DCT (R-PDSO-G8) PLASTIC SMALL OUTLINE



4212201/A 10/11

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

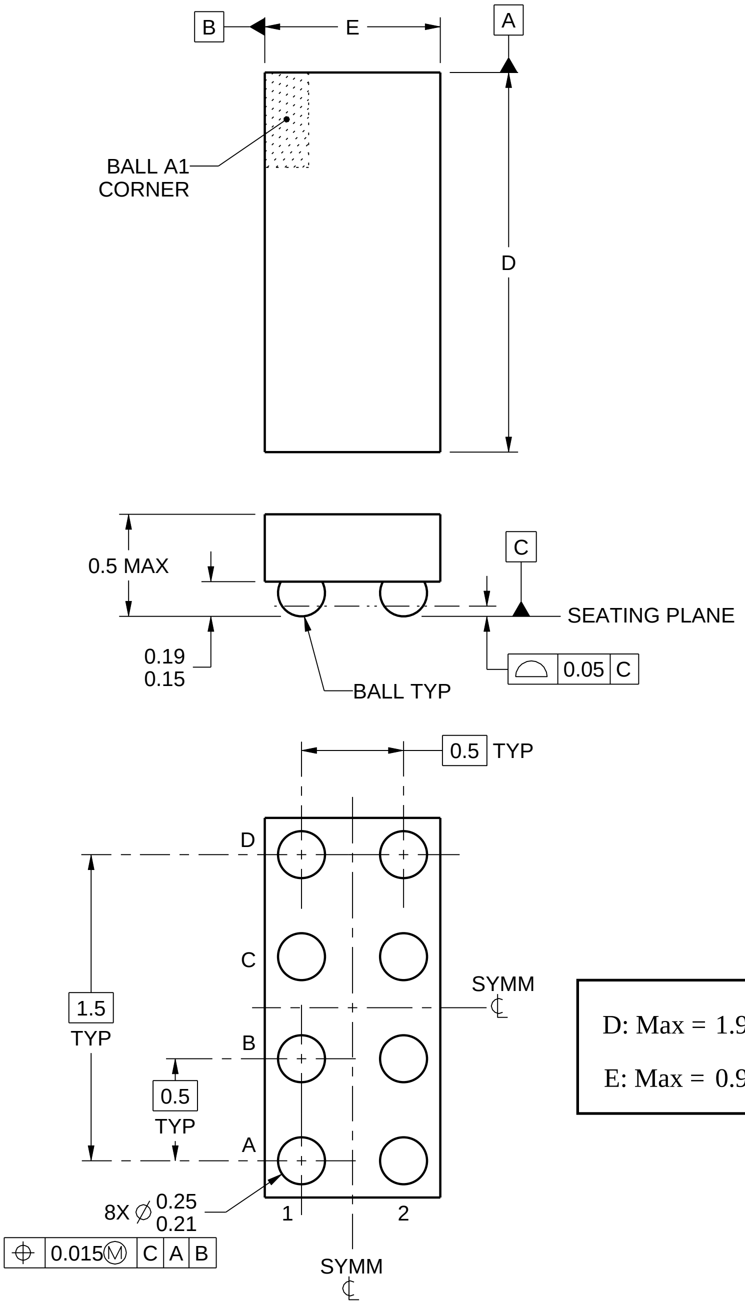
# PACKAGE OUTLINE



# YZP0008

## DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



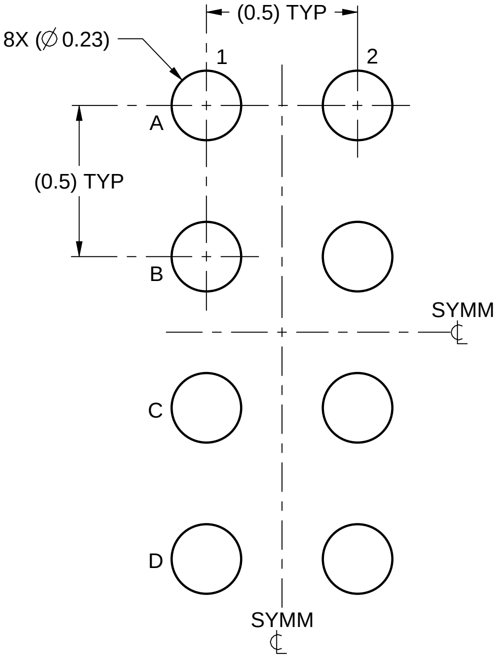
D: Max = 1.919 mm, Min =1.858 mm

E: Max = 0.918 mm, Min =0.857 mm

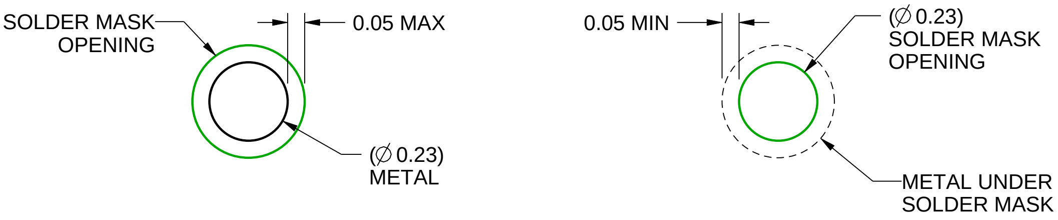
4223082/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X



NON-SOLDER MASK
DEFINED
(PREFERRED)

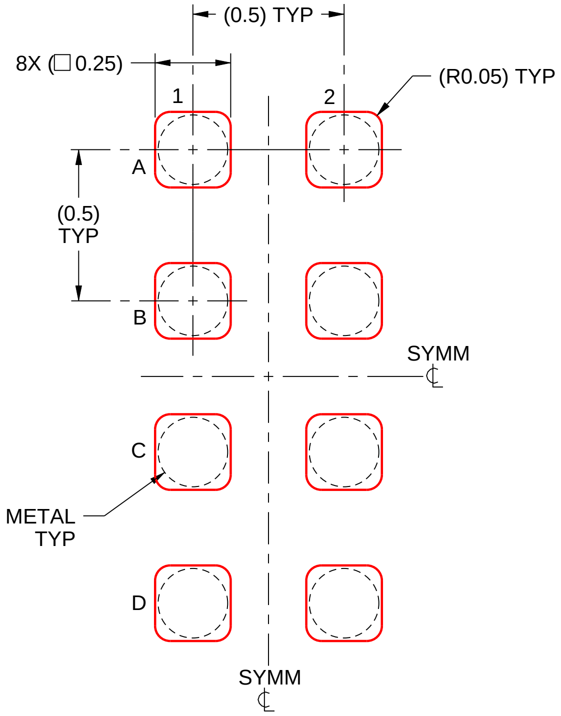
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



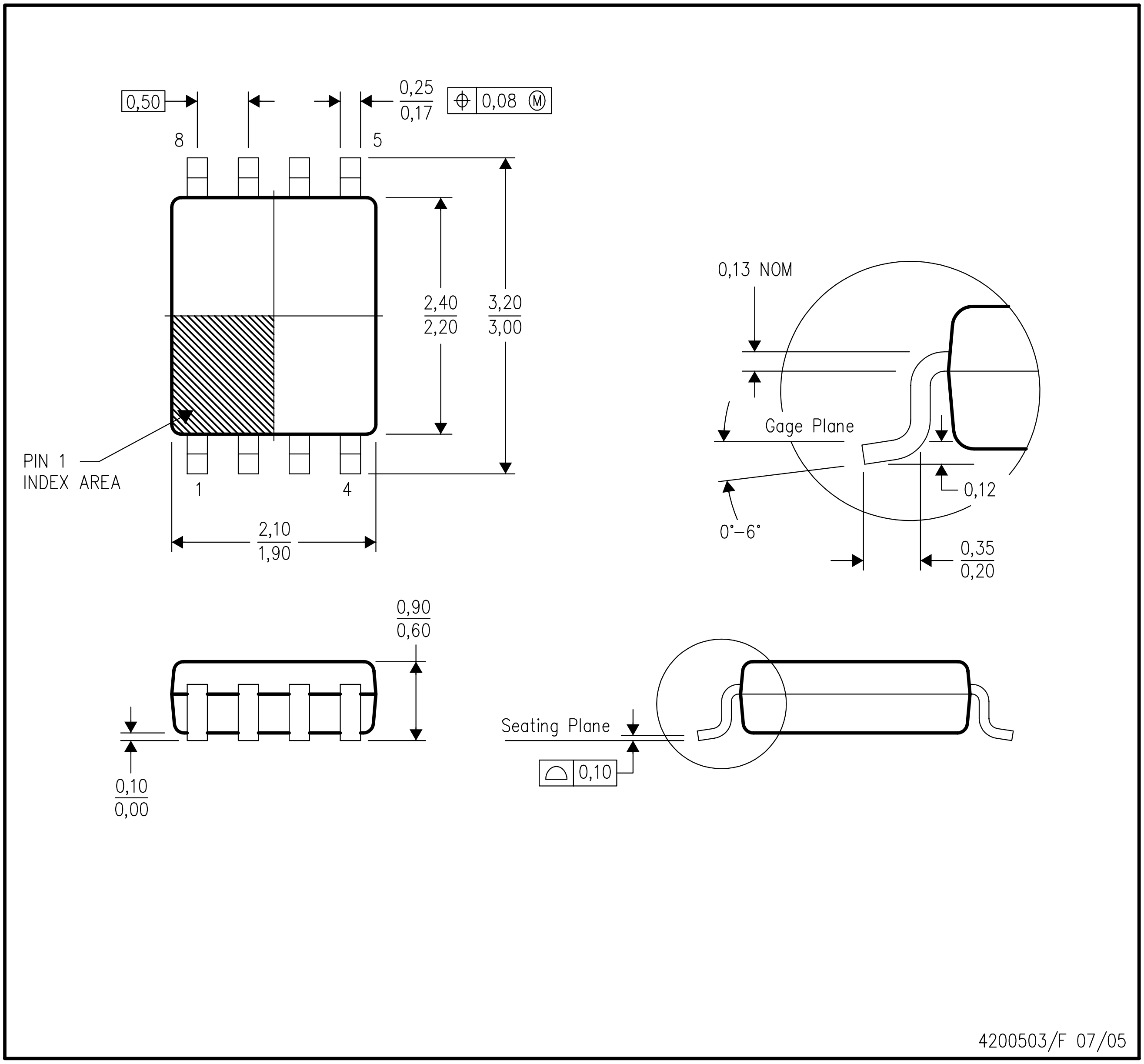
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

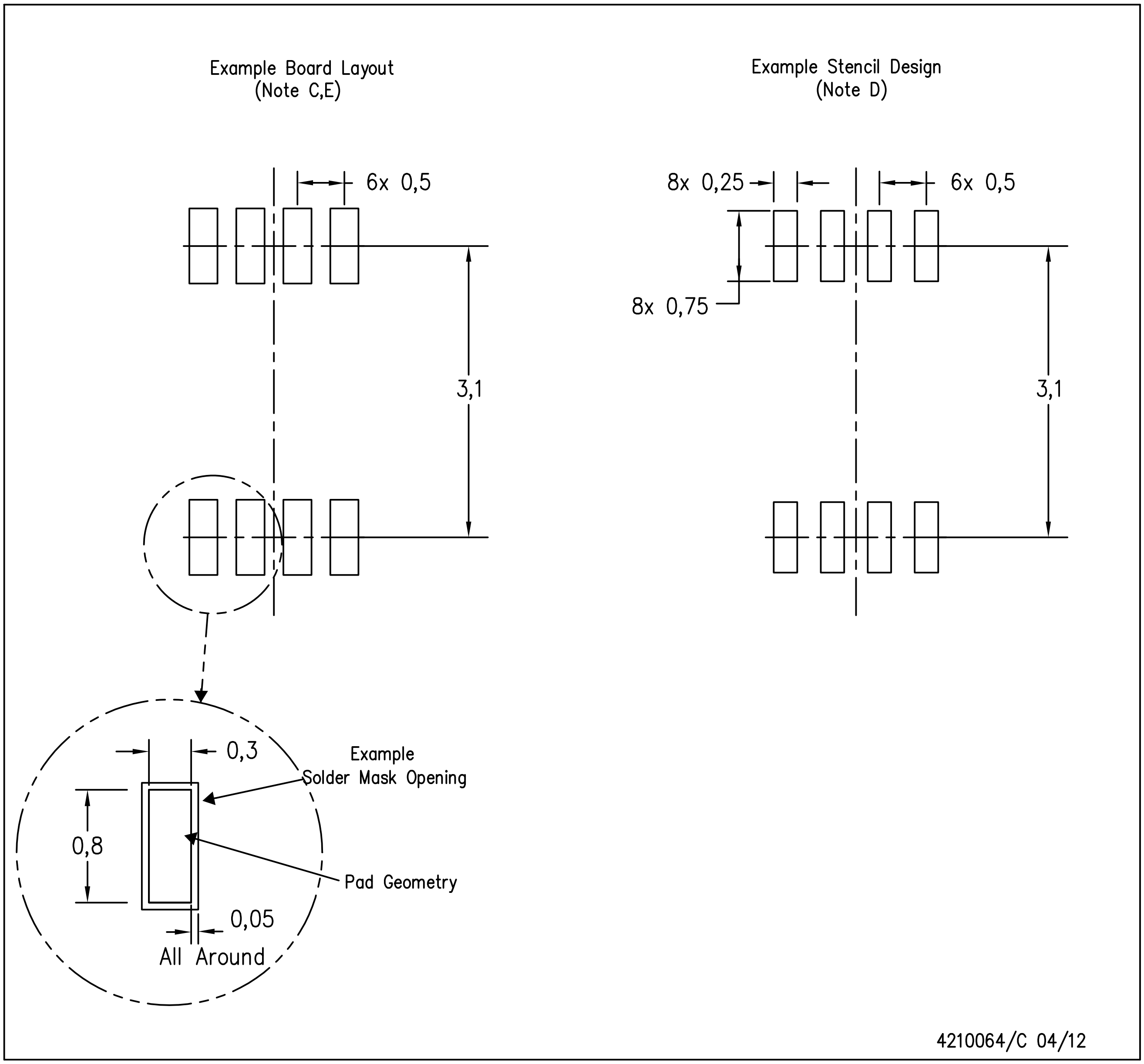
## DCU (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



4200503/F 07/05

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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