## FEATURES

- **Member of the Texas Instruments Widebus+™ Family**
- **Operates From 2.7 V to 3.6 V**
- **Inputs Accept Voltages to 5.5 V**
- **Max $t_{pd}$ of 4.2 ns at 3.3 V**
- **$I_{off}$ and Power-Up 3-State Support Hot Insertion**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V $V_{CC}$)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **1000-V Charged-Device Model (C101)**

## DESCRIPTION/ORDERING INFORMATION

This 32-bit buffer/driver is designed for 2.7-V to 3.6-V $V_{CC}$ operation.

The SN74LVCZ32240A is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as eight 4-bit buffers, four 8-bit buffers, two 16-bit buffers, or one 32-bit buffer. This device provides inverting outputs.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

During power up or power down, when $V_{CC}$ is between 0 and 1.5 V, the device is in the high-impedance state. However, to ensure the high-impedance state above 1.5 V, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

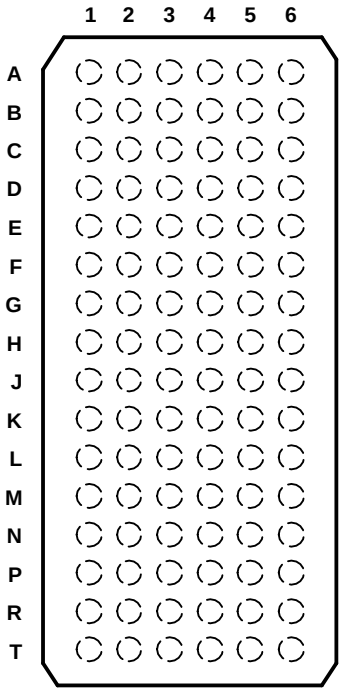
This device is fully specified for hot-insertion applications using $I_{off}$ and power-up 3-state. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down ($V_{CC}$ = 0 V). The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE(1) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | LFBGA – GKE | Tape and reel | SN74LVCZ32240AGKER | ZC240A |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**GKE PACKAGE**
**(TOP VIEW)**



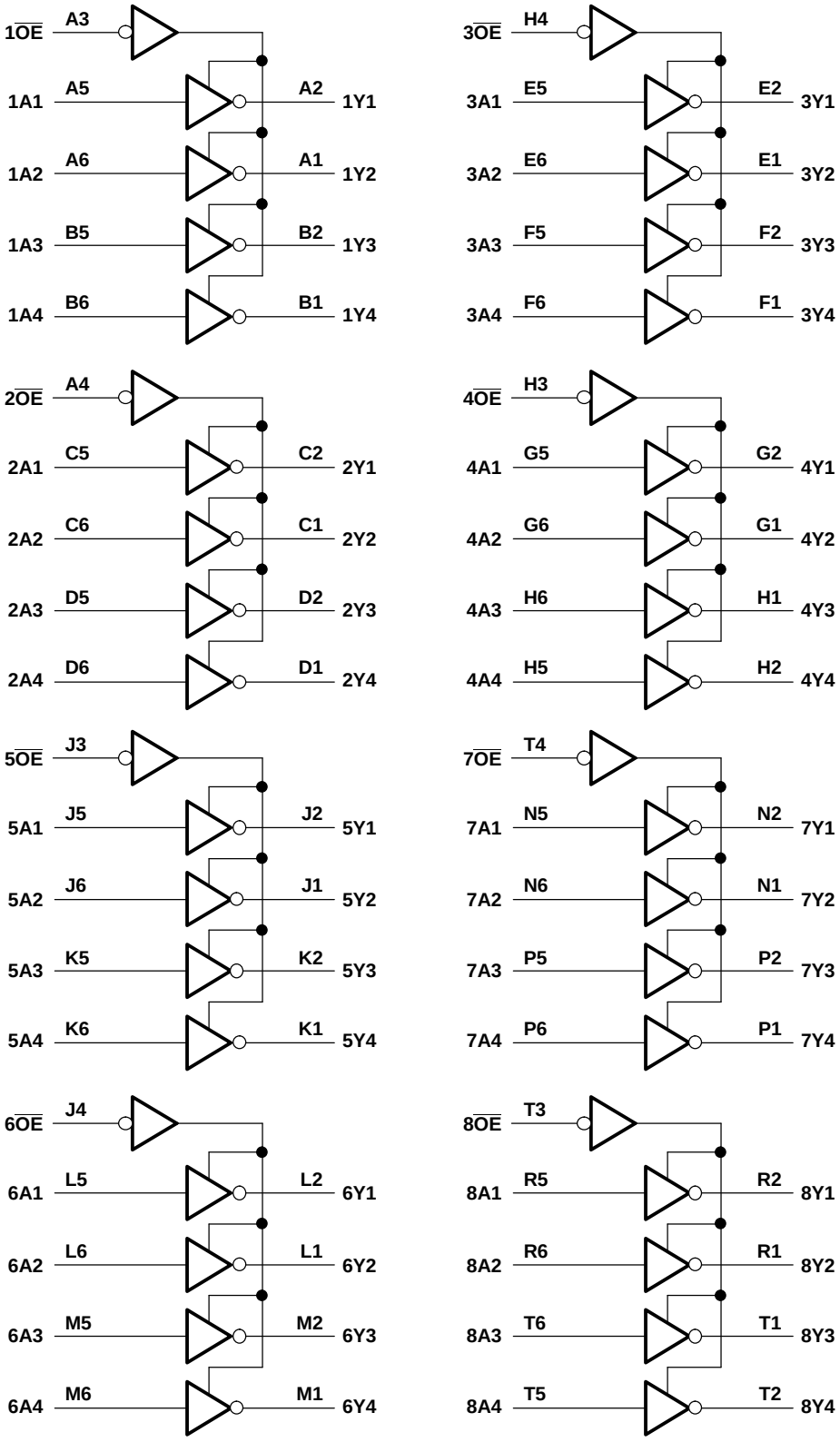

## TERMINAL ASSIGNMENTS

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| **A** | 1Y2 | 1Y1 | $1\overline{OE}$ | $2\overline{OE}$ | 1A1 | 1A2 |
| **B** | 1Y4 | 1Y3 | GND | GND | 1A3 | 1A4 |
| **C** | 2Y2 | 2Y1 | $1V_{CC}$ | $1V_{CC}$ | 2A1 | 2A2 |
| **D** | 2Y4 | 2Y3 | GND | GND | 2A3 | 2A4 |
| **E** | 3Y2 | 3Y1 | GND | GND | 3A1 | 3A2 |
| **F** | 3Y4 | 3Y3 | $1V_{CC}$ | $1V_{CC}$ | 3A3 | 3A4 |
| **G** | 4Y2 | 4Y1 | GND | GND | 4A1 | 4A2 |
| **H** | 4Y3 | 4Y4 | $4\overline{OE}$ | $3\overline{OE}$ | 4A4 | 4A3 |
| **J** | 5Y2 | 5Y1 | $5\overline{OE}$ | $6\overline{OE}$ | 5A1 | 5A2 |
| **K** | 5Y4 | 5Y3 | GND | GND | 5A3 | 5A4 |
| **L** | 6Y2 | 6Y1 | $2V_{CC}$ | $2V_{CC}$ | 6A1 | 6A2 |
| **M** | 6Y4 | 6Y3 | GND | GND | 6A3 | 6A4 |
| **N** | 7Y2 | 7Y1 | GND | GND | 7A1 | 7A2 |
| **P** | 7Y4 | 7Y3 | $2V_{CC}$ | $2V_{CC}$ | 7A3 | 7A4 |
| **R** | 8Y2 | 8Y1 | GND | GND | 8A1 | 8A2 |
| **T** | 8Y3 | 8Y4 | $8\overline{OE}$ | $7\overline{OE}$ | 8A4 | 8A3 |

## FUNCTION TABLE
## (EACH 4-BIT BUFFER)

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | L |
| L | L | H |
| H | X | Z |

## LOGIC DIAGRAM (POSITIVE LOGIC)



## Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 6.5 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 6.5 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state(2) | | –0.5 | 6.5 | V |
| $V_O$ | Voltage range applied to any output in the high or low state(2)(3) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through each $V_{CC}$ or GND | | | ±100 | mA |
| $\theta_{JA}$ | Package thermal impedance(4) | | | 40 | °C/W |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of $V_{CC}$ is provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | V |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | High or low state | 0 | $V_{CC}$ | V |
| | | 3-state | 0 | 5.5 | |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2.7 V | | –12 | mA |
| | | $V_{CC}$ = 3 V | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2.7 V | | 12 | mA |
| | | $V_{CC}$ = 3 V | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 10 | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | | 150 | | µs/V |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | $I_{OH}$ = –100 µA | | 2.7 V to 3.6 V | $V_{CC}$ – 0.2 | | | V |
| | $I_{OH}$ = –12 mA | | 2.7 V | 2.2 | | | |
| | | | 3 V | 2.4 | | | |
| | $I_{OH}$ = –24 mA | | 3 V | 2.2 | | | |
| $V_{OL}$ | $I_{OL}$ = 100 µA | | 2.7 V to 3.6 V | | | 0.2 | V |
| | $I_{OL}$ = 12 mA | | 2.7 V | | | 0.4 | |
| | $I_{OL}$ = 24 mA | | 3 V | | | 0.55 | |
| $I_I$ | $V_I$ = 0 to 5.5 V | | 3.6 V | | | ±5 | A |
| $I_{off}$ | $V_I$ or $V_O$ = 5.5 V | | 0 | | | ±5 | A |
| $I_{OZ}$ | $V_O$ = 0 to 5.5 V | | 3.6 V | | | ±5 | µA |
| $I_{OZPU}$ | $V_O$ = 0.5 V to 2.5 V, | $\overline{OE}$ = don't care | 0 to 1.5 V | | | ±5 | µA |
| $I_{OZPD}$ | $V_O$ = 0.5 V to 2.5 V, | $\overline{OE}$ = don't care | 1.5 V to 0 | | | ±5 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND | $I_O$ = 0 | 3.6 V | | | 200 | µA |
| | 3.6 V ≤ $V_I$ ≤ 5.5 V(2) | | | | | 200 | |
| $\Delta I_{CC}$ | One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | 2.7 V to 3.6 V | | | 100 | µA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | | 3.3 V | | 4.5 | | pF |
| $C_o$ | $V_O$ = $V_{CC}$ or GND | | 3.3 V | | 6 | | pF |

(1) All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
(2) This applies in the disabled state only.

## Switching Characteristics

over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | 1 | 4.5 | 1 | 4.2 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | 1.5 | 5 | 1.5 | 4.7 | ns |
| $t_{dis}$ | $\overline{OE}$ | Y | 1.5 | 6.2 | 1.5 | 5.9 | ns |

## Switching Characteristics

over recommended operating free-air temperature range, $C_L$ = 30 pF (unless otherwise noted) (see Figure 1)

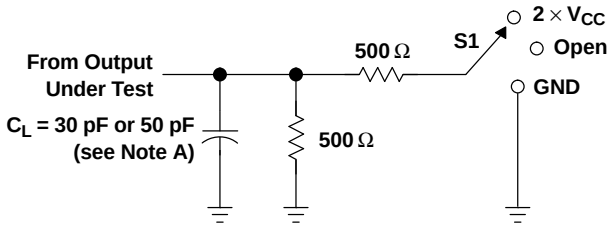
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | 1 | 4.4 | 1 | 4.1 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | 1 | 4.8 | 1 | 4.5 | ns |
| $t_{dis}$ | $\overline{OE}$ | Y | 1.4 | 5.9 | 1.4 | 5.6 | ns |

## Operating Characteristics

$T_A$ = 25°C

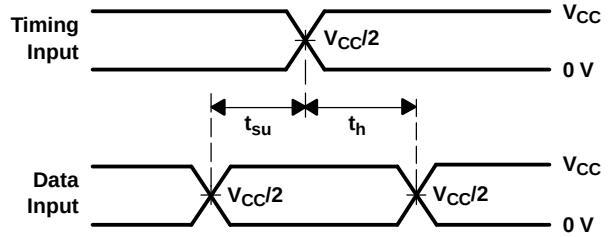
| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ = 3.3 V | UNIT |
|---|---|---|---|---|---|
| | | | | TYP | |
| $C_{pd}$ | Power dissipation capacitance per buffer/driver | Outputs enabled | f = 10 MHz | 31 | pF |
| | | Outputs disabled | | 3.5 | |

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.7 V and 3.3 V ± 0.3 V

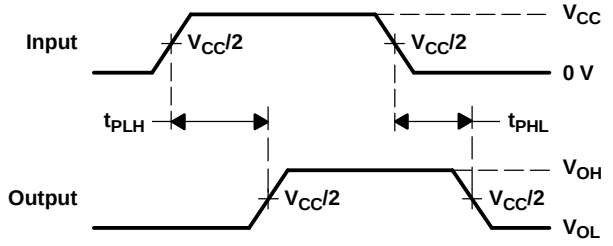



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

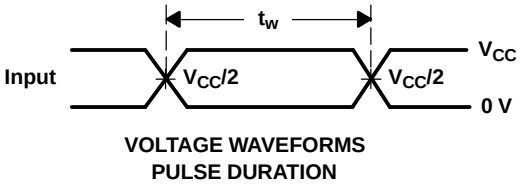
LOAD CIRCUIT



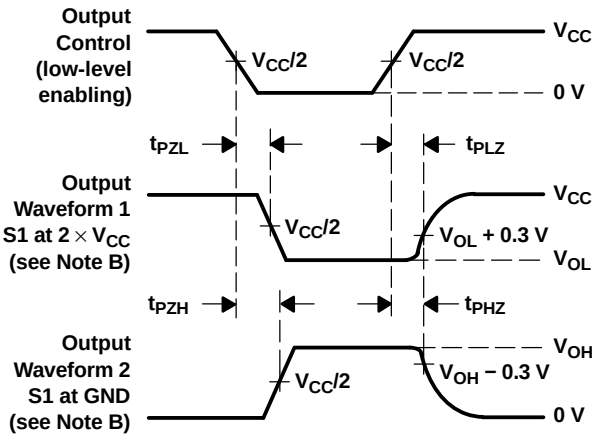

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

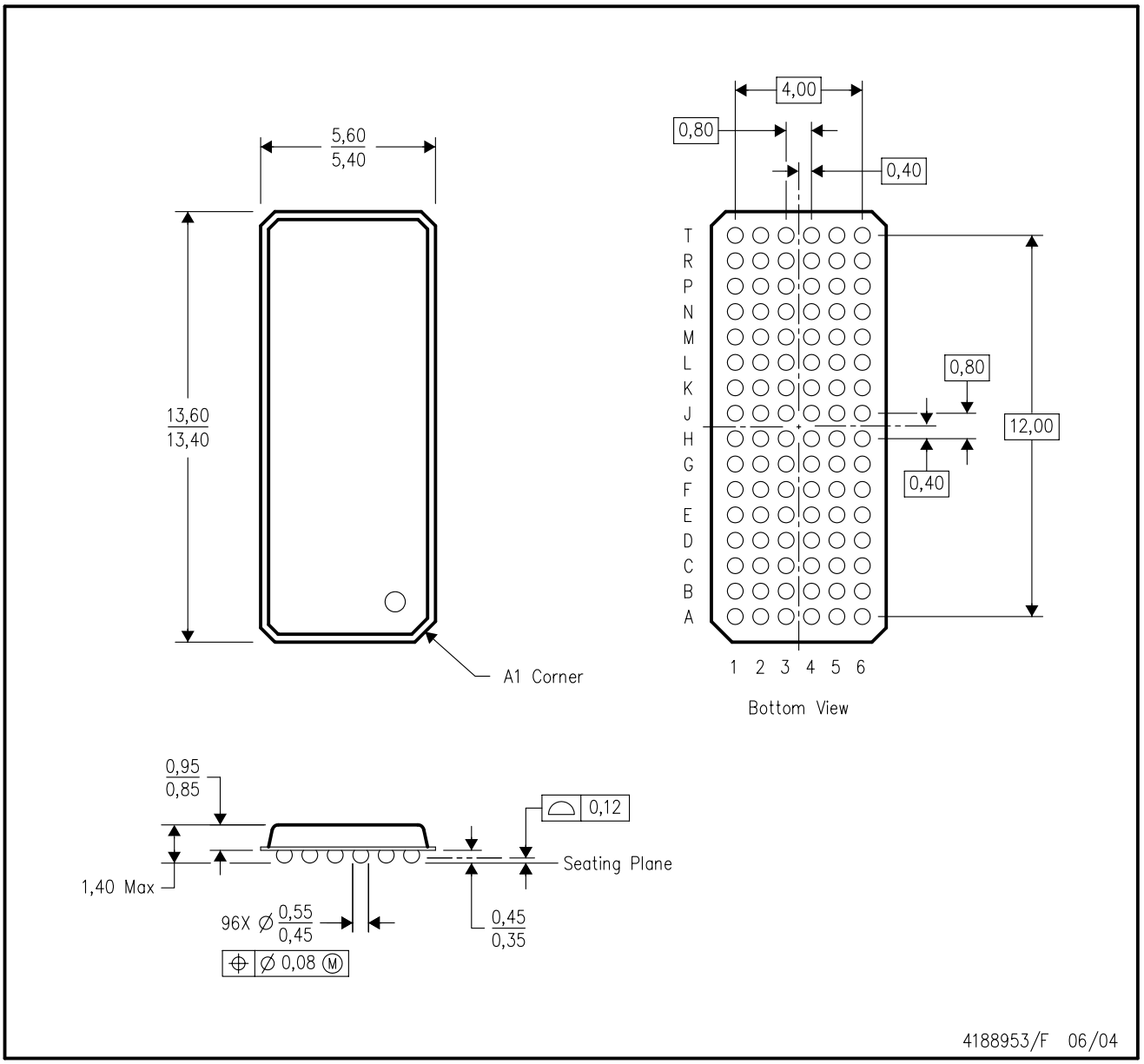
| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| SN74LVCZ32240AGKER | ACTIVE | LFBGA | GKE | 96 | 1000 | TBD | SNPB | Level-3-220C-168 HR |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

GKE (R–PBGA–N96) PLASTIC BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–205 variation CC.
D. This package is tin–lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead–free.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265