SN74SSTV32852
24-BIT TO 48-BIT REGISTERED BUFFER WITH SSTL_2 INPUTS AND OUTPUTS

SCES361C – AUGUST 2001 – REVISED FEBRUARY 2003

- **Member of the Texas Instruments Widebus™ Family**
- **1-to-2 Outputs Support Stacked DDR DIMMs**
- **Supports SSTL_2 Data Inputs**
- **Outputs Meet SSTL_2 Class II Specifications**
- **Differential Clock (CLK and $\overline{\text{CLK}}$) Inputs**
- **Supports LVCMOS Switching Levels on the $\overline{\text{RESET}}$ Input**
- **$\overline{\text{RESET}}$ Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low**
- **Pinout Optimizes DIMM PCB Layout**
- **One Device Per DIMM Required**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **– 2000-V Human-Body Model (A114-A)**
  - **– 1000-V Charged-Device Model (C101)**

description/ordering information

This 24-bit to 48-bit registered buffer is designed for 2.3-V to 2.7-V V_{CC} operation.

All inputs are SSTL_2, except the LVCMOS reset ($\overline{\text{RESET}}$) input. All outputs are SSTL_2, Class II compatible.

The SN74SSTV32852 operates from a differential clock (CLK and $\overline{\text{CLK}}$). Data are registered at the crossing of CLK going high and $\overline{\text{CLK}}$ going low.

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are forced low. The LVCMOS $\overline{\text{RESET}}$ input always must be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	LFBGA – GKF	Tape and reel	SN74SSTV32852GKFR	SV852

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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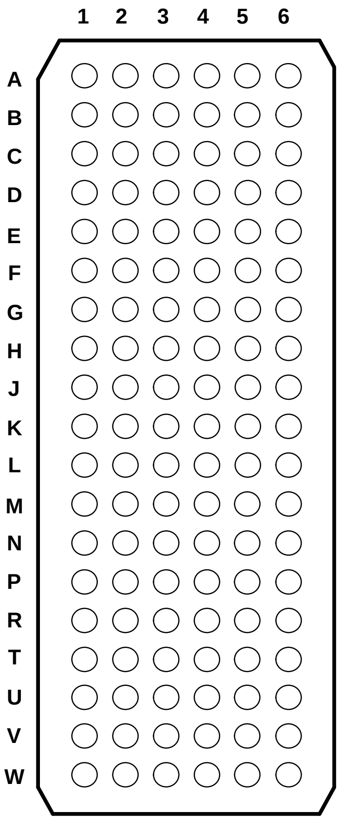
GKF PACKAGE
(TOP VIEW)



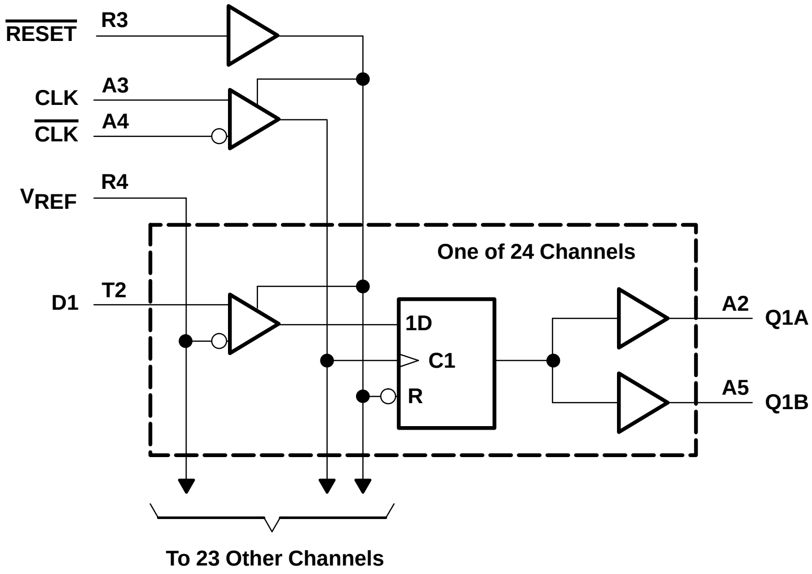
terminal assignments

	1	2	3	4	5	6
A	Q2A	Q1A	CLK	$\overline{\text{CLK}}$	Q1B	Q2B
B	Q3A	V_{DDQ}	GND	GND	V_{DDQ}	Q3B
C	Q5A	Q4A	V_{DDQ}	V_{DDQ}	Q4B	Q5B
D	Q7A	Q6A	GND	GND	Q6B	Q7B
E	Q8A	GND	V_{DDQ}	V_{DDQ}	GND	Q8B
F	Q10A	Q9A	V_{DDQ}	V_{DDQ}	Q9B	Q10B
G	Q12A	Q11A	GND	GND	Q11B	Q12B
H	Q13A	V_{CC}	V_{DDQ}	V_{DDQ}	V_{CC}	Q13B
J	Q14A	Q15A	GND	GND	Q15B	Q14B
K	Q17A	Q16A	V_{DDQ}	V_{DDQ}	Q16B	Q17B
L	Q18A	Q19A	GND	GND	Q19B	Q18B
M	Q20A	V_{DDQ}	GND	GND	V_{DDQ}	Q20B
N	Q22A	Q21A	V_{DDQ}	V_{DDQ}	Q21B	Q22B
P	Q23A	V_{DDQ}	GND	GND	V_{DDQ}	Q23B
R	Q24A	V_{CC}	$\overline{\text{RESET}}$	V_{REF}	V_{CC}	Q24B
T	D2	D1	D6	D18	D13	D14
U	D4	D3	D10	D22	D15	D16
V	D5	D7	D11	D23	D19	D17
W	D8	D9	D12	D24	D21	D20

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{\text{RESET}}$	CLK	$\overline{\text{CLK}}$	D	Q
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q_0
L	X or floating	X or floating	X or floating	L

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} or V_{DDQ}	–0.5 V to 3.6 V
Input voltage range, V_I (see Notes 1 and 2)	–0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to V_{DDQ} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DDQ}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{DDQ})	±50 mA
Continuous current through each V_{CC}, V_{DDQ}, or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3)	36°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 3.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		V_{DDQ}		2.7	V
V_{DDQ}	Output supply voltage		2.3		2.7	V
V_{REF}	Reference voltage ($V_{REF} = V_{DDQ}/2$)		1.15	1.25	1.35	V
V_{TT}	Termination voltage		V_{REF}–40mV	V_{REF}	V_{REF}+40mV	V
V_I	Input voltage		0		V_{CC}	V
V_{IH}	AC high-level input voltage	Data inputs	V_{REF}+310mV			V
V_{IL}	AC low-level input voltage	Data inputs			V_{REF}–310mV	V
V_{IH}	DC high-level input voltage	Data inputs	V_{REF}+150mV			V
V_{IL}	DC low-level input voltage	Data inputs			V_{REF}–150mV	V
V_{IH}	High-level input voltage	$\overline{\text{RESET}}$	1.7			V
V_{IL}	Low-level input voltage	$\overline{\text{RESET}}$			0.7	V
V_{ICR}	Common-mode input voltage range	CLK, $\overline{\text{CLK}}$	0.97		1.53	V
$V_{I(PP)}$	Peak-to-peak input voltage	CLK, $\overline{\text{CLK}}$	360			mV
I_{OH}	High-level output current				–20	mA
I_{OL}	Low-level output current				20	
T_A	Operating free-air temperature		0		70	°C

NOTE 4: The $\overline{\text{RESET}}$ input of the device must be held at valid logic voltage levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless $\overline{\text{RESET}}$ is low. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP[†]	MAX	UNIT
V_{IK}		$I_I = –18$ mA		2.3 V			–1.2	V
V_{OH}		$I_{OH} = –100$ µA		2.3 V to 2.7 V	V_{DDQ}–0.2			V
		$I_{OH} = –16$ mA		2.3 V	1.95			
V_{OL}		$I_{OL} = 100$ µA		2.3 V to 2.7 V			0.2	V
		$I_{OL} = 16$ mA		2.3 V			0.35	
I_I	All inputs	$V_I = V_{CC}$ or GND		2.7 V			±5	µA
I_{CC}	Static standby	$\overline{\text{RESET}}$ = GND	$I_O = 0$	2.7 V			10	µA
	Static operating	$\overline{\text{RESET}} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$					35	mA
I_{CCD}	Dynamic operating – clock only	$\overline{\text{RESET}} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{\text{CLK}}$ switching 50% duty cycle	$I_O = 0$	2.7 V		46		µA/ MHz
	Dynamic operating – per each data input	$\overline{\text{RESET}} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{\text{CLK}}$ switching 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle				12		µA/ clock MHz/ D input
r_{OH}	Output high	$I_{OH} = –20$ mA		2.3 V to 2.7 V	7		20	Ω
r_{OL}	Output low	$I_{OL} = 20$ mA		2.3 V to 2.7 V	7		20	Ω
C_i	Data inputs	$V_I = V_{REF} \pm 310$ mV		2.5 V	3	3.75	4.25	pF
	CLK, $\overline{\text{CLK}}$	$V_{ICR} = 1.25$ V, $V_{I(PP)} = 360$mV			3	3.5	4	
	$\overline{\text{RESET}}$	$V_I = V_{CC}$ or GND			3.5	4.35	5	

[†] All typical values are at $V_{CC} = 2.5$ V, $T_A = 25°C$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				V_{CC} = 2.5 V ± 0.2 V		UNIT
				MIN	MAX	
f_{clock}	Clock frequency				200	MHz
t_w	Pulse duration, CLK, $\overline{\text{CLK}}$ high or low			2.5		ns
t_{act}	Differential inputs active time (see Note 5)				22	ns
t_{inact}	Differential inputs inactive time (see Note 6)				22	ns
t_{su}	Setup time	Fast slew rate (see Notes 7 and 9)	Data before CLK↑, $\overline{\text{CLK}}$↓	0.75		ns
		Slow slew rate (see Notes 8 and 9)		0.9		
t_h	Hold time	Fast slew rate (see Notes 7 and 9)	Data after CLK↑, $\overline{\text{CLK}}$↓	0.75		ns
		Slow slew rate (see Notes 8 and 9)		0.9		

NOTES: 5. V_{REF} must be held at a valid input level, and data inputs must be held low for a minimum time of t_{act} max, after $\overline{\text{RESET}}$ is taken high.

6. V_{REF}, data, and clock inputs must be held at valid voltage levels (not floating) for a minimum time of t_{inact} max, after $\overline{\text{RESET}}$ is taken low.

7. Data signal input slew rate ≥1 V/ns

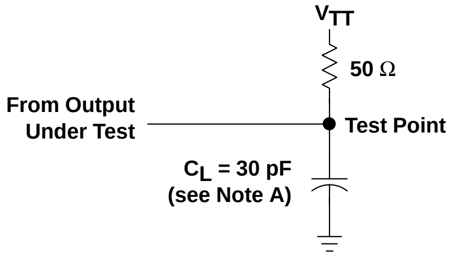
8. Data signal input slew rate ≥0.5 V/ns and <1 V/ns

9. CLK, $\overline{\text{CLK}}$ input slew rates are ≥1 V/ns.

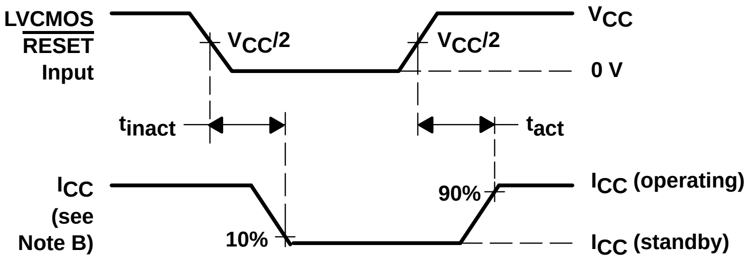
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		UNIT
			MIN	MAX	
f_{max}			200		MHz
t_{pd}	CLK and $\overline{\text{CLK}}$	Q	1.1	3.1	ns
t_{PHL}	$\overline{\text{RESET}}$	Q		5	ns

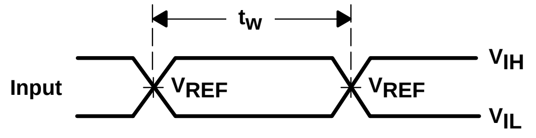
PARAMETER MEASUREMENT INFORMATION



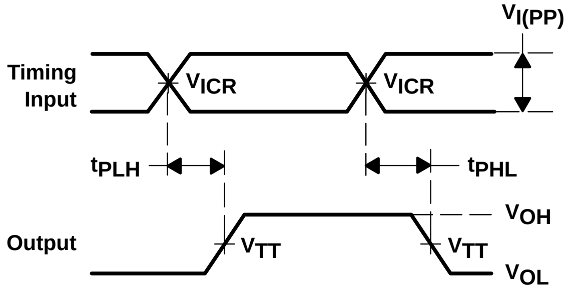
LOAD CIRCUIT



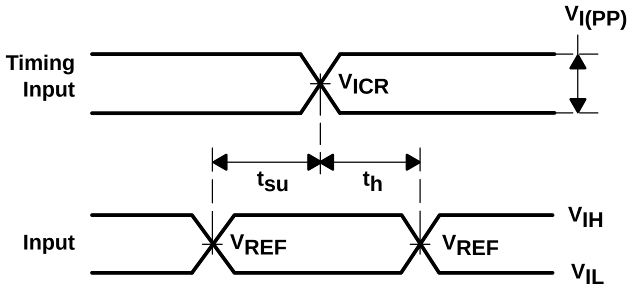
VOLTAGE AND CURRENT WAVEFORMS
INPUTS ACTIVE AND INACTIVE TIMES



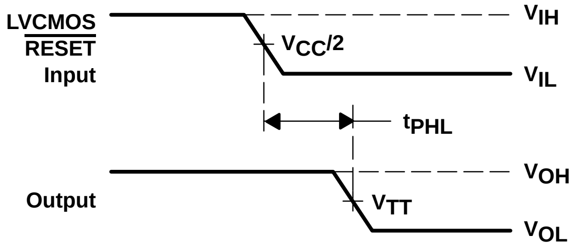
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. I_{CC} tested with clock and data inputs held at V_{CC} or GND, and I_O = 0 mA.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise noted).
- D. The outputs are measured one at a time with one transition per measurement.
- E. $V_{TT} = V_{REF} = V_{DDQ}/2$
- F. $V_{IH} = V_{REF}$ + 310 mV (ac voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVCMOS input.
- G. $V_{IL} = V_{REF}$ – 310 mV (ac voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
- H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74SSTV32852GKFR	ACTIVE	BGA MI CROSTA R	GKF	114	1000	TBD	SNPB	Level-3-220C-168 HR
SN74SSTV32852ZKFR	ACTIVE	LFBGA	ZKF	114	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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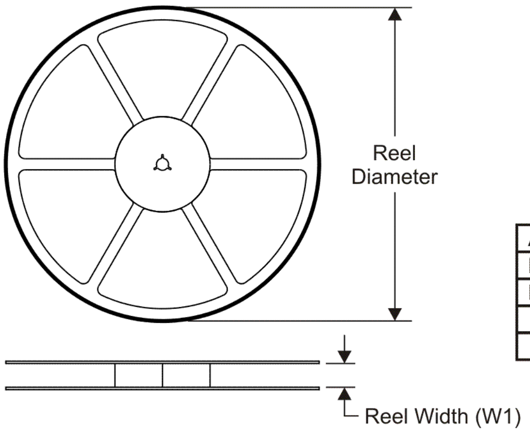
OTHER QUALIFIED VERSIONS OF SN74SSTV32852 :
- Enhanced Product: SN74SSTV32852-EP

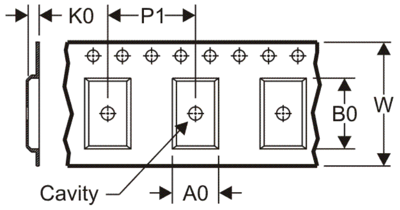
NOTE: Qualified Version Definitions:
  - Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

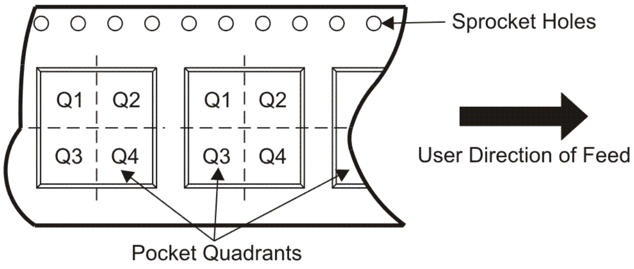


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

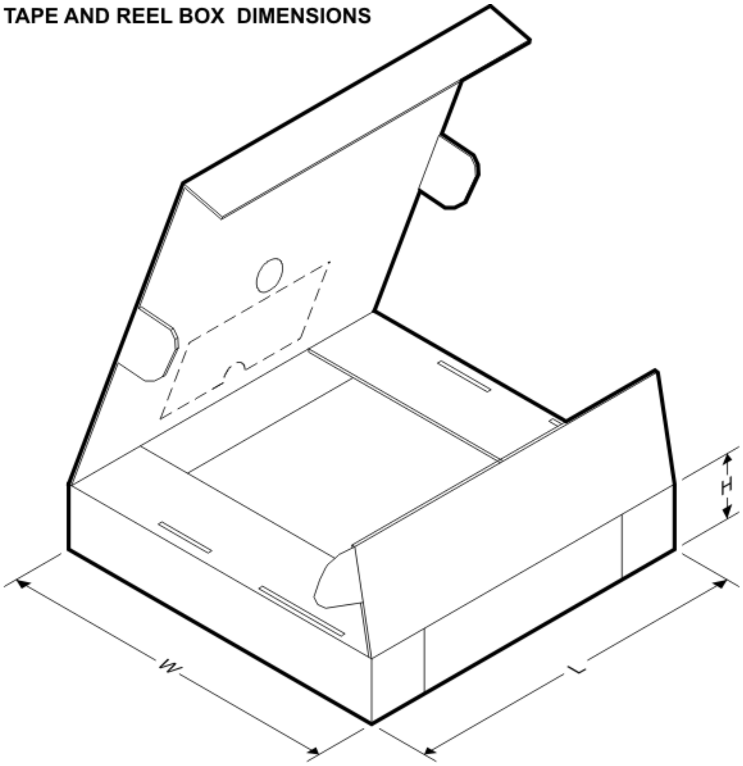
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74SSTV32852GKFR	BGA MICROSTAR	GKF	114	1000	330.0	24.4	5.8	16.3	1.8	8.0	24.0	Q1
SN74SSTV32852ZKFR	LFBGA	ZKF	114	1000	330.0	24.4	5.8	16.3	1.8	8.0	24.0	Q1

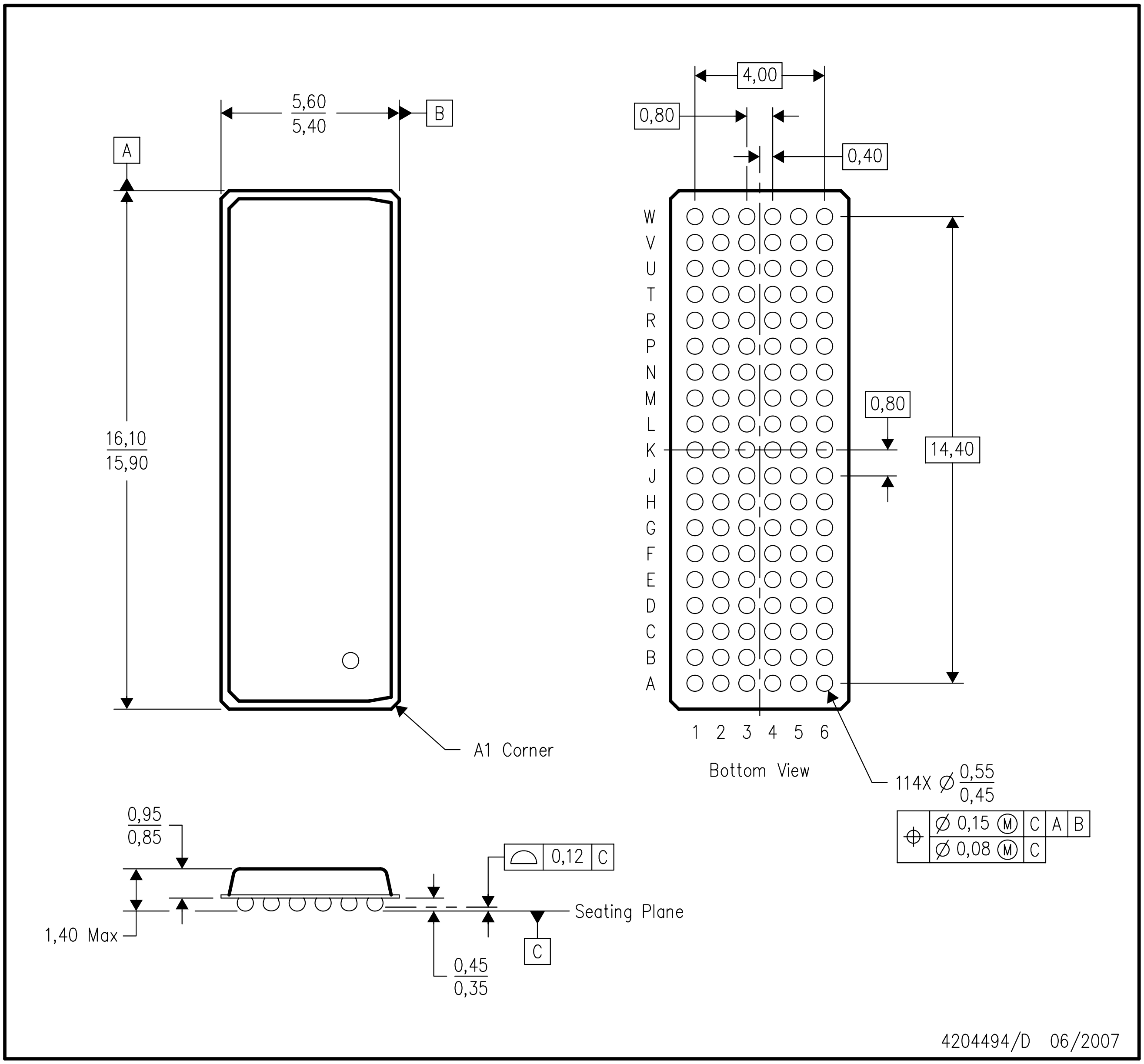
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

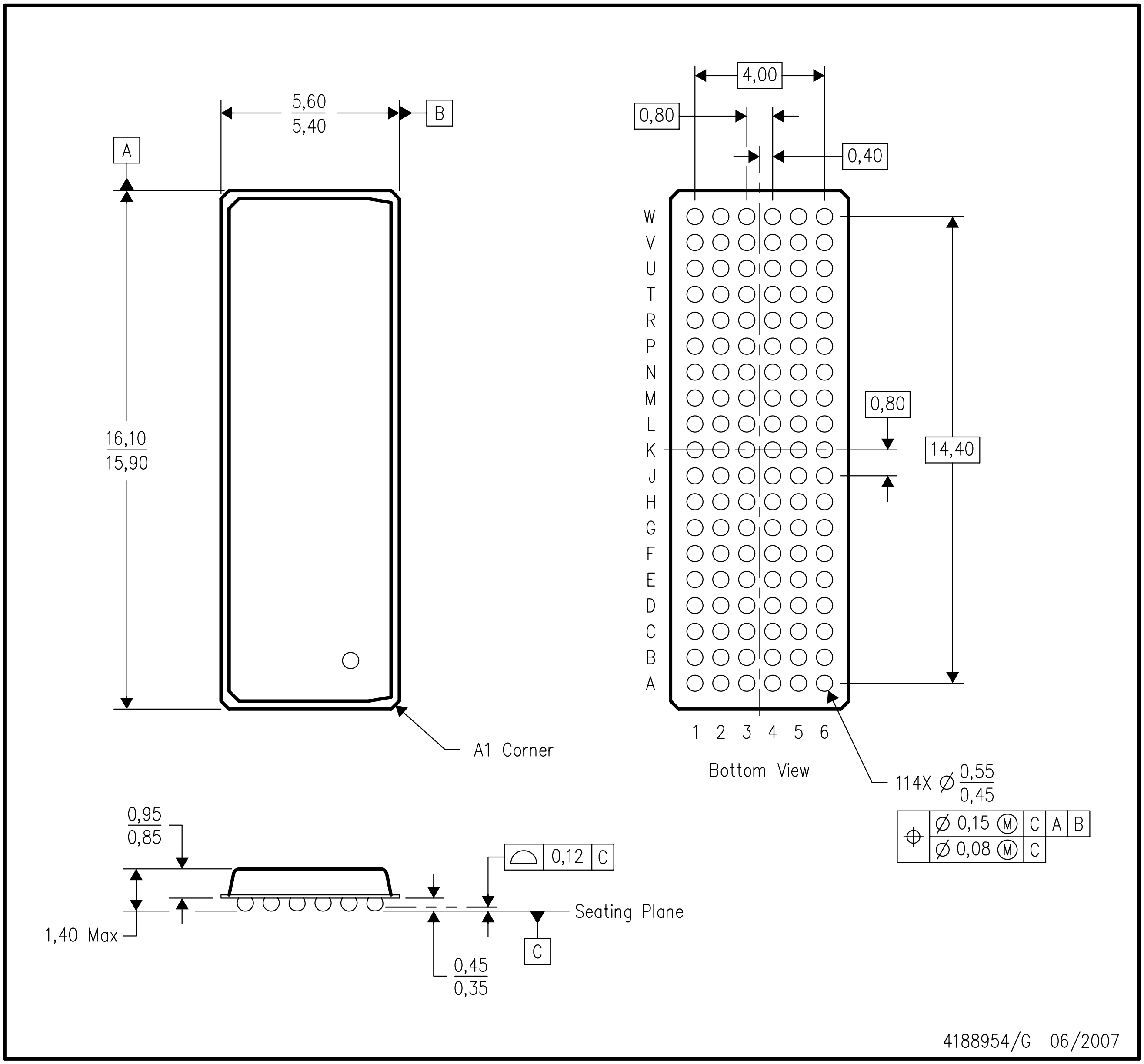
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74SSTV32852GKFR	BGA MICROSTAR	GKF	114	1000	346.0	346.0	41.0
SN74SSTV32852ZKFR	LFBGA	ZKF	114	1000	346.0	346.0	41.0

ZKF (R–PBGA–N114) PLASTIC BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO–205 variation DC.
- D. This package is lead–free. Refer to the 114 GKF package (drawing 4188954) for tin–lead (SnPb).

GKF (R–PBGA–N114) PLASTIC BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO–205 variation DC.
- D. This package is tin–lead (SnPb). Refer to the 114 ZKF package (drawing 4204494) for lead–free.

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