KODENSHI AUK

SN7500x/P

Pulse Width Modulation

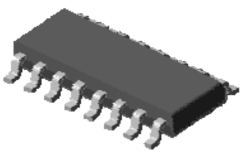
◈ Description

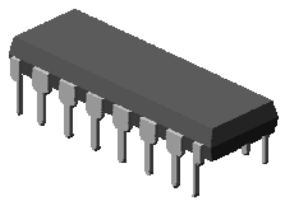
The SN7500 is a monolithic integrated circuit which includes all the necessary building blocks for the design of pulse width modulate(PWM) switching power supplies, including push-pull, bridge and series configuration. The precision of voltage reference is improved up to ±1%/±2% through trimming and this provides a better output voltage regulation. The device can operate at switching frequencies between 1KHz and 300KHz and output voltage up to 36V.
The SN7500 is specified over an operating temperature range of -40℃~+85℃.

◈ Features

- Internal Regulator Provides a Stable 5V Reference Supply Trimmed to ±1% or ±2% Accuracy
- Uncommitted output transistors capable of 200mA source or sink
- Internal protection from double pulsing of out-puts with narrow pulse widths or with supply voltages below specified limits
- Easily synchronized to other circuits
- Dead time control comparator
- Output control selects single-ended or push-pull operation
- Operating temperature range : -40℃ ~ +85℃
- Halogen-Free Package is Available
- High Level ESD Protection : 400V(MM), 4KV(HBM)

◈ Package Type


SOP-16


DIP-16

◈ Application

- Charger
- SMPS
- Back Light Inverter

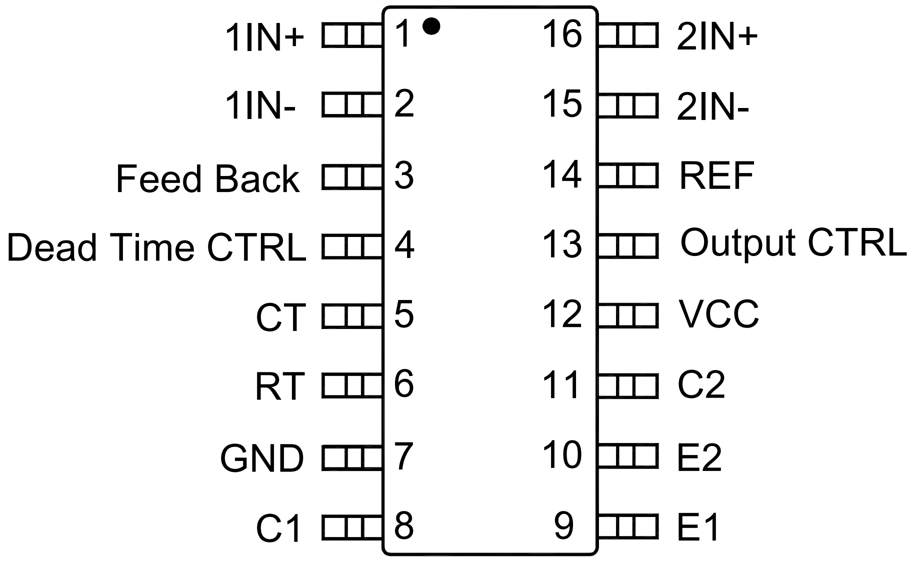
◈ Ordering Information

Device Name	PKG Type	Marking
SN7500x	SOP-16	SN7500---(1) YWW---(2)
SN7500xP	DIP-16	SN7500---(1) YWW---(2)

(a) Rank X : B = Vref 2% / C = Vref 1%

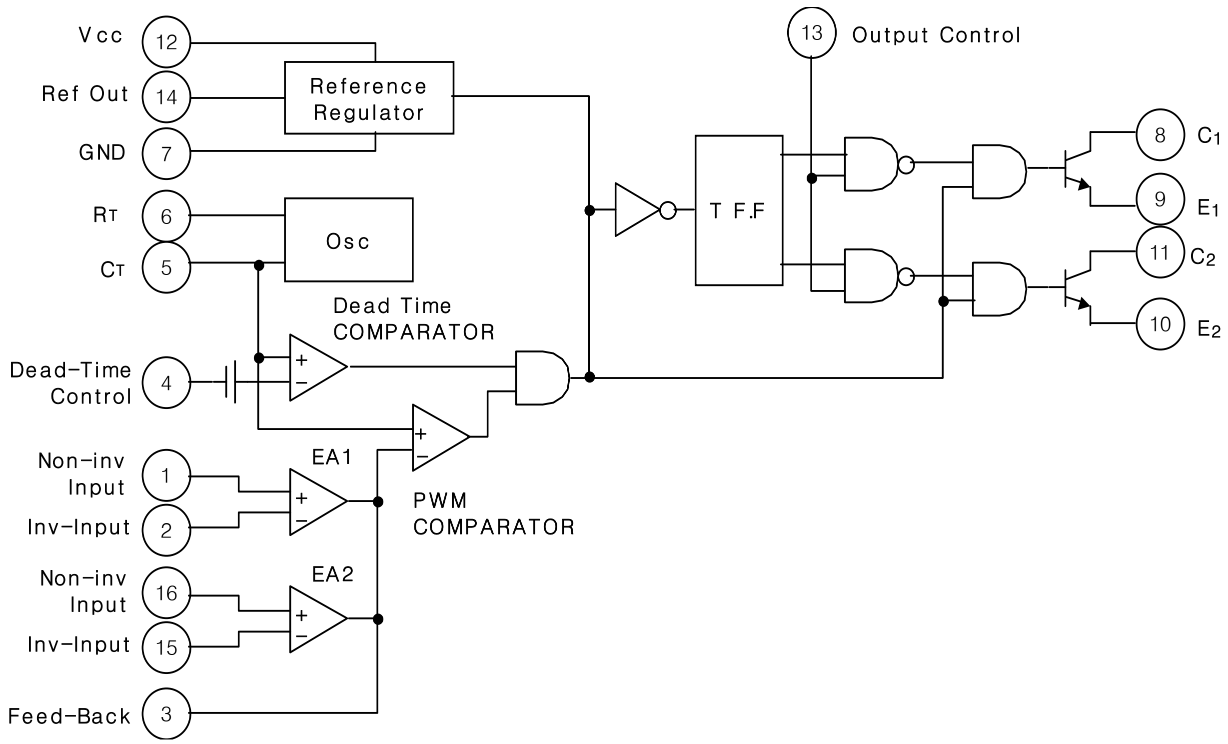
(b) Marking Information : (1) Device Code, (2) Year & Week Code

◈ Pin Configuration (Top View)



1. Non-INV Input
2. INV Input
3. Feed-Back
4. Dead-Time Control
5. CT
6. RT
7. GND
8. C1
9. E1
10. E2
11. C2
12. Vcc
13 Output Control
14. Ref Out
15. INV-Input
16. Non-INV Input

◈ Block Diagram



◈Absolute Maximum Ratings

Ta=25°C

Characteristic		Symbol	Ratings	Unit
Supply Voltage		V_{CC}	40	V
Collector Supply Voltage		V_C	40	V
Output Current		Io	250	mA
Amplifier Input Voltage		Vin	Vcc+0.3	V
Power Dissipation	SOP-16	P_D	1500	mW
	DIP-16	P_D	1700	mW
Operating Temperature		T_{opr}	-40 ~ +85	°C
Storage Temperature		T_{stg}	-55 ~ +150	°C

◈Recommended Operating Condition

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	7	15	36	V
Collector Output Voltage	V_{C1}, V_{C2}	-	30	36	V
Collector Output Current	I_{C1}, I_{C2}	-	-	200	mA
Amplifier Input Voltage	Vin	-0.3	-	Vcc-2.0	V
Current Into Feedback Terminal	I_{FB}	-	-	0.3	mA
Reference Output Current	I_{REF}	-	-	10	mA
Timing Resistor	R_T	1.8	30	500	kΩ
Timing Capacitor	C_T	0.0047	0.001	10	uF
Oscillator Frequency	f_{OSC}	1	40	300	KHz
PWM Input Voltage (Pin 3, 4, 13)	-	0.3	-	5.3	V

Reference Section

Characteristic	Symbol	Test Condition		Min.	Typ.	Max.	Unit
Output Reference Voltage	Vref	Iref = 1.0mA, Ta=25℃	SN7500B	4.90	5.00	5.10	V
		Iref = 1.0mA, Ta=-25~85℃		4.80	5.00	5.20	
		Iref = 1.0mA, Ta=25℃	*SN7500C	4.95	5.00	5.05	
		Iref = 1.0mA, Ta=-25~85℃		4.90	5.00	5.10	
Line Regulation	V_{LINE}	7V < Vcc < 20V		-	2	25	mV
Load Regulation	V_{LOAD}	1mA< I_{REF} <10mA		-	1	15	mV
Short Circuit Current	Isc	Vref=0V		10	35	50	mA

[* : Under Development] SN7500B(Tol. 2%), SN7500C(Tol. 1%)

Oscillator Section

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Oscillation Frequency	f_{OSC}	C_t=0.001 ㎌, R_t=30 ㏀	-	40	-	KHz
		C_t=0.01 ㎌, R_t=12 ㏀, Ta=25℃	9.2	10	10.8	
		C_t=0.01 ㎌, R_t=12 ㏀, Ta=25~85℃	9	-	12	
Oscillation Frequency Change With Temperature	$\Delta f_{SOC}/\triangle T$	C_t=0.01 ㎌, R_t=12 ㏀, Ta=25~85℃	-	-	2	%

Dead Time Control Section

Characteristic		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Bias Current (Pin4)		$I_{IB(DT)}$	Vcc = 15V, 0V < V_4 < 5.25V	-	-2	-10	uA
Max. Duty cycle		$D_{(Max)}$	Vcc = 15V, Pin4 = 0V, Output Control Pin = Vref	45	-	-	%
Input Threshold Voltage	Zero Duty	V_{TH}	-	-	2.8	3.3	V
	Max Duty			0	-	-	

Error Amplifier Section

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Offset Voltage	V_{IOS}	V_3 = 2.5V	-	2	10	mV
Input Offset Current	I_{IOS}	V_3 = 2.5V	-	25	250	nA
Input Bias Current	I_{IB}	V_3 = 2.5V	-	0.2	1	uA
Common Mode Input voltage Range	V_{ICR}	7V ≤ V_{CC} ≤ 20V	-0.3	-	V_{CC}-2	V
Large Signal Open Loop Voltage Range	G_{VO}	0.5V ≤ V_3 ≤ 3.5V	60	74	-	dB
Unity Gain Band width	GBW	-	-	650	-	KHz
Open Loop Voltage Gain	GVO	0.5V ≤ Vo ≤ 3.5V	70	95	-	dB
Output Sink Current	Isink	-15mV ≤ Vid ≤ -5V , V_3=0.7V	-0.3	-0.7	-	mA
Common Mode Rejection Ratio	CMRR	-	65	80	-	dB
Output Source Current	Isource	15mV ≤ Vid ≤ 5V , V_3=3.5V	2	-	-	mA

PWM Comparator Section (Pin3)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Threshold Voltage	V_{ITH}	Zero duty cycle	-	4	4.5	V
Input Sink Current	Io^-	V_3=0.7V	-0.3	-0.7	-	mA

Output Section

Characteristic		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Saturation Voltage	Common-Emitter	$V_{CE(SAT)}$	V_E= 0V, I_C = 200mA	-	1.1	1.3	V
	Emitter-Follower		V_{CC} =15V, I_E = -200mA	-	1.5	2.5	
Collector off-state Current		$I_{C(off)}$	V_{CC} = V_{CE} = 20V, V_E = 0	-	2	100	uA
Emitter off-state Current		$I_{E(off)}$	V_{CC} = V_C = 20V, V_E = 0	-	-	-100	
Total Device							
Standby power Supply Current		I_{CC}	Pin6=Vref, Vcc=15V	-	3.5	10	mA

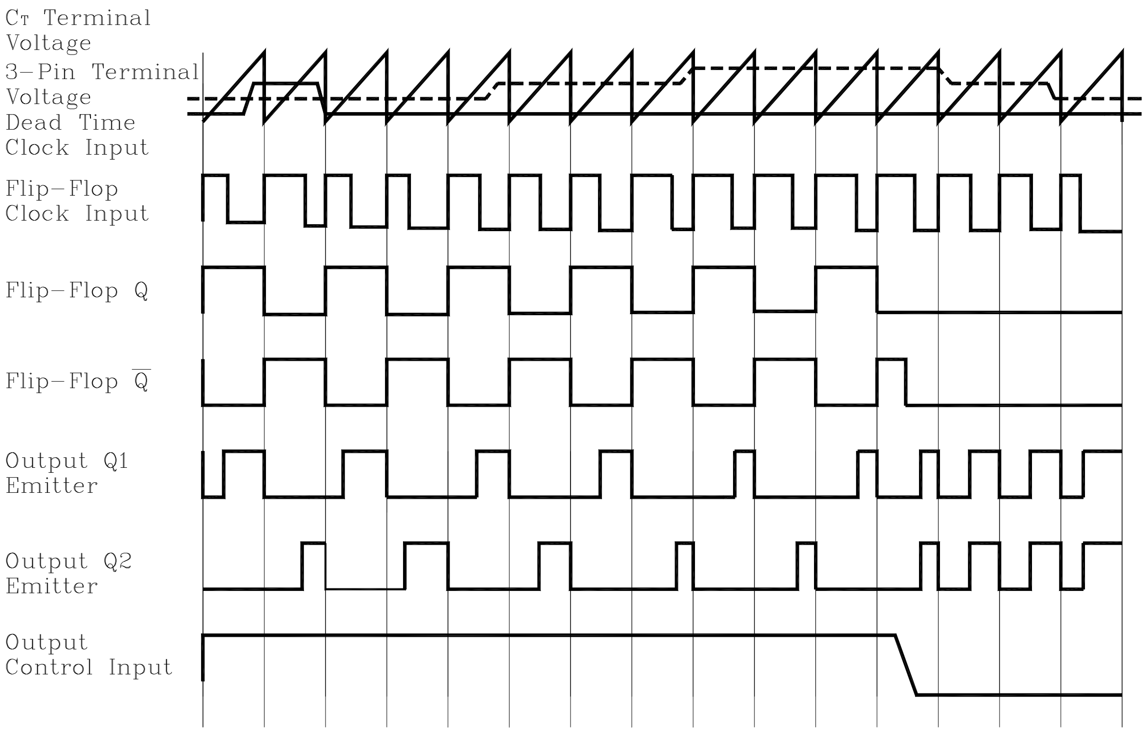
Output Switching Characteristic

Characteristic		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Rise Time	Common Emitter	t_r	-	-	100	200	ns
	Emitter Follower			-	100	200	
Fall Time	Common Emitter	t_f	-	-	25	100	
	Emitter Follower			-	25	100	

INFORMATION

The basic oscillator(switching)frequency is controlled by an external resistor (R_T) and capacitor(C_T). The relationship between the values of R_T,C_T and frequency is shown in.
The level of the sawtooth wave form is compared with an error voltage by the pulse width modulated comparator. The output of the PWM Comparator directs the pulse steering flip flop and the output control logic.
The error voltage is generated by the error amplifier. The error amplifier boosts the voltage difference between the output and the 5V internal reference. See Figure7 for error amp sensing techniques. The second error amp is typically used to implement current limiting. The output control logic (Pin13) selects either push-pull or single-ended operation of the output transistors (see Figure6). The dead time control prevents on-state overlap of the output transistors as can be seen is Figure5. The dead time is approximately 3 to 5% of the total period if the dead time control(pin4) is grounded. This dead time can be increased by connecting the dead time control to a voltage up to 5 V. The frequency response of the error amps can be modified by using external resistors and capacitors. These components are typically connected between the compensation terminal (pin3) and the inverting input of the error amps(pin2 or pin15). The switching frequency of two or more SJ7500 circuits can be synchronized. The timing capacitor, Ct is connected as shown in Figure8. Charging current is provided by the master circuit. Discharging is through all the circuits slaved to the master. Rt is required only for the master circuit.

Operating Waveform



Test Circuit

Fig.1 Error Amplifier Test Circuit

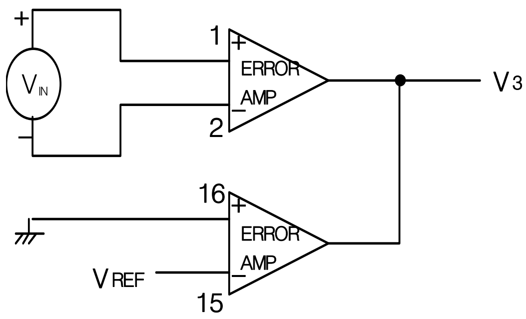


Fig.2 Current Limit sense Amplifier Test Circuit

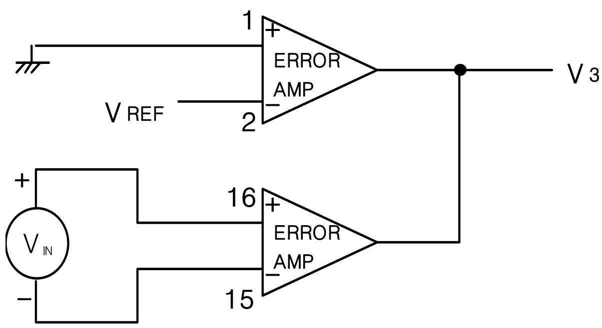


Fig. 3 Common-Emitter Configuration Test circuit and Waveform

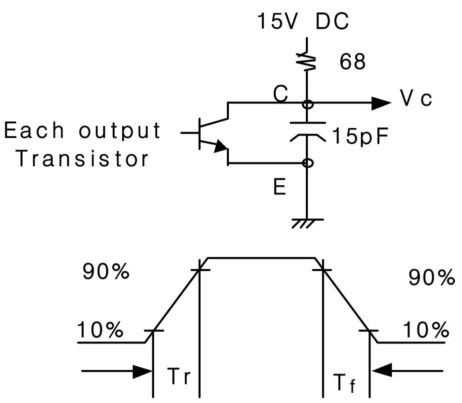


Fig. 5 Dead-Time and Feedback Control Test Circuit

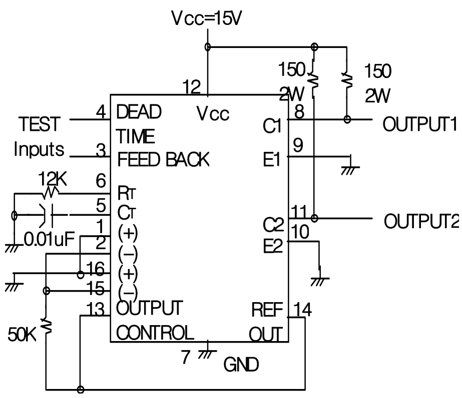
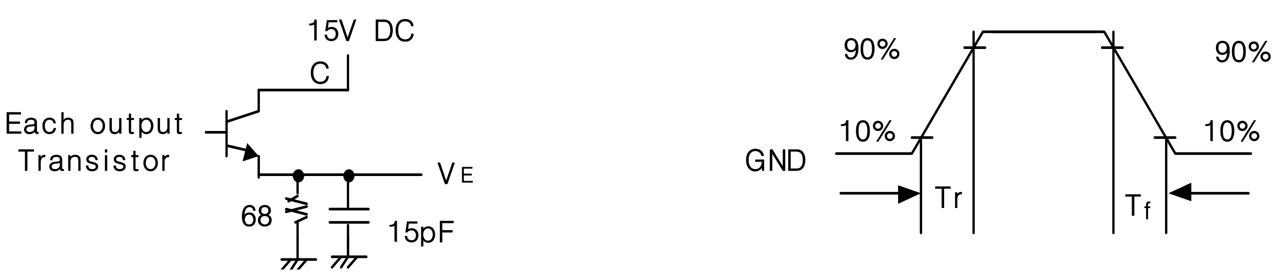


Fig. 4 Emitter-Follower Configuration Test circuit and waveform Voltage waveform



APPLICATION CIRCUIT

Fig. 6 Output Connections for Single-Ended and Push-Pull Configurations

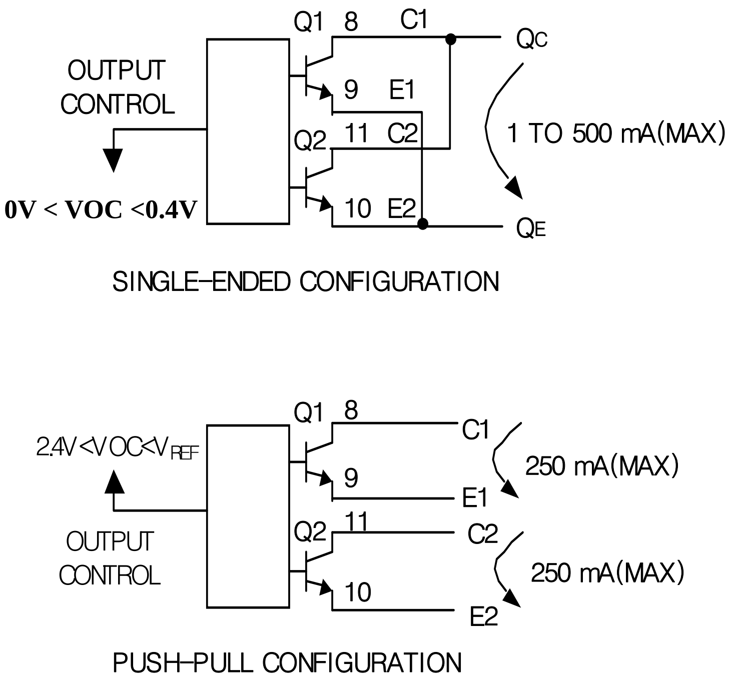


Fig. 7 Error Amplifier Sensing Techniques

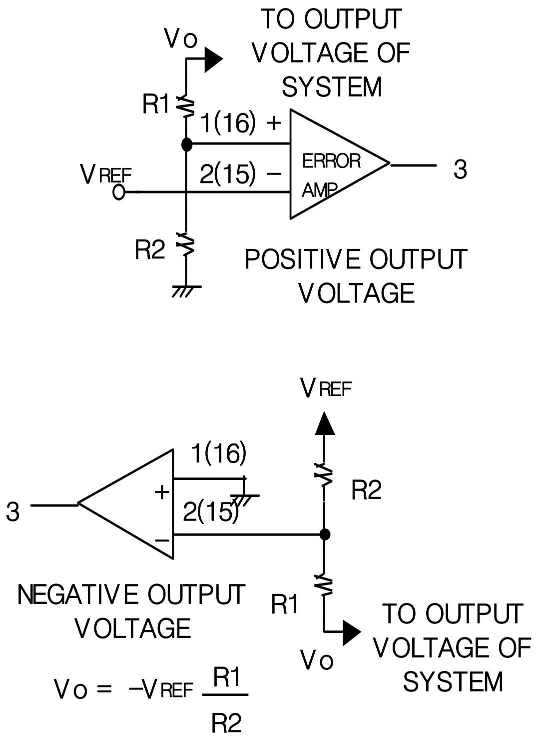


Fig. 8 Slaving Tow or More Control Circuits

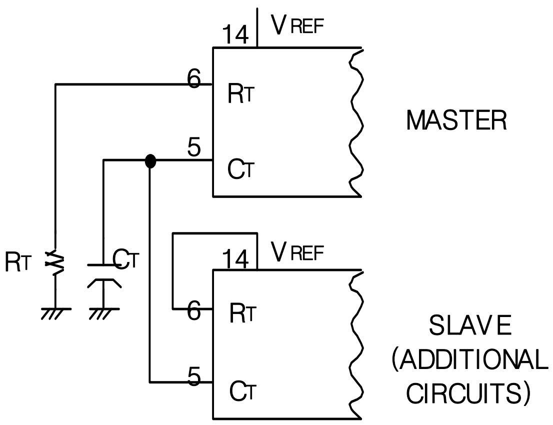
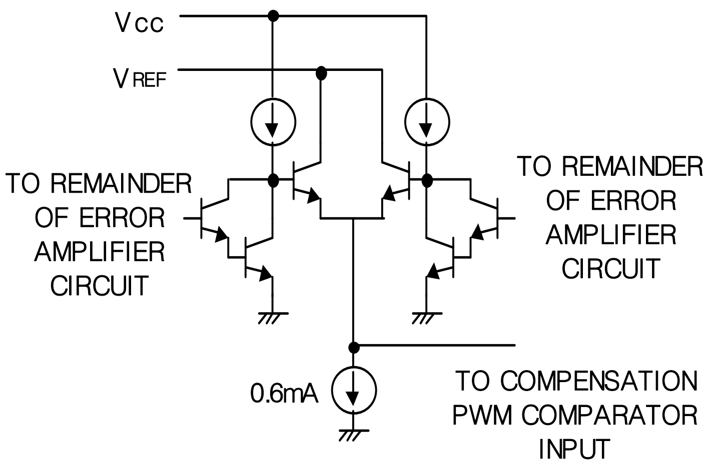


Fig. 9Error Amplifier and Current Limit Sense Amplifier Output Circuits



◈ Electrical Characteristic Curves

Fig.10 Oscillator Frequency vs Timing Resistance

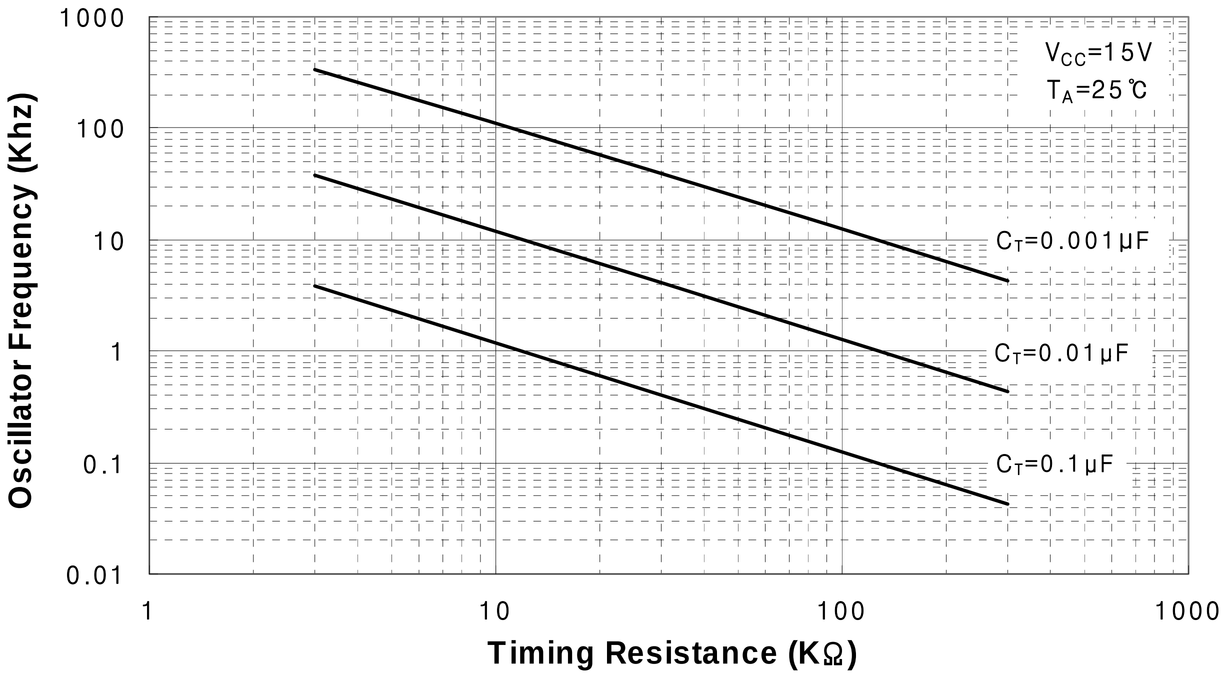
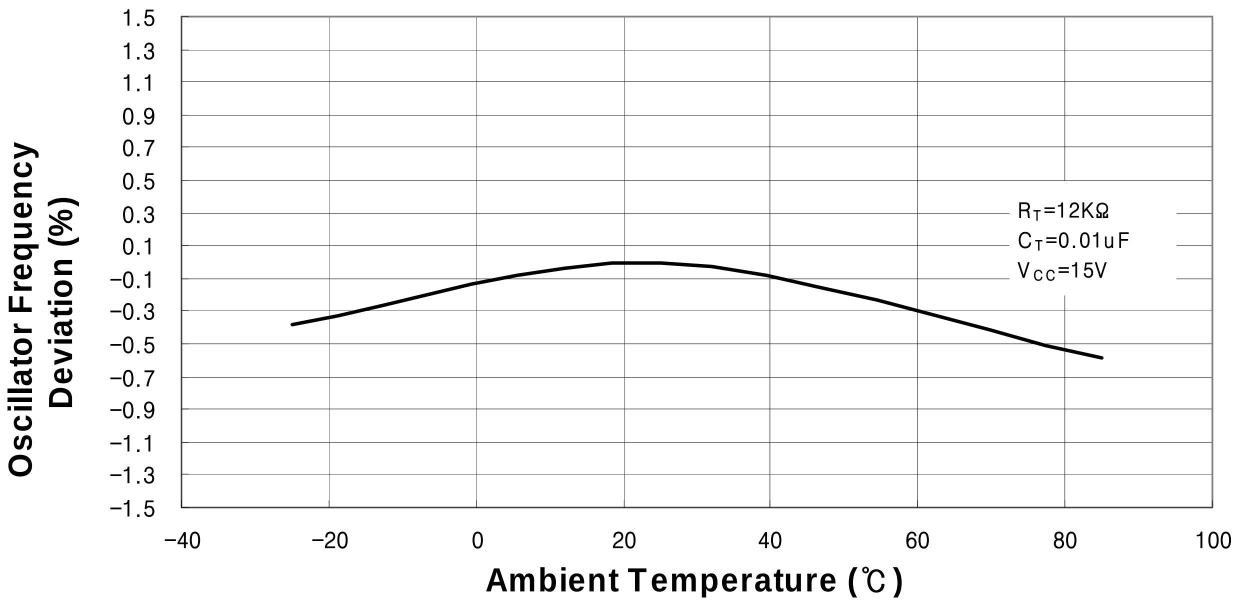
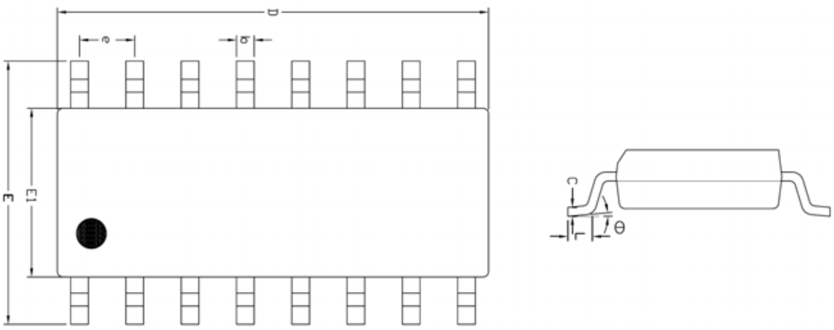


Fig.11 Frequency Deviation vs Ambient Temperature

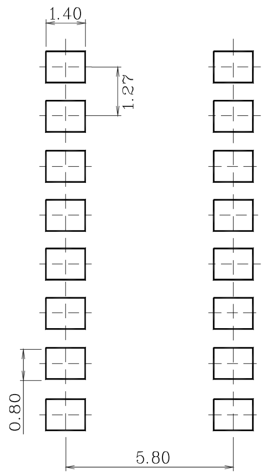


◈ SOP-16 Outline Dimension (unit : mm)

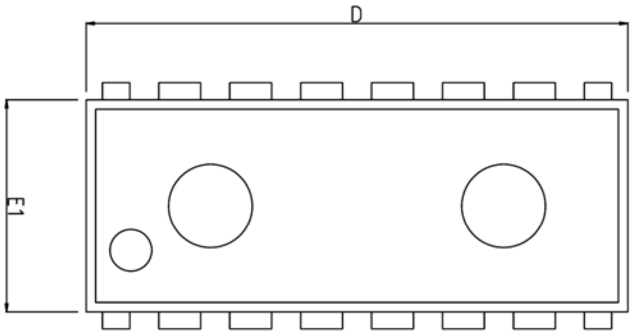


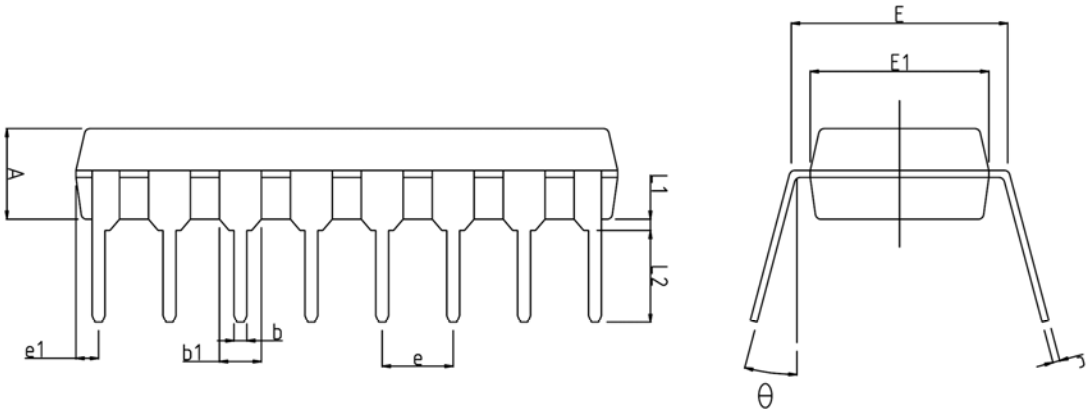
SYMBOL	MILLIMETER(mm)			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	1.245	–	1.445	
A1	0.125	0.175	0.275	
b	0.320	0.420	0.520	
c	0.170	0.220	0.270	
D	9.806	9.906	10.006	
E	5.870	6.020	6.170	
E1	3.761	3.861	3.961	
e	1.270 BSC			
L	0.462	0.562	0.662	
θ	0 °	–	8 °	

※ Recommend PCB solder land [Unit: mm]



◈ DIP-16 Outline Dimension (unit : mm)





SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	3.05	3.25	3.45	
b	0.36	0.46	0.56	
b1	1.40	1.50	1.60	
c	0.20	0.25	0.35	
D	19.20	19.40	19.60	
E	7.37	7.62	7.87	
E1	6.20	6.40	6.60	
e	2.54 TYP			
e1	0.81 TYP			
L1	0.51	–	–	
L2	3.00	3.30	3.60	
θ	0°	–	15°	