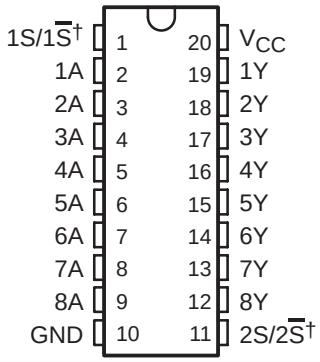
SLLS076B − JANUARY 1977 − REVISED MAY 1995

- **Meets or Exceeds the Requirements of IBM™ System 360/370 Input/Output Specification**
- **Input Resistance . . . 7 kΩ to 20 kΩ**
- **Output Compatible With TTL**
- **Schottky-Clamped Transistors**
- **Operates From a Single 5-V Supply**
- **High Speed . . . Low Propagation Delay**
- **Ratio Specification . . . t_{PLH} /t_{PHL}**
- **Common Strobe for Each Group of Four Receivers**
- **SN75128 . . . Active-High Strobes**
  SN75129 . . . Active-Low Strobes

N PACKAGE
(TOP VIEW)



† S and S̄ for SN75128 and SN75129, respectively

description

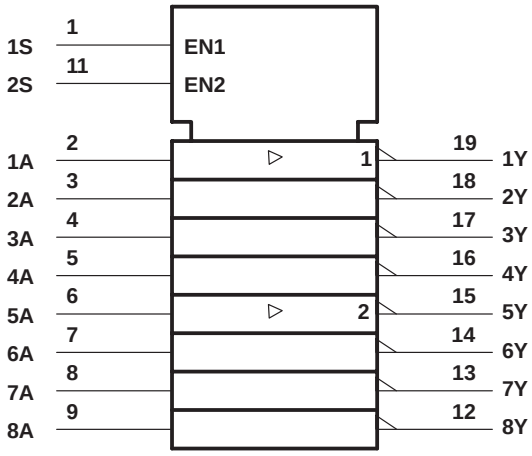
The SN75128 and SN75129 are eight-channel line receivers designed to satisfy the requirements of the input-output interface specification for IBM 360/370. Both devices feature common strobes for each group of four devices. The SN75128 has active-high strobes; the SN75129 has active-low strobes. Special low-power design and Schottky-diode-clamped transistors allow low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs.

For new IBM 360/370 interface designs, see the SN751730.

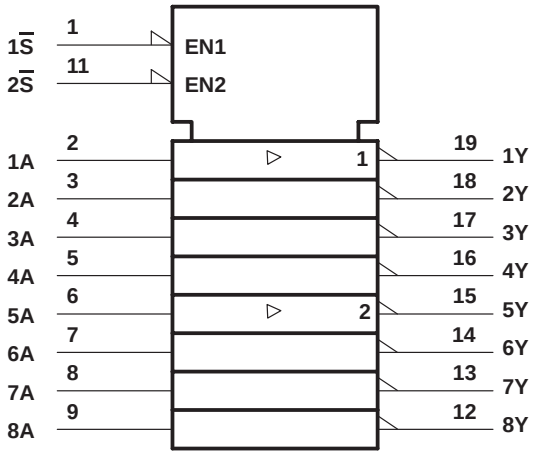
The SN75128 and SN75129 are characterized for operation from 0°C to 70°C.

logic symbols†

SN75128



SN75129



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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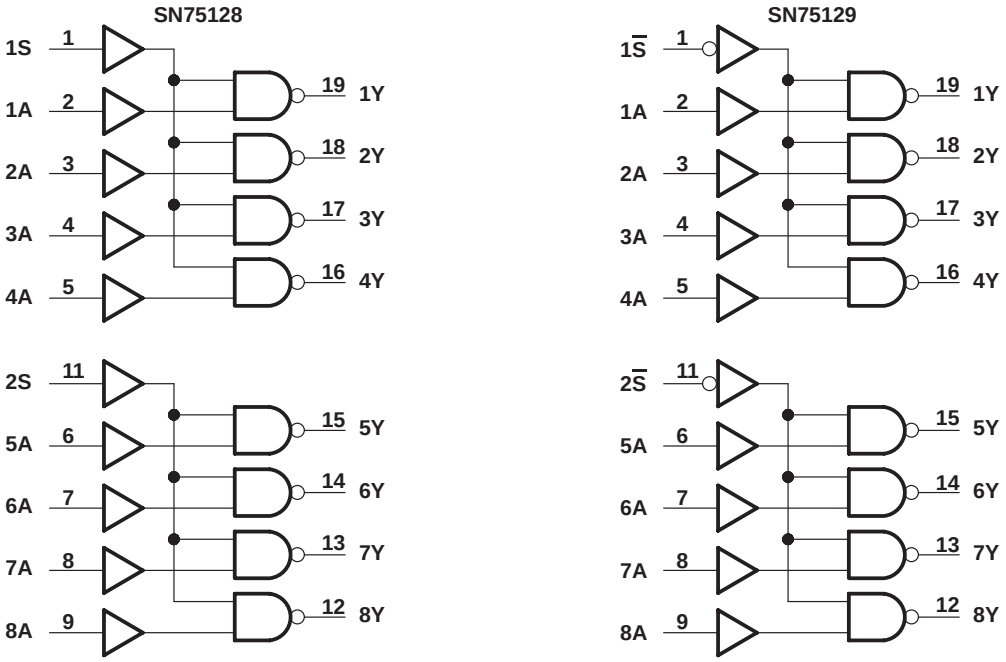
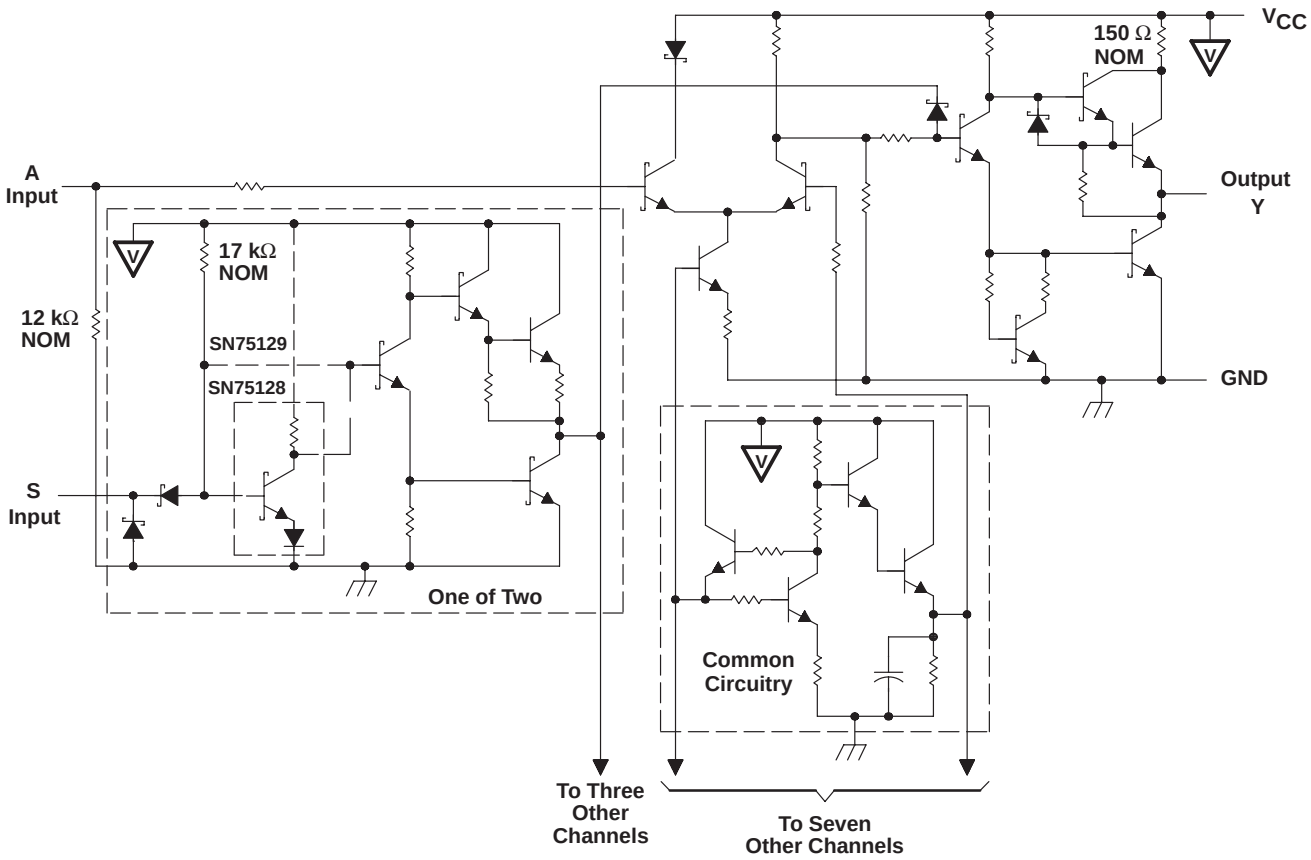
logic diagrams (positive logic)



schematic (each driver)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage range, V_I (A) . . . . . −0.15 V to 7 V
Input voltage, V_I (S) . . . . . 7 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}	A	1.7			V
	S	2			
Low-level input voltage, V_{IL}	A			0.7	V
	S			0.7	
High-level output current, I_{OH}				−0.4	mA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

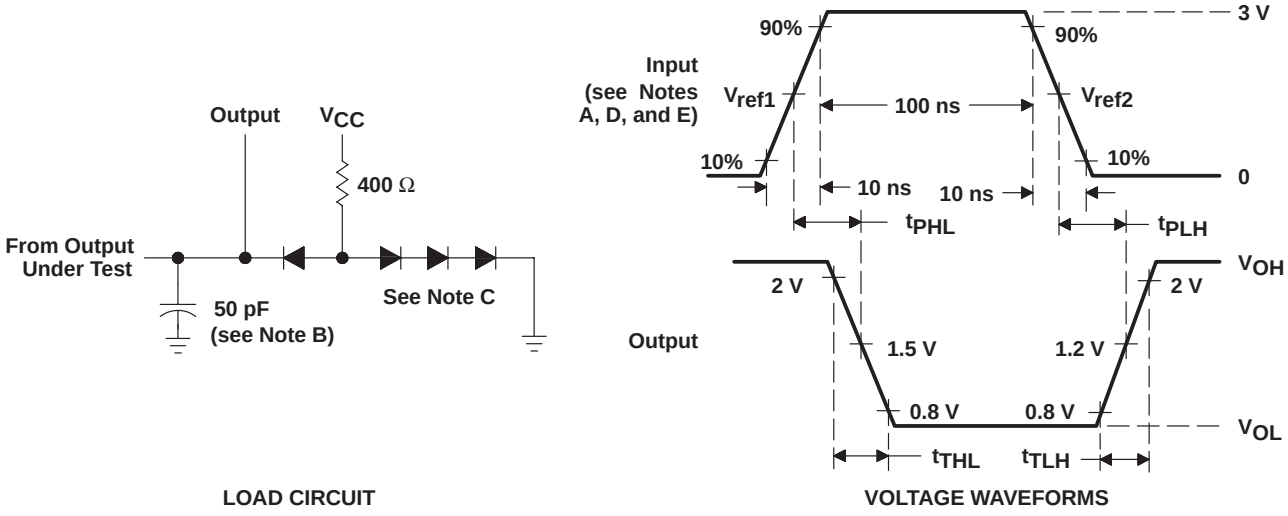
PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 4.5 V,	V_{IL} = 0.7 V,	I_{OH} = −0.4 mA	2.4	3.1		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V,	V_{IH} = 1.7 V,	I_{OL} = 16 mA		0.4	0.5	V
V_{IK}	Input clamp voltage	S	V_{CC} = 4.5 V,	I_I = −18 mA				−1.5	V
I_{IH}	High-level input current	A	V_{CC} = 5.5 V,	V_I = 3.11 V			0.3	0.42	mA
		S	V_{CC} = 5.5 V,	V_I = 2.7 V				20	µA
I_{IL}	Low-level input current	A	V_{CC} = 5.5 V,	V_I = 0.15 V				30	µA
		S	V_{CC} = 5.5 V,	V_I = 0.4 V				−0.4	mA
I_{OS}	Short-circuit output current‡		V_{CC} = 5.5 V,	V_O = 0		−18		−60	mA
r_I	Input resistance		V_{CC} = 4.5 V,	0 V or open,	ΔV_I = 0.15 V to 4.15 V	7		20	kΩ
I_{CC}	Supply current	SN75128	V_{CC} = 5.5 V,	Strobe at 2.4 V,	All A inputs at 0.7 V		19	31	mA
		SN75129	V_{CC} = 5.5 V,	Strobe at 0.4 V,	All A inputs at 0.7 V		19	31	
		SN75128	V_{CC} = 5.5 V,	Strobe at 2.4 V,	All A inputs at 4 V		32	53	
		SN75129	V_{CC} = 5.5 V,	Strobe at 0.4 V,	All A inputs at 4 V		32	53	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM	TEST CONDITIONS	SN75128			SN75129			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	A	R_L = 400 Ω, C_L = 50 pF, See Figure 1	7	14	25	7	14	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	18	30	10	18	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output	S			26	40		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output				22	35		16	30	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of propagation delay times	A		0.5	0.8	1.3	0.5	0.8	1.3	
t_{TLH}	Transition time, low-to-high-level output			1	7	12	1	7	12	ns
t_{THL}	Transition time, high-to-low-level output			1	3	12	1	3	12	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Input pulses are supplied by a generator having the following characteristics: Z_O = 50 Ω, PRR ≤ 5 MHz.
B. Includes probe and jig capacitance
C. All diodes are 1N3064 or equivalent.
D. The strobe inputs of SN75129 are in phase with the output.
E. V_{ref1} = 0.7 V and V_{ref2} = 1.7 V for testing data (A) inputs, V_{ref1} = V_{ref2} = 1.3 V for strobe inputs.

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

VOLTAGE TRANSFER CHARACTERISTICS

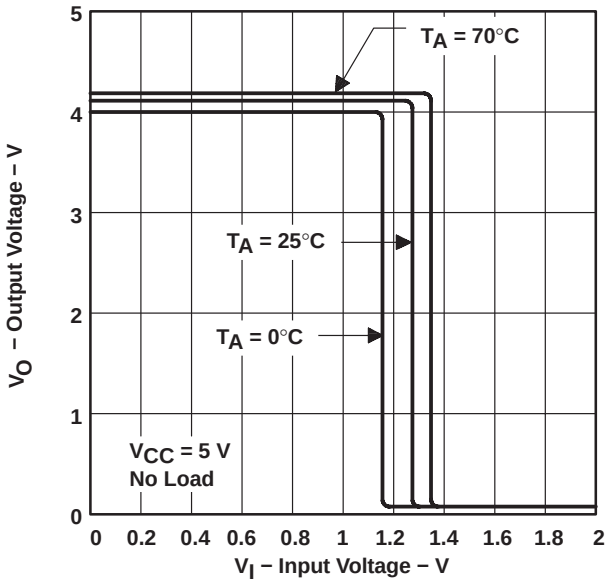


Figure 2

VOLTAGE TRANSFER CHARACTERISTICS FROM A INPUTS

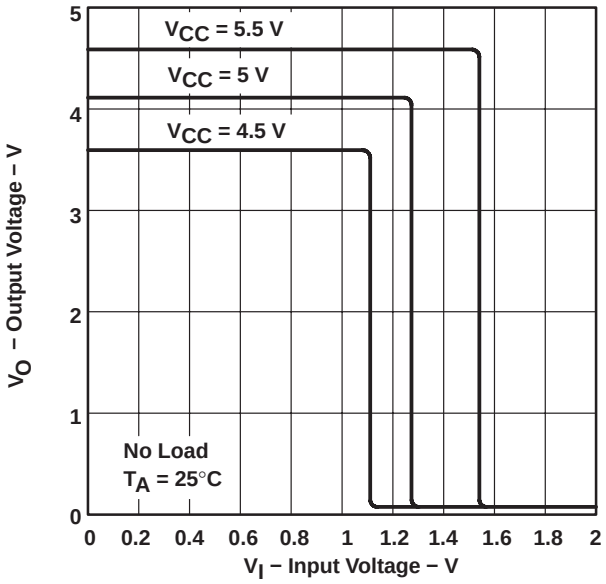


Figure 3

INPUT CURRENT vs INPUT VOLTAGE

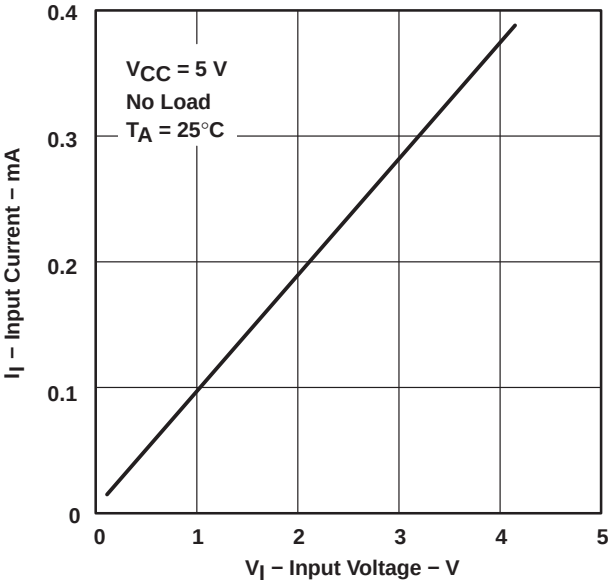


Figure 4

LOW-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT

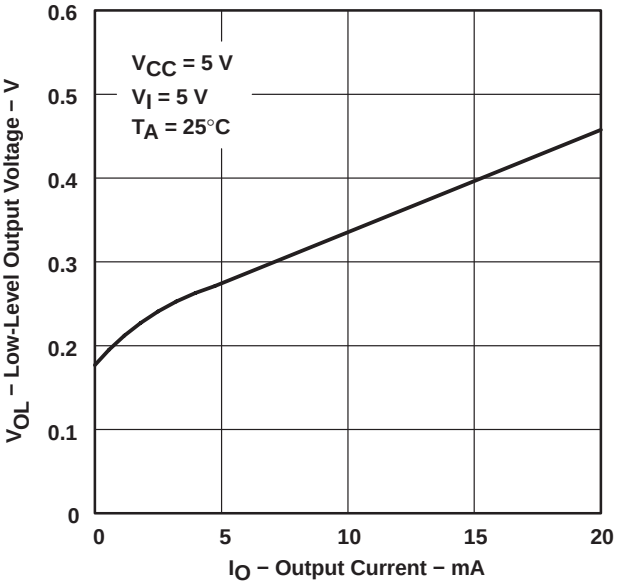


Figure 5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN75128N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN75129DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN75129N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

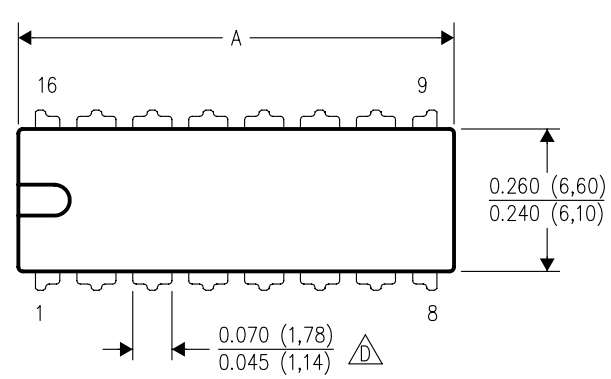
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

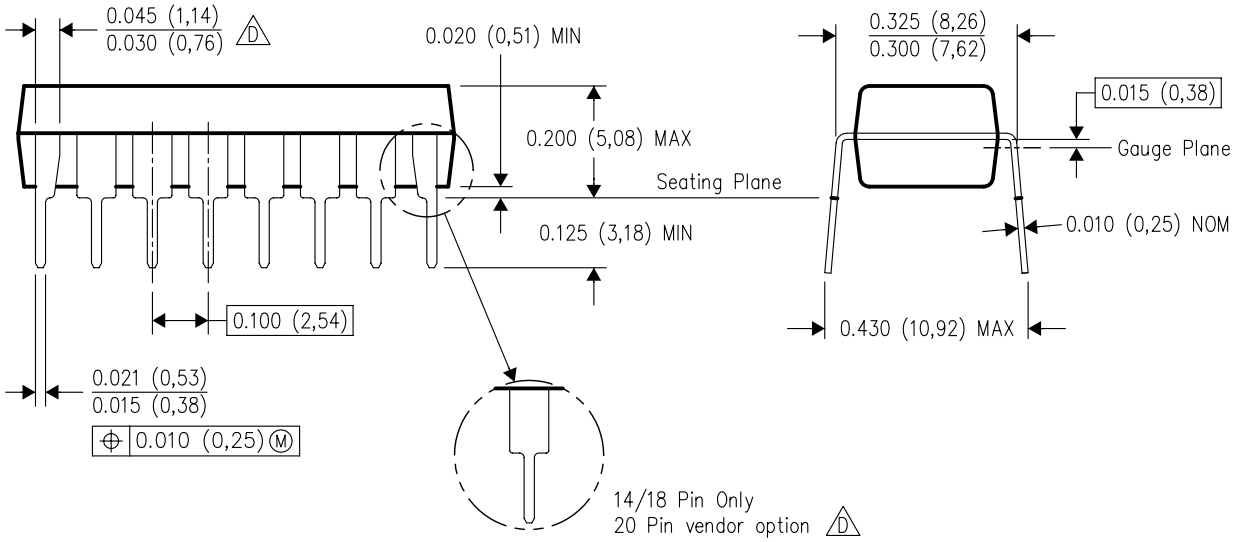
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

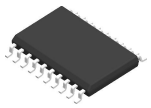


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

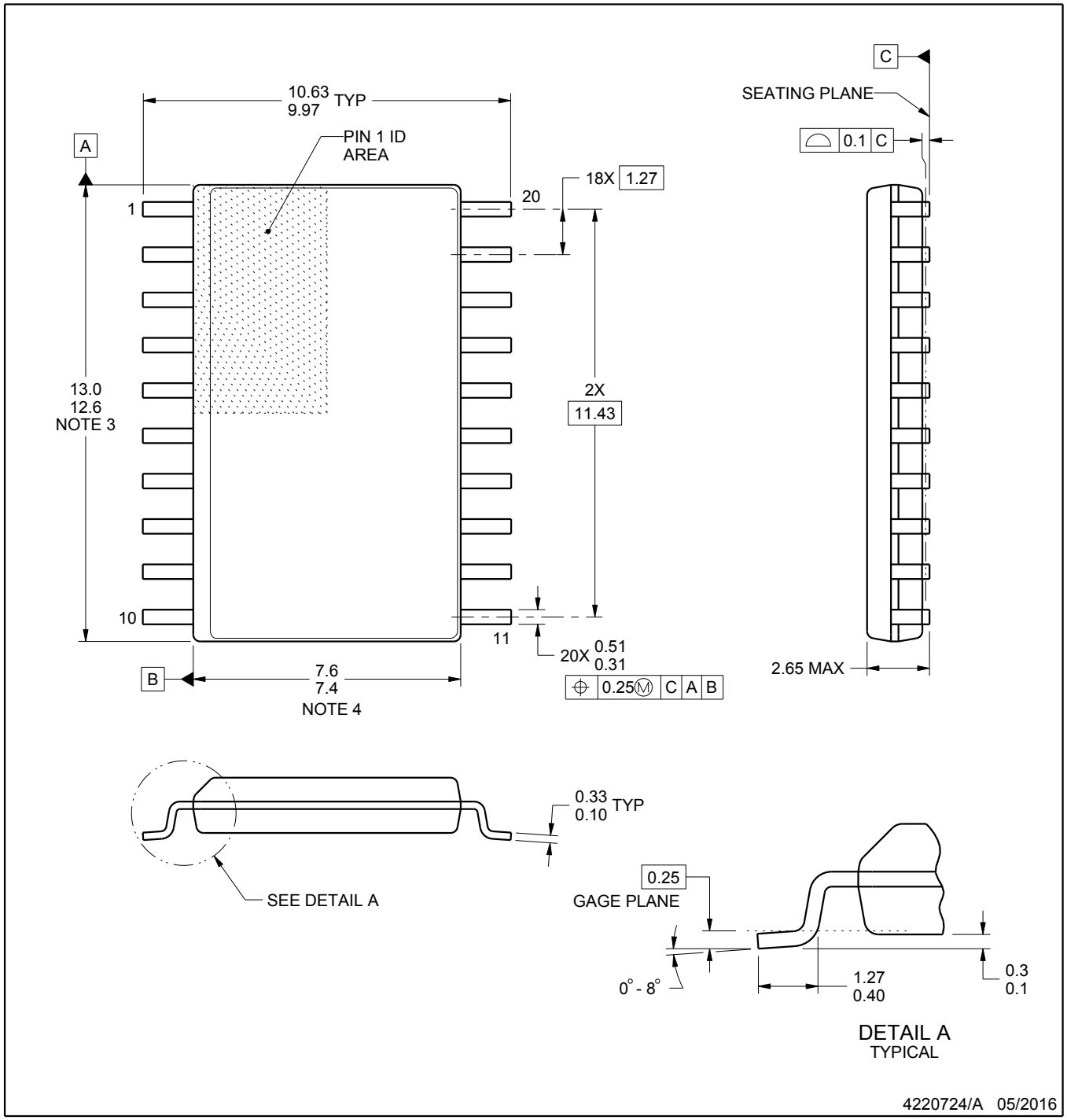


PACKAGE OUTLINE

DW0020A

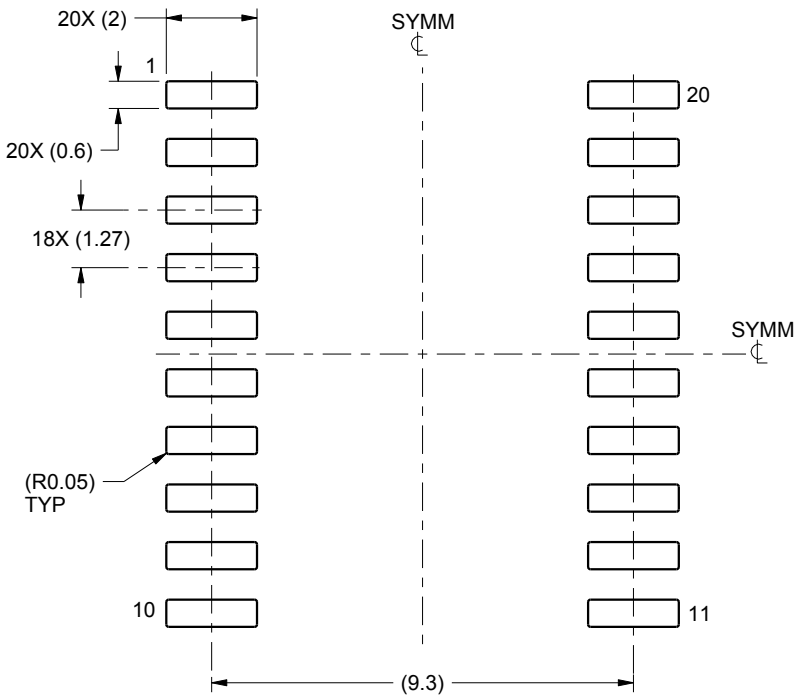
SOIC - 2.65 mm max height

SOIC

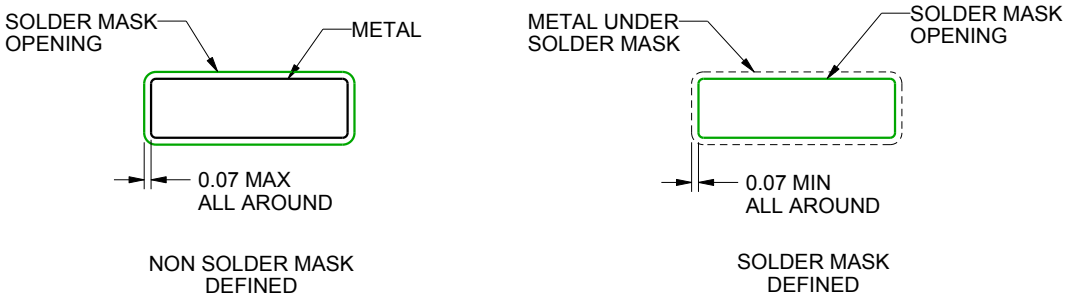


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

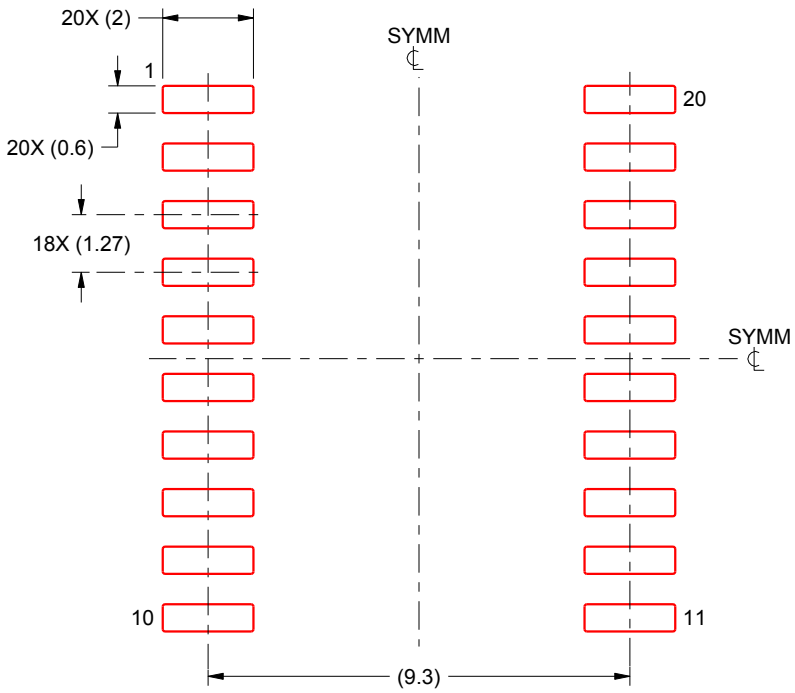


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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