SN75LP185A LOW-POWER MULTIPLE RS-232 DRIVERS AND RECEIVERS

SLLS257G - AUGUST 1996 - REVISED SEPTEMBER 1998

- Single-Chip TIA/EIA-232-F Interface for IBM™ PC/AT™ Serial Port
- Designed to Transmit and Receive 4-μs Pulses (Equivalent to 256 kbit/s)
- Less Than 21-mW Power Consumption
- Wide Supply-Voltage Range, 4.75 V to 15 V
- Driver Output Slew Rates Are Internally Controlled to 30 V/μs Max
- Receiver Input Hysteresis, 1000 mV Typ
- TIA/EIA-232-F Bus-Pin ESD Protection Exceeds:
 - 15-kV, Human-Body Model
 - 15-kV IEC1000-4-2, Air Gap
 - 8-kV IEC1000-4-2. Contact
- Three Drivers and Five Receivers Meet or Exceed the Requirements of TIA/EIA-232-F and ITU V.28
- Complements the SN75LP196
- Designed to Replace the Industry-Standard SN75185 and SN75C185 With the Same Flow-Through Pinout
- Packaged in Plastic Small-Outline Package

DW PACKAGE (TOP VIEW) V_{DD} [20 Vcc RA1 [] 2 RY1 19 RA2 [] 3 RY2 18 RA3 [] 4 RY3 17 DY1 🛮 5 ∏ DA1 16 DY2 6 15 🛮 DA2 RA4 **1** 7 14 RY4 DY3 🛮 8 DA3 13 RY5 RA5 **∏** 9 12 11 | GND V_{SS} 🛮 10

description

The SN75LP185A is a low-power bipolar device containing three drivers and five receivers with 15 kV of ESD protection on the bus pins with respect to each other. Bus pins are defined as those pins that tie directly to the serial-port connector, including GND. The pinout matches the flow-through design of the industry-standard SN75185 and SN75C185. The flow-through pinout of the SN75LP185A allows easy interconnection of the UART and serial-port connector of the IBM PC/AT and compatibles. The SN75LP185A provides a rugged, low-cost solution for this function with the combination of the bipolar processing and 15 kV of ESD protection.

The SN75LP185A has internal slew-rate control to provide a maximum rate of change in the output signal of $30 \text{ V/}\mu\text{s}$. The driver output swing is nominally clamped at $\pm 6 \text{ V}$ to enable the higher data rates associated with this device and to reduce EMI emissions. Even though the driver outputs are clamped, they can handle voltages up to $\pm 15 \text{ V}$ without damage. All the logic inputs can accept 3.3-V or 5-V input signals.

The SN75LP185A complies with the requirements of TIA/EIA-232-F and ITU V.28. These standards are for data interchange between a host computer and peripheral at signaling rates up to 20 kbit/s. The switching speeds of the SN75LP185A support rates up to 256 kbit/s.

The SN75LP185A is characterized for operation from 0°C to 70°C.



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Function Tables

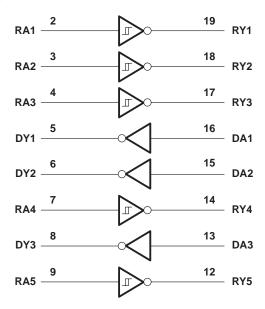
DRIVER

INPUT DA	OUTPUT DY
Н	L
L	Н
Open	L

RECEIVER

INPUT RA	OUTPUT RY
Н	L
L	Н
Open	Н

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Positive supply-voltage range (see	Note 1): V _{CC}	
	V _{DD} (see Note 1)	–0.5 V to 15 V
Negative supply-voltage range, V _{SS}		0.5 V to –15 V
		0.5 V to V _{CC} +0.4 V
		–0.5 V to 6 V
		Class 3, A: 15 kV
		Class 3, B: 500 V
		Class 3, C: 8 kV
		Class 3, D: 15 kV
		Class 3, A: 5 kV
		Class 3, B: 400 V
Package thermal impedance, θ _{IA} (s		
		65°C to 150°C
		260°C
. ,	,	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal, unless otherwise noted.

- 2. Per MIL-STD-883 Method 3015.7
- 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage (see Note 4)		4.75	5	5.25	V
V_{DD}	Supply voltage (see Note 5)		9	12	15	V
VSS	Supply voltage (see Note 5)		-9	-12	-15	V
VIH	High-level input voltage	DA	2			V
V _{IL}	Low-level input voltage	DA			0.8	V
VI	Receiver input voltage	RA	-25		25	V
loh	High-level output current	RY			-1	mA
loL	Low-level output current	RY			2	mA
TA	Operating free-air temperature		0		70	°C

NOTES: 4. V_{CC} cannot be greater than V_{DD}.

5. The device operates down to $V_{DD} = V_{CC}$ and $|V_{SS}| = V_{CC}$, but supply currents increase and other parameters may vary slightly from the data-sheet limits.



SN75LP185A LOW-POWER MULTIPLE RS-232 DRIVERS AND RECEIVERS

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supply currents over the recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS				TYP	MAX	UNIT
Supply current for V _{CC} , I _{CC} Supply current for V _{DD} , I _{DD} Supply current for V _{SS} , I _{SS}		V _{DD} = 9 V,	$V_{SS} = -9 V$			1000	
	No load, All inputs at minimum V _{OH} or maximum V _{OL}	V _{DD} = 12 V,	$V_{SS} = -12 \text{ V}$			1000	
		V _{DD} = 9 V,	$V_{SS} = -9 V$			450	μA
		V _{DD} = 12 V,	$V_{SS} = -12 \text{ V}$			450	μΑ
		V _{DD} = 9 V,	$V_{SS} = -9 V$			-625	
		V _{DD} = 12 V,	$V_{SS} = -12 \text{ V}$			-625	

driver electrical characterisitics over the recommended operating conditions (unless otherwise noted)

	PARAMETER		TEST CO	NDITIONS		MIN	TYP	MAX	UNIT
Vou	High-level output voltage	$V_{IL} = 0.8 \text{ V},$ $R_{I} = 3 \text{ k}\Omega,$	V _{DD} = 9 V,	$V_{SS} = -9 V$		5	5.8	6.6	>
VOH	r ligit-level output voltage	See Figure 1	V _{DD} = 12 V,	$V_{SS} = -12 V$,	See Note 6	5	5.8	6.6	V
Voi	Low-level output voltage	V _{IH} = 2 V,	V _{DD} = 9 V,	$V_{SS} = -9 V$		– 5	-5.8	-6.9	V
VOL	Low-level output voltage	$R_L = 3 \text{ k}\Omega$, See Figure 1	V _{DD} = 12 V,	$V_{SS} = -12 \text{ V},$	See Note 6	-5	-5.9	-6.9	V
lн	High-level input current	V _I at V _{CC}	V _I at V _{CC}					1	μΑ
Iμ	Low-level input current	V _I at GND						-1	μΑ
IOS(H)	Short-circuit high-level output current	VO = GND or V	SS,	See Figure 2 a	nd Note 7		-30	- 55	mA
I _{OS(L)}	Short-circuit low-level output current	$V_O = GND \text{ or } V_{DD},$		See Figure 2 a	nd Note 7		30	55	mA
r _O	Output resistance	$V_{DD} = V_{SS} = V_{SS}$	CC = 0,	V _O = 2 V		300			Ω

NOTES: 6. Maximum output swing is nominally clamped at ±6 V to enable the higher data rates associated with this device and to reduce EMI emissions. The driver outputs may slightly exceed the maximum output voltage over the full VCC and temperature ranges.



^{7.} Not more than one output should be shorted at one time.

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driver switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
tPHL	Propagation delay time, high- to low-level output	$R_L = 3 \text{ k}\Omega \text{ to } 7 \text{ k}\Omega, C$	C _L = 15 pF, See Figure 1	300	800	1600	ns
tPLH	Propagation delay time, low- to high-level output	$R_L = 3 \text{ k}\Omega \text{ to } 7 \text{ k}\Omega, C$	C _L = 15 pF, See Figure 1	300	800	1600	ns
		V _{CC} = 5 V,	Using V _{TR} = 10%-to-90% transition region, Driver speed = 250 kbit/s, C _L = 15 pF, See Note 8	375		2240	
tTLH	Transition time,	$V_{DD} = 12 \text{ V},$ $V_{SS} = -12 \text{ V},$	Using V _{TR} = ± 3 V transition region, Driver speed = 250 kbit/s, C _L = 15 pF	200		1500	ns
	Iow- to high-level output	$R_L = 3 kΩ$ to 7 kΩ, See Figure 1 and Note 9	Using $V_{TR} = \pm 2 \text{ V}$ transition region, Driver speed = 250 kbit/s, $C_L = 15 \text{ pF}$	133		1000	
			Using V _{TR} = ±3 V transition region, Driver speed = 125 kbit/s, C _L = 2500 pF			2750	
		, 00	Using V _{TR} = 10%-to-90% transition region, Driver speed = 250 kbit/s, C _L = 15 pF, See Note 8	375		2240	
tTHL	Transition time, tTHL high- to low-level output		Using $V_{TR} = \pm 3 \text{ V}$ transition region, Driver speed = 250 kbit/s, $C_L = 15 \text{ pF}$	200		1500	ns
			Using $V_{TR} = \pm 2 \text{ V}$ transition region, Driver speed = 250 kbit/s, $C_L = 15 \text{ pF}$	133		1000	
			Using V _{TR} = ± 3 V transition region, Driver speed = 125 kbit/s, C _L = 2500 pF			2750	
SR	Output slew rate	V _{CC} = 5 V, V _{DD} = 12 V, V _{SS} = -12 V	Using V _{TR} = ±3 V transition region, Driver speed = 0 to 250 kbit/s, C _L = 15 pF	4	20	30	V/us

NOTES: 8. Equivalent to the SN75C185. The SN75LP185A output-voltage swing is clamped to about 70% of the typical SN75C185 output-voltage swing, and the specified limits reflect the reduced output swing.

9. Maximum output swing is limited to ± 6 V to enable the higher data rates associated with this device and to reduce EMI emissions.

receiver electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TE	ST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage	See Figure 3		1.6	2	2.55	V
V _{IT} _	Negative-going input threshold voltage	See Figure 3		0.6	1	1.45	V
V _{HYS}	Input hysteresis, V _{IT+} V _{IT-}	See Figure 3		600	1000		mV
Vон	High-level output voltage	$I_{OH} = -1 \text{ mA}$		2.5	3.9		V
VoL	Low-level output voltage	$I_{OL} = 2 \text{ mA}$			0.33	0.5	V
l	I High level inner compart		V _I = 3 V		0.6	1	mA
lΗ	High-level input current	V _I = 25 V		3.6	5.1	8.3	IIIA
1	Low lovel input ourrent	V _I = −3 V		-0.43	-0.6	-1	mA
¹IL	Low-level input current	V _I = -25 V		-3.6	-5.1	-8.3	IIIA
IOS(H)	Short-circuit high-level output current	$V_{O} = 0,$	See Figure 5 and Note 7			-20	mA
I _{OS(L)}	Short-circuit low-level output current	$V_O = V_{CC}$	See Figure 5 and Note 7			20	mA
R _{IN}	Input resistance	$V_{ } = \pm 3 \text{ V to } \pm 25$	V	3	5	7	kΩ

NOTE 7: Not more than one output should be shorted at one time.

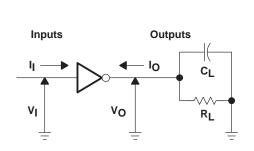


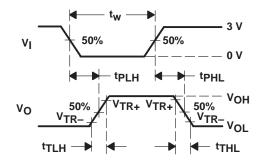
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receiver switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 4)

	PARAMETER	MIN	TYP	MAX	UNIT
tPHL	Propagation delay time, high- to low-level output		400	900	ns
tPLH	Propagation delay time, low- to high-level output		400	900	ns
tTLH	Transition time, low- to high-level output		200	500	ns
tTHL	Transition time, high- to low-level output		200	400	ns
tSK(p)	Pulse skew tpLH tpHL		200	425	ns

PARAMETER MEASUREMENT INFORMATION





NOTES: A. The pulse generator has the following characteristics: For C_L < 1000 pF: t_W = 4 μ s, PRR = 250 kbit/s, Z_O = 50 Ω , t_T = t_f < 50 ns. For C_L = 2500 pF: t_W = 8 μ s, PRR = 125 kbit/s, Z_O = 50 Ω , t_T = t_f < 50 ns.

B. C_L includes probe and jig capacitance.

Figure 1. Driver Parameter Test Circuit and Waveform

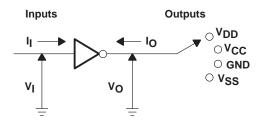


Figure 2. Driver IOS Test

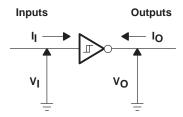
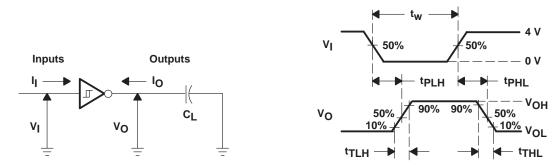


Figure 3. Receiver VIT Test



PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: t_W = 4 μ s, PRR = 250 kbit/s, Z_O = 50 Ω , t_f = t_f < 50 ns.

B. C_L includes probe and jig capacitance.

Figure 4. Receiver Parameter Test Circuit and Waveform

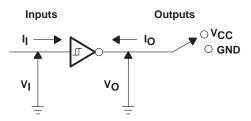


Figure 5. Receiver IOS Test

APPLICATION INFORMATION

Diodes placed in series with the V_{DD} and V_{SS} leads protect the SN75LP185A in the fault condition when the device outputs are shorted to ± 15 V and the power supplies are at low voltage and provide low-impedance paths to ground (see Figure 6).

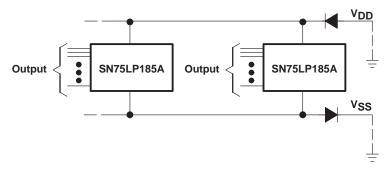


Figure 6. Power-Supply Protection to Meet Power-Off Fault Conditions of TIA/EIA-232-F



PACKAGE OPTION ADDENDUM

30-Mar-2005

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN75LP185ADW	OBSOLETE	SOIC	DW	20	TBD	Call TI	Call TI
SN75LP185ADWR	OBSOLETE	SOIC	DW	20	TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



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