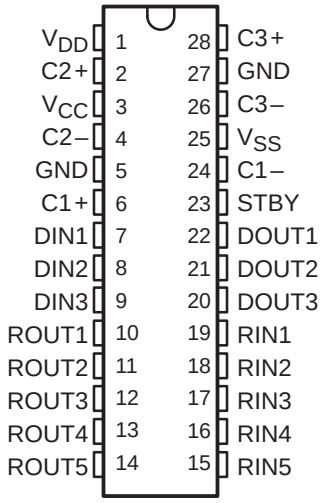
SLLS135E – FEBRUARY 1992 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI EIA/TIA-232-E and ITU V.28**
- **Operates With Single 3.3-V Power Supply**
- **LinBiCMOS™ Process Technology**
- **Three Drivers and Five Receivers**
- **±30-V Input Levels (Receiver)**
- **ESD Protection on RS-232 Lines Exceeds 6 kV Per MIL-STD-883C, Method 3015**
- **Applications**
  - **EIA/TIA-232 Interface**
  - **Battery-Powered Systems**
  - **Notebook PC**
  - **Computers**
  - **Terminals**
  - **Modems**
- **Voltage Converter Operates With Low Capacitance . . . 0.47 μF Min**
- **Functionally Compatible With the SN75LV4737A**

DB PACKAGE
(TOP VIEW)



† The DB package is only available in left-end taped and reeled (SN75LV4735DBLE).

description

The SN75LV4735† is a low-power 3.3-V multichannel RS-232 line driver/receiver. It includes three independent RS-232 drivers and five independent RS-232 receivers. It is designed to operate off a single 3.3-V supply and has an internal switched-capacitor voltage converter to generate the RS-232 output levels. The SN75LV4735 provides a single chip, single 3.3-V supply interface between the asynchronous communications element (ACE or UART) and the serial-port connector of the data terminal equipment (DTE). This device has been designed to conform to standard ANSI EIA/TIA-232-E.

The switched-capacitor voltage converter of the SN75LV4735 uses five small external capacitors to generate the positive and negative voltages required by EIA/TIA-232-E line drivers from a single 3.3-V input. The drivers feature output slew-rate limiting to eliminate the need for external filter capacitors. The receivers can accept ±30 V without damage.

The device also features a reduced power or standby mode that cuts the quiescent power to the integrated circuits when not transmitting data between the CPU and peripheral equipment. The STBY input is driven high for standby (reduced power) mode and driven low for normal operating mode. When in the standby mode, all driver outputs (DOUT1–3) and receiver outputs (ROUT1–5) are in the high-impedance state. If the standby feature is not used in an application, STBY should be tied to GND.

The SN75LV4735 has been designed using LinBiCMOS™ technology and cells contained in the Texas Instruments LinASIC™ library. The SN75LV4735 is characterized for operation from 0°C to 70°C.

† Patent-pending design

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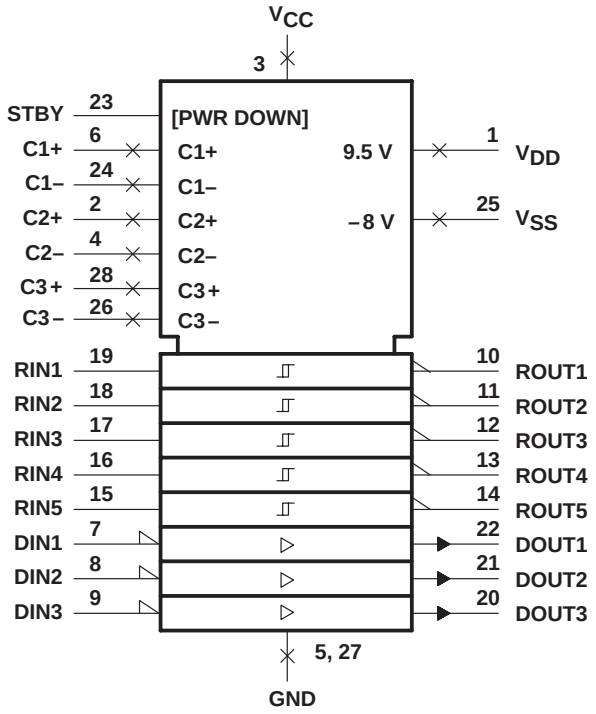
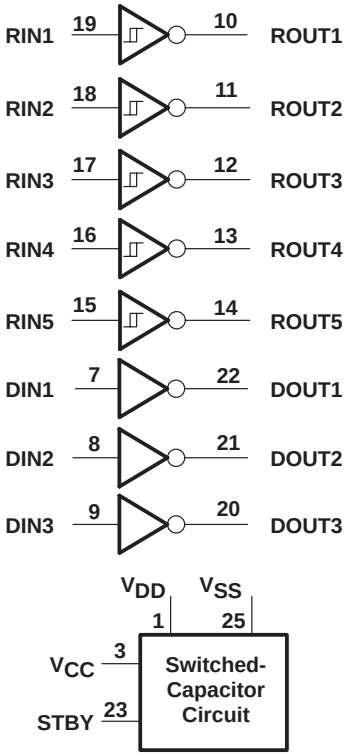
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Function Tables

EACH DRIVER

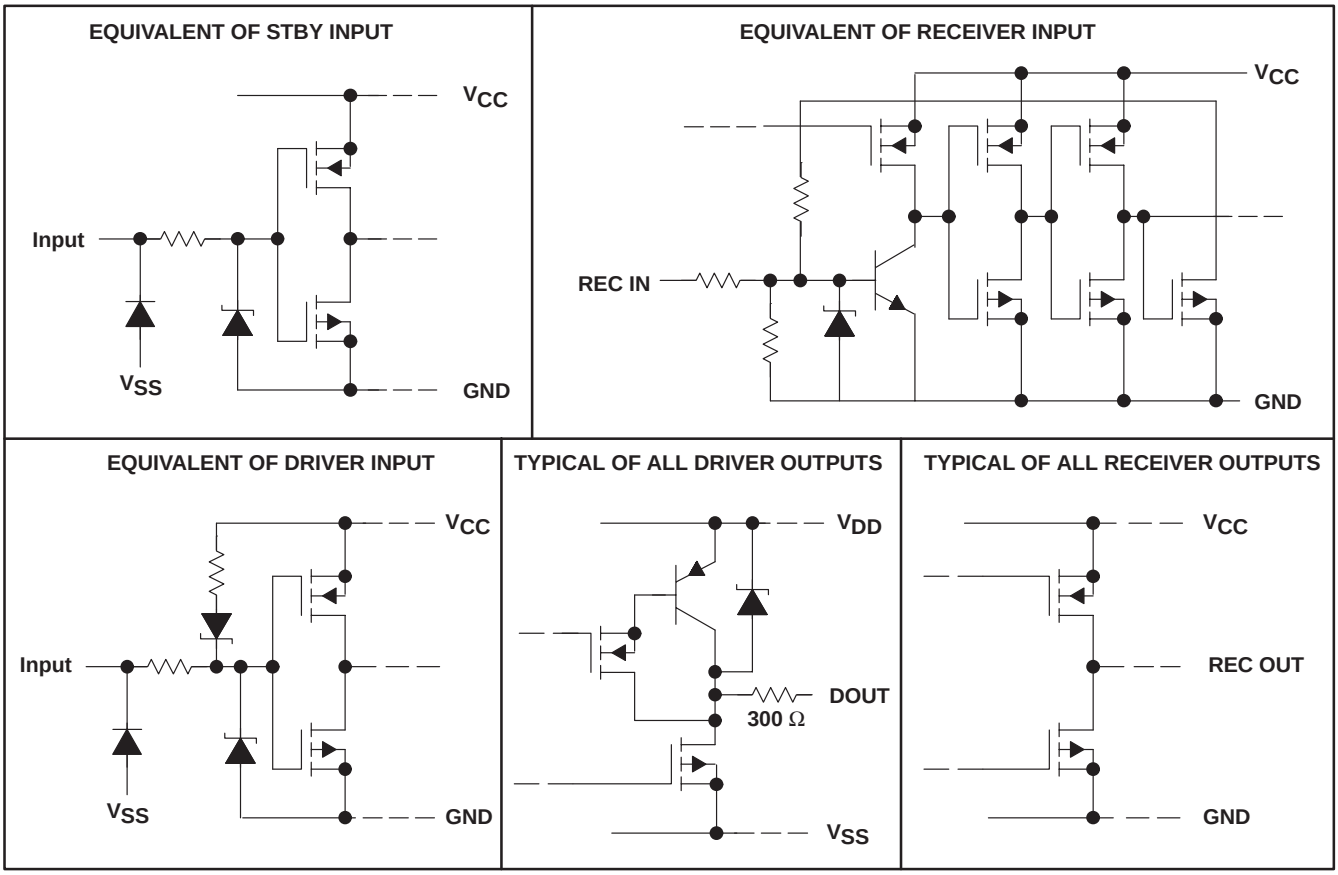
INPUTS		OUTPUT
DIN	STBY	
X	H	Z
L	L	H
H	L	L
Open	L	L

EACH RECEIVER

INPUTS		OUTPUT
RIN	STBY	
X	H	Z
L	L	H
H	L	L
Open	L	H

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 4 V
Positive output supply voltage, V_{DD} (see Note 1) . . . . . 15 V
Negative output supply voltage, V_{SS} . . . . . –15 V
Input voltage range, V_I: DIN1–DIN3, STBY . . . . . –0.3 V to 7 V
RIN1–RIN5 . . . . . –30 V to 30 V
Output voltage range, V_O: DOUT1–DOUT3 . . . . . V_{SS} – 0.3 V to V_{DD} + 0.3 V
ROUT1–ROUT5 . . . . . –0.3 V to 7 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to network GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DB	668 mW	5.3 mW/°C	430 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
Positive output supply voltage, V_{DD}		8	10		V
Negative output supply voltage, V_{SS}		–7	–8		V
Input voltage, V_I (see Note 2)	RIN(1–5)			±30	V
High-level input voltage, V_{IH}	DIN(1–3), STBY	2			V
Low-level input voltage, V_{IL}	DIN(1–3), STBY			0.8	V
External capacitor		0.47	1		µF
Operating free-air temperature, T_A		0		70	°C

NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only. For example, if –10 V is a maximum, the typical value is a more negative voltage.

supply currents

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current from V_{CC} (normal operating mode)	No load, STBY AT 0 V, All other inputs open		8.5	20	mA
$I_{CC(SB)}$	Supply current (standby mode)	No load, STBY at V_{CC}, All other inputs open			10	µA

DRIVER SECTION

electrical characteristics over operating free-air temperature range, V_{CC} = 3.3 V ±0.3 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		R_L = 3 kΩ	5.5	7		V
V_{OL}	Low-level output voltage (see Note 2)		R_L = 3 kΩ		–5.5	–5	V
I_{IH}	High-level input current		V_I at V_{CC}			1	µA
I_{IL}	Low-level input current	STBY	V_I at GND			–1	µA
		Other inputs	V_I at GND			–10	µA
$I_{OS(H)}$	High-level short-circuit output current (see Note 3)		V_{CC} = 3.6 V, V_O = 0		–10	–20	mA
$I_{OS(L)}$	Low-level short-circuit output current (see Note 3)		V_{CC} = 3.6 V, V_O = 0		10	20	mA
r_O	Output resistance		V_{CC} = V_{DD} = V_{SS} = 0, V_O = –2 V to 2 V, See Note 4	300			Ω

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTES: 2. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.
3. Not more than one output should be shorted at one time.
4. Test conditions are those specified by EIA/TIA-232-E.

switching characteristics, V_{CC} = 3.3 V ±0.3 V, T_A = 0°C to 70°C

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 3 kΩ to GND, C_L = 50 pF, See Figure 2	200	400	600	ns
t_{PHL}	Propagation delay time, high- to low-level output		100	200	350	ns
t_{PZL}	Output enable time to low level (see Note 5)	R_L = 3 kΩ to GND, C_L = 50 pF, See Figure 3		3	7	ms
t_{PZH}	Output enable time to high level (see Note 5)			1	5	ms
t_{PHZ}	Output disable time from high level (see Note 5)			1	3	µs
t_{PLZ}	Output disable time from low level (see Note 5)			0.5	3	µs
SR	Output slew rate (see Note 6)	R_L = 3 kΩ to 7 kΩ, C_L = 50 pF, See Figure 2	3		30	V/µs
SR(tr)	Transition-region slew rate	R_L = 3 kΩ to GND, C_L = 2500 pF, See Figure 4		3		V/µs

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTES: 5. Output enable occurs when STBY is driven low. Output disable occurs when STBY is driven high.
6. Measured between 3-V and –3-V points of output waveform (EIA/TIA-232-E conditions); all unused inputs are tied either high or low.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			2.2	2.6	V
V_{IT-}	Negative-going input threshold voltage		0.6	1		V
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)		0.5	1.2	1.8	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA, See Note 7	2.4	2.6		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA		0.2	0.4	V
r_I	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTE 7: If the inputs are left unconnected, the receiver interprets this as an input low, and the receiver outputs remain in the high state.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 3 kΩ to GND, See Figure 5	45	80	130	ns
t_{PHL}	Propagation delay time, high- to low-level output		70	100	170	ns
t_{PZL}	Output enable time to low level (see Note 5)	R_L = 3 kΩ to GND, See Figure 6		160	250	ns
t_{PZH}	Output enable time to high level (see Note 5)			4	10	µs
t_{PHZ}	Output disable time from high level (see Note 5)			300	500	ns
t_{PLZ}	Output disable time from low level (see Note 5)			140	200	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTE 5: Output enable occurs when STBY is driven low. Output disable occurs when STBY input is driven high.

APPLICATION INFORMATION

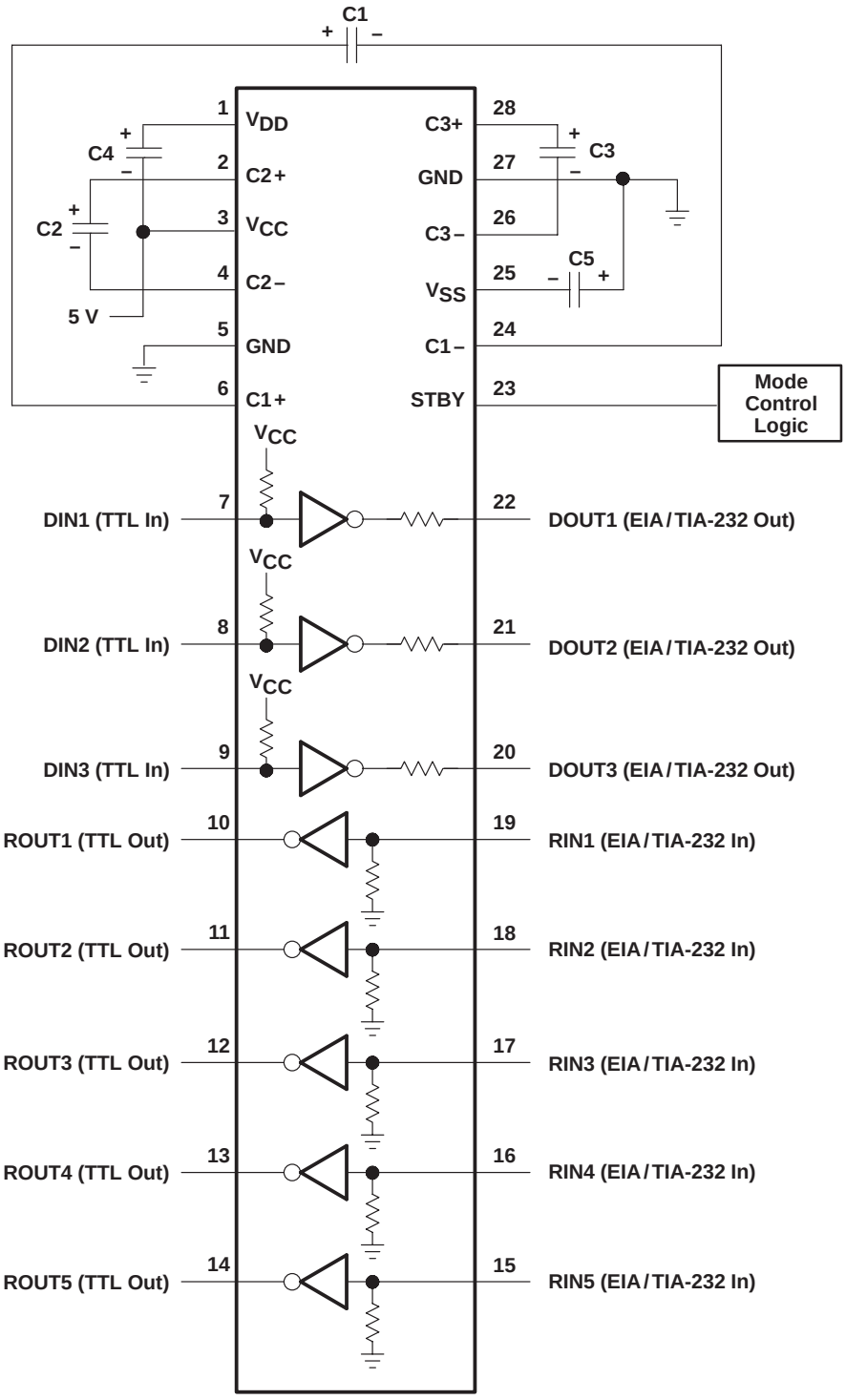
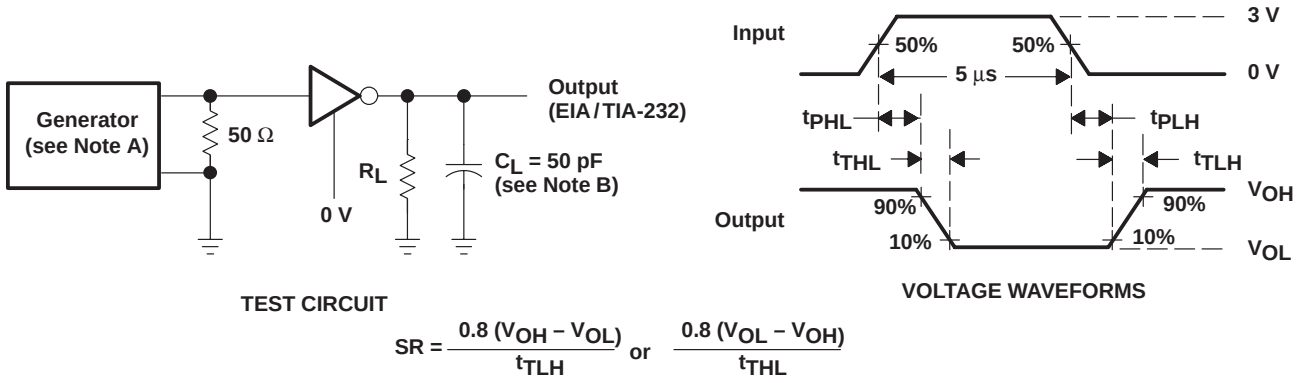


Figure 1. Typical Operating Circuit

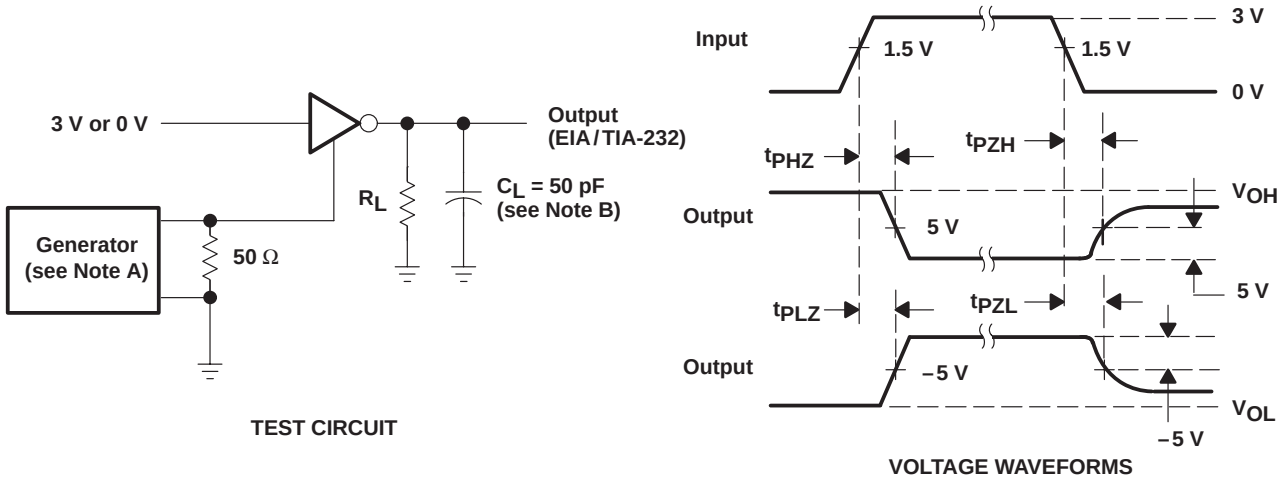
PARAMETER MEASUREMENT INFORMATION



$$SR = \frac{0.8\,(V_{OH} - V_{OL})}{t_{TLH}} \text{ or } \frac{0.8\,(V_{OL} - V_{OH})}{t_{THL}}$$

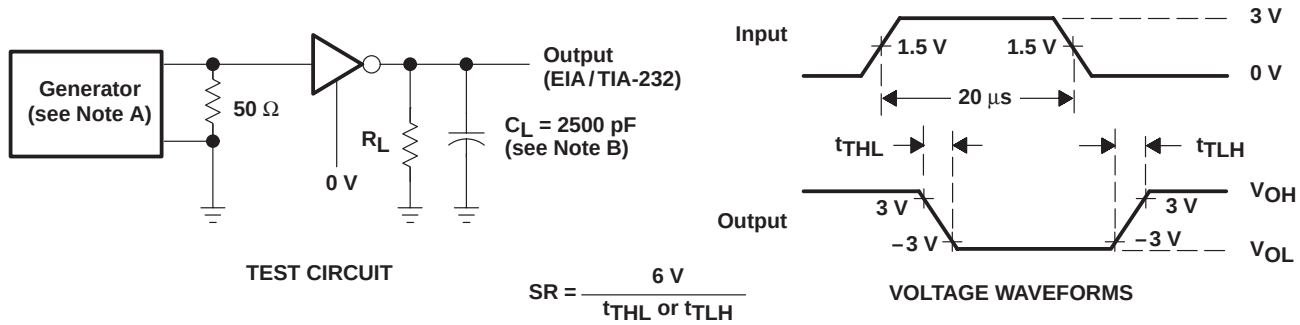
NOTES: A. The pulse generator has the following characteristics: 50% duty cycle, $t_r \le 10$ ns, $t_f = 10$ ns.
B. C_L includes probe and jig capacitance.

Figure 2. Driver Test Circuit and Voltage Waveforms, Slew Rate at 5-μs Input



NOTES: A. The pulse generator has the following characteristics: 50% duty cycle, $t_r \le 10$ ns, $t_f = 10$ ns.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

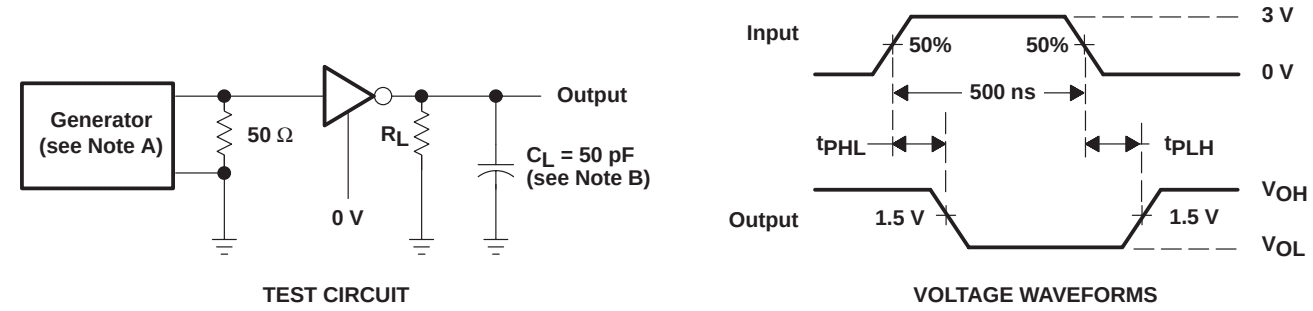


$$SR = \frac{6\text{ V}}{t_{THL} \text{ or } t_{TLH}}$$

NOTES: A. The pulse generator has the following characteristics: 50% duty cycle, $t_r \le 10$ ns, $t_f = 10$ ns.
B. C_L includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms, Slew Rate at 20-μs Input

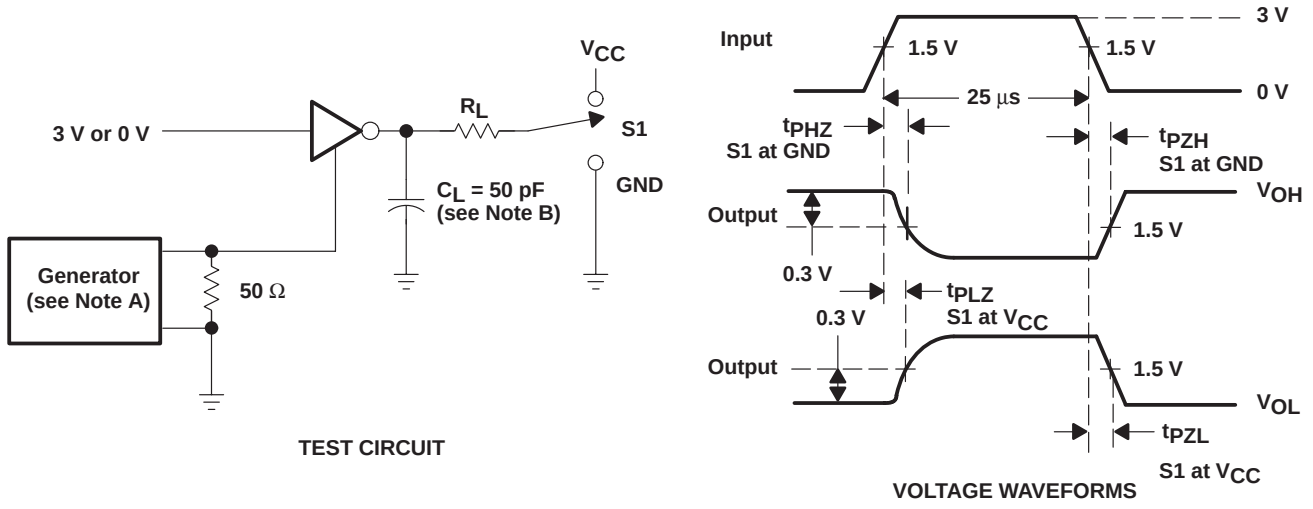
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \le 10$ ns, $t_f = 10$ ns.
B. C_L includes probe and jig capacitance.

Figure 5. Receiver Test Circuit and Voltage Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

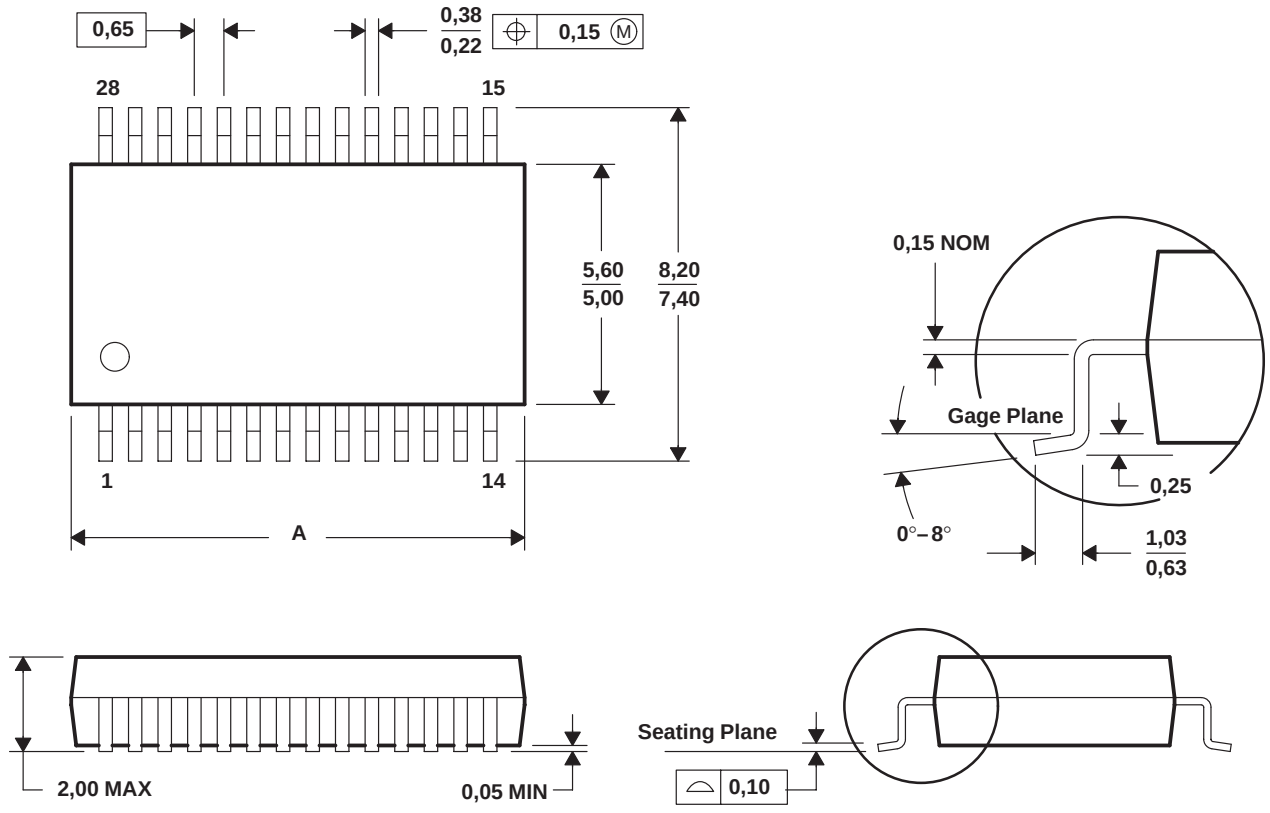
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \le 10$ ns, $t_f = 10$ ns.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms Enable and Disable Times

MECHANICAL DATA

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

28 PIN SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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