1. General Description

Sonix SN93300 series is a 2.4GHz wireless multi-media processor that target on wireless transmission for video, audio and data applications. It supports at least 3 popular types of 2.4GHz RF transceiver, including

Nordic® nRF24L01,
AMICCOM® A7121,
Muchip® MU2302.

Within bandwidth limit of 2Mbps, 3Mbps and 4Mbps data rate for each brand RF transceiver, SN93300 supports 1-way video, 2-way audio and 2-way data transmission. SN93300 implements most popular LCD panel interfaces and supports ISP CMOS sensor interface.

For PC peripheral applications, it supports USB 1.1 interface and follow UVC/UAC driver-less class compliance of Microsoft® XP® SP2 or VISTA® OS.

2. Features

- Support 2.4GHz ISM band FSK RF transceivers.
- Firmware protocol base adaptive FHSS (frequency hopping spreading spectrum). Meet telecommunication regulations.
  - FCC 15.247
  - CE ETSI EN 300 328-1
- Built-in baseband supports antenna diversity for receiver.
- Built-in PLL for internal clock generation with input crystal frequency of 12MHz.
- Built-in wake up function for remote power-on/off control.
- Using external serial flash to store customized code and data.
- No external SDRAM needed.
- Path delay from Tx camera to Rx display has less than 0.1 second for video and audio.
- Remote command delay has less than 0.01 second.
- Packages of LQFP 48/80/100
- USB 1.1 interface.
  - USB Video Class 1.1 compliant.
  - USB Audio Class 1.0 compliant.
- Support ISP CMOS sensor interface with 16-bit YUY2 format.
- 1/2, 1/4 image scaling function to keep fully view angle for small size panel.
- Support 1.5X or 2X digital zoom-in function for VGA sensor.
- For VGA sensor, combined scaling and windowing function provides similar view angle for QVGA/QQVGA output format.
- Built-in JPEG codec.
- Built-in TV encoder.
- Support image DSP technology to eliminate blocking effect.
- Support digital microphone interface to eliminate MIC interference by RF antenna.
- Support snapshot function and store images in serial flash.
- Preview snapshot by
  - LCD panel
  - PC software via USB download
- Receiver image frame rate
  - Max. 30 frame/sec @ QQVGA
  - Max. 30 frame/sec @ QVGA
  - Max. 15 frame/sec @ VGA
- Support OSD (On Screen Display).
  - Maximum 128 characters.
  - Each character has 16x16 or 8x8 dot matrix option.
  - Each character has 4 colors, 1 background color and transparency option.
- Support panel types: TFT/CSTN/LTPS
- Video output interfaces:
  - UPS051
  - RGB Dummy
  - 8080 IF (CPU IF)
  - Parallel RGB (8 bit x 3)
  - YUV422 (Sensor IF)
  - BT601 (output h-sync, v-sync, 8/16 bit data, 13.5MHz clock)
  - BT656 (output 8 bit data, 27MHz clock)
  - CVBS
- Video input interfaces:
  - YUV422 (Sensor IF)
  - BT656
- Built-in 4 of 10 bit, 8K/16K sampling rate ADC for microphone, AD key, battery detection and general purpose analog input.
- Built-in 10 bit, 8K/16K sampling rate DAC for analog audio output.
- Support GPIO and PWM pin for local or remote control.
- PWM pins support stepper motor control.
- Each GPIO has wakeup capability.
- Support multiple ID for security.
- System current assumption:
  - Camera-site : 100mA~200mA (RF+PA+SN93300+Sensor)
  - Monitor-site : 100mA~200mA (RF+PA+SN93300+Panel)

3. Applications

- Baby Monitor
- Wireless PC-Camera
- Home Security
- Camera Radio Controlled Toy
- Video Door Bell
- Vision-Based Robotic System
- Wireless Backup Camera
- Wireless Photo Frame

4. 2.4GHz Devices Coexistence and Anti-interference

In 2.4GHz ISM band, SN93300 overcomes different interferences, like microwave-oven, and work coexistence with other 2.4GHz wireless devices, like cordless phone, WiFi, bluetooth, wireless keyboard and mouse. The robust anti-interference capability is controlled by Sonix adaptive frequency hopping spreading spectrum protocol.

Sonix adaptive frequency hopping spreading spectrum protocol provides enough flexible to help customers to meet telecommunication regulations.

5. Selection Guide

	Package	Body Size (mm^2) & Pitch (mm)	Position of Application	Interface														GPIO option						
				RF	Sensor Port (input option)			LCD port (output option)								USB	UART	Pure GPIO	Wakeup pin #	PWM / Motor control	ADC	DAC	Digital Microphone	RC- OSC Wakeup
					YUV 422	BT656	I^2C	UPS051 / UPS052	RGB dummy	8080 (CPU)	18-bit Parallel RGB	24-bit Parallel RGB	YUV 422 output	BT601 / BT656	TV-out	GPIO									
SN93110	LQFP-48	7x7 0.5	• USB	√												0	√	√	8		2	0	0		
SN93310	LQFP-48	7x7 0.5														0	√		7		1	0	0		
SN93130	LQFP-80	10x10 0.4	• Panel • TV-out • USB	√				√	√	√	√					22	√	√	6	2	1	4	1		√
SN93330	LQFP-100	14x14 0.5						√	√	√	√	√	√	√	√	28	√		14	14	2	4	1	√	√
SN93131	LQFP-80	10x10 0.4	• Camera • TV-in	√	√		√									8		√	8	2	2	4	1		√
SN93331	LQFP-80	10x10 0.4			√	√	√									5			10	10	2	4	1	√	√

6. System Block Diagram

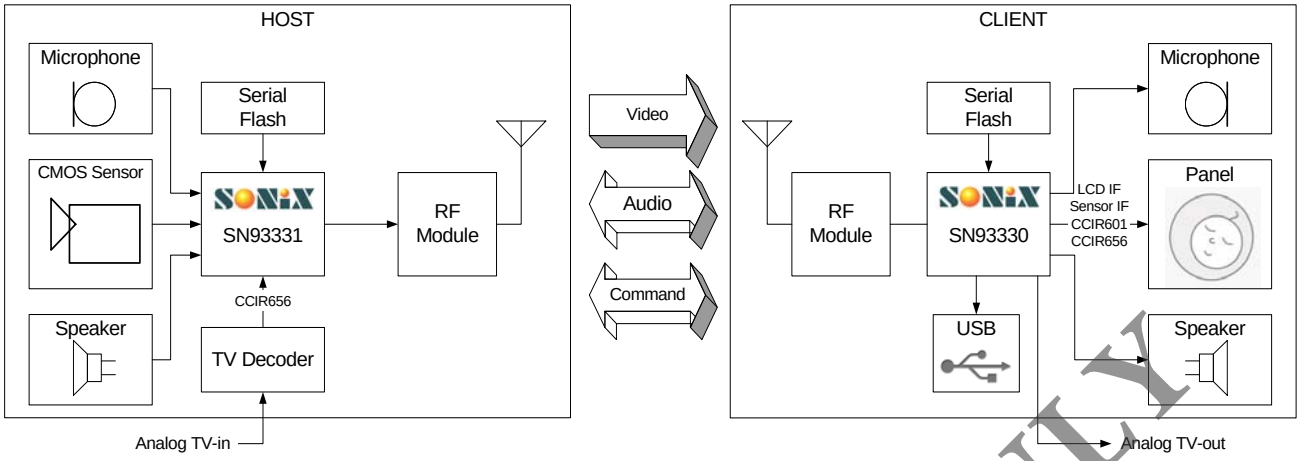


Fig 1. CMOS + SN93331 + SN93330

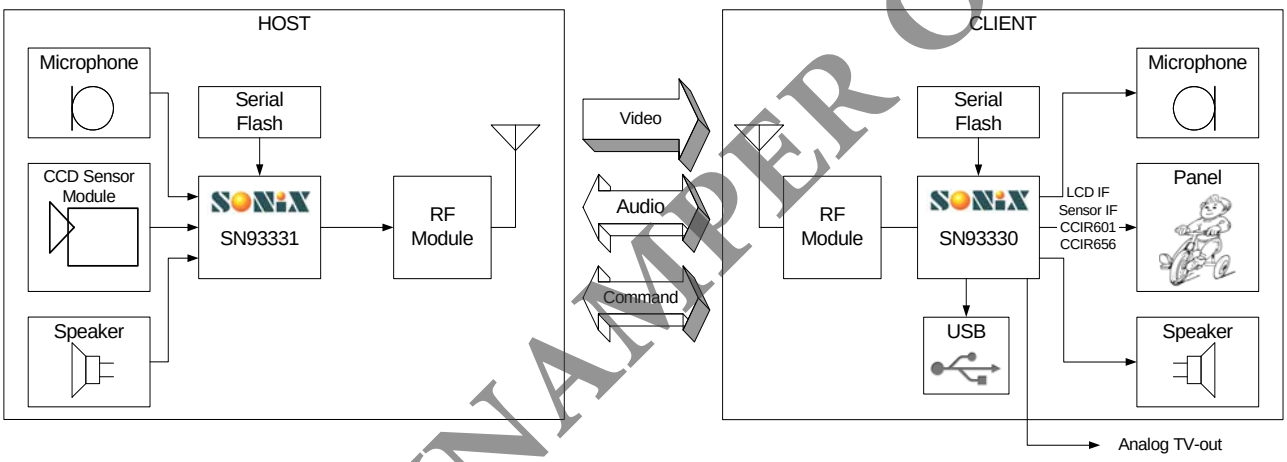


Fig 2. CCD Module + SN93331 + SN93330

(For wireless backup camera application)

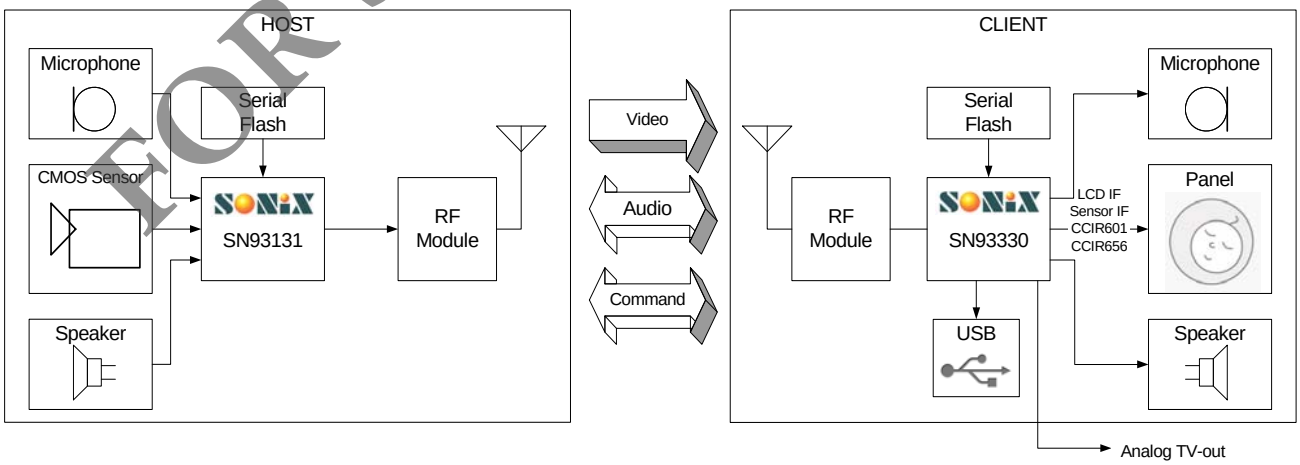
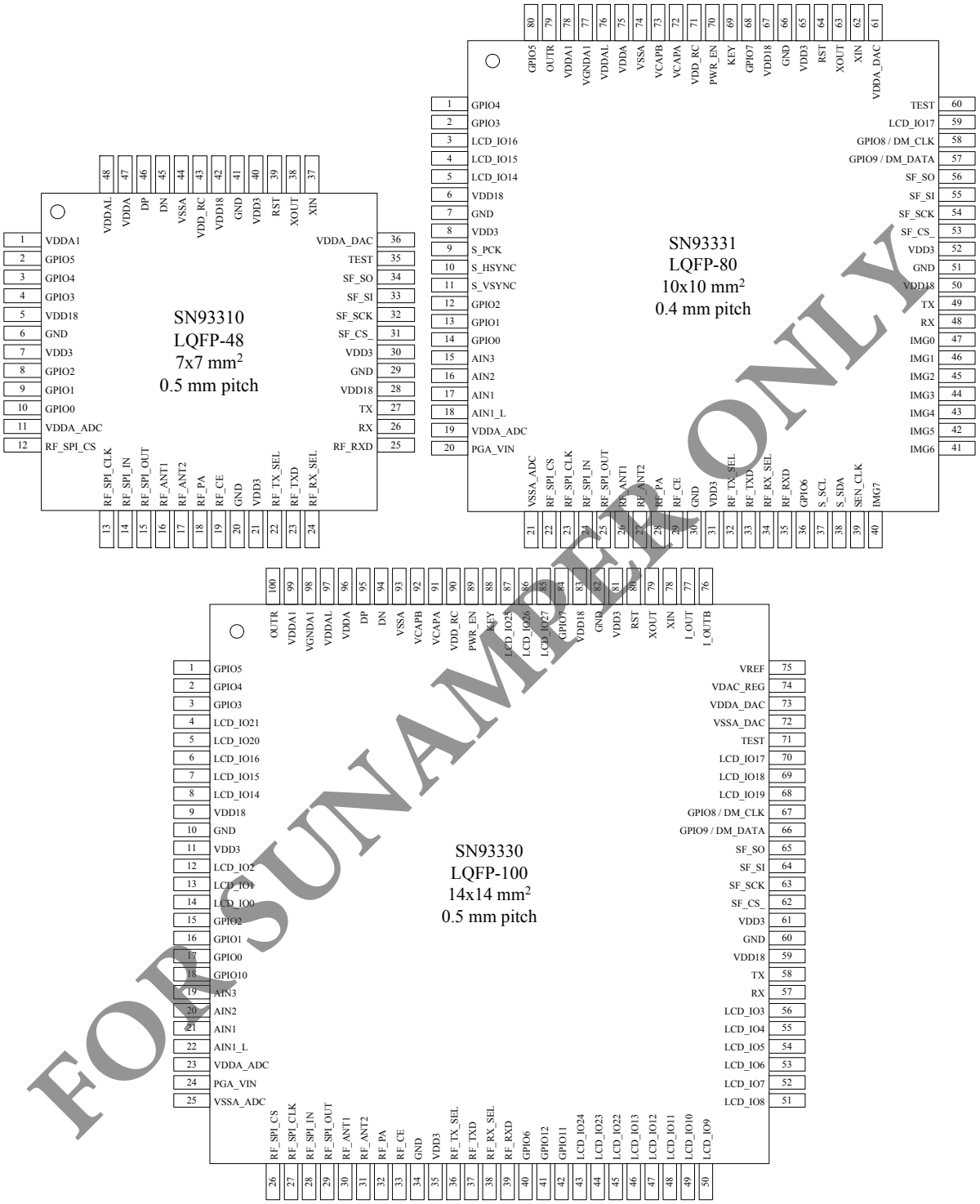


Fig 3. SN93131 + SN93330

(Compatible with SN93131 Host)

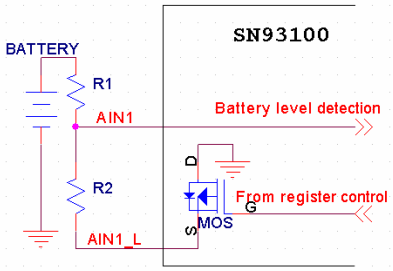
7. Pin Diagram



8. Pin Description

Note: (SUB) means internal pad bond to dice substrate.

SN93330 LQFP-100	SN93331 LQFP-80	SN93310 LQFP-48	Pin Name	DIR	PD/U FAST	Description
1	80	2	GPIO5	B	8mA	General-purpose I/O
2	1	3	GPIO4	B	8mA	General-purpose I/O
3	2	4	GPIO3	B	8mA	General-purpose I/O

SN93330 LQFP-100	SN93331 LQFP-80	SN93310 LQFP-48	Pin Name	DIR	PD/U FAST	Description
4			LCD_IO21	B	4mA	LCD_IO
5			LCD_IO20	B	4mA	LCD_IO
6	3		LCD_IO16	B	4mA	LCD_IO
7	4		LCD_IO15	B	4mA	LCD_IO
8	5		LCD_IO14	B	4mA	LCD_IO
9	6	5	VDD18	P		1.8V core power
10 (SUB)	7 (SUB)	6 (SUB)	GND	P		Core & I/O ground
11	8	7	VDD3	P		3.3V I/O power
12	9		LCD_IO2 / S_PCK	B	4mA	LCD_IO/PCK
13	10		LCD_IO1 / S_HSYNC	B	4mA	LCD_IO/HSYNC
14	11		LCD_IO0 / S_VSYNC	B	4mA	LCD_IO/VSYNC
15	12	8	GPIO2	B	8mA	General-purpose I/O
16	13	9	GPIO1	B	8mA	General-purpose I/O
17	14	10	GPIO0	B	8mA	General-purpose I/O
18			GPIO10	B	8mA	General-purpose I/O
19	15		AIN3	B		Analog input channel 3. Input level: 0V~2V.
20	16		AIN2	B		Analog input channel 2. Input level: 0V~2V.
21	17		AIN1	B		Analog input channel 1. Input level: 0V~2V. (For battery detection)
22	18		AIN1_L	B		Register controlled internal MOS Gate to floating AIN1_L to prevent current leakage of battery at standby mode. Register pull R2 to ground for battery level detection. (ADC input range is 0V~2V, therefore need to adjust R1 & R2 to make AIN1 level to 2V for fully charge battery.) 
23	19	11	VDDA_ADC	P		Analog power of ADC block 3.3V.
24	20	(SUB)	PGA_VIN	B		Analog audio input. Input level 0V~2V.
25	21	(SUB)	VSSA_ADC	P		Analog ground of ADC block.
26	22	12	RF_SPI_CS	B	4mA	RF SPI_CS / GPIO
27	23	13	RF_SPI_CLK	B	4mA	RF SPI clock
28	24	14	RF_SPI_IN	B	4mA	RF SPI input
29	25	15	RF_SPI_OUT	B	4mA	RF SPI output / GPIO
30	26	16	RF_ANT1	B	4mA	RF antenna 1 / GPIO
31	27	17	RF_ANT2	B	4mA	RF antenna 2 / GPIO
32	28	18	RF_PA	B	4mA	RF PA / GPIO
33	29	19	RF_CE	B	4mA	RF CE / GPIO
34 (SUB)	30 (SUB)	20 (SUB)	GND	P		Core & I/O ground
35	31	21	VDD3	P		3.3V I/O power
36	32	22	RF_TX_SEL	B	4mA	RF TX enable / GPIO
37	33	23	RF_TXD	B	4mA	RF TX data / GPIO
38	34	24	RF_RX_SEL	B	4mA	RF RX enable / GPIO

SN93330 LQFP-100	SN93331 LQFP-80	SN93310 LQFP-48	Pin Name	DIR	PD/U FAST	Description
39	35	25	RF_RXD	B	4mA	RF RX data
40	36		GPIO6	B	8mA	General-purpose I/O
41			GPIO12	B	8mA	General-purpose I/O
42			GPIO11	B	8mA	General-purpose I/O
43			LCD_IO24	B	4mA	LCD_IO
44			LCD_IO23	B	4mA	LCD_IO
45			LCD_IO22	B	4mA	LCD_IO
46	37		LCD_IO13 / S_SCL	B	4mA	LCD_IO / I2C SCL of sensor interface.
47	38		LCD_IO12 / S_SDA	B	4mA	LCD_IO / I2C SDA of sensor interface
48	39		LCD_IO11 / SEN_CLK	B	8mA	LCD_IO / Sensor clock of sensor interface
49	40		LCD_IO10 / IMG7	B	4mA	LCD_IO / IMG7 of sensor interface
50	41		LCD_IO9 / IMG6	B	4mA	LCD_IO / IMG6 of sensor interface
51	42		LCD_IO8 / IMG5	B	4mA	LCD_IO / IMG5 of sensor interface
52	43		LCD_IO7 / IMG4	B	4mA	LCD_IO / IMG4 of sensor interface
53	44		LCD_IO6 / IMG3	B	4mA	LCD_IO / IMG3 of sensor interface
54	45		LCD_IO5 / IMG2	B	4mA	LCD_IO / IMG2 of sensor interface
55	46		LCD_IO4 / IMG1	B	4mA	LCD_IO / IMG1 of sensor interface
56	47		LCD_IO3 / IMG0	B	4mA	LCD_IO / IMG0 of sensor interface
57	48	26	RX	B	4mA	RS232 RX
58	49	27	TX	B	4mA	RS232 TX
59	50	28	VDD18	P		1.8V core power
60 (SUB)	51 (SUB)	29 (SUB)	GND	P		Core & I/O ground
61	52	30	VDD3	P		3.3V I/O power
62	53	31	SF_CS	O	4mA	Chip select to serial flash.
63	54	32	SF_SCK	O	4mA	Clock to serial flash.
64	55	33	SF_SI	I	4mA	Data from serial flash
65	56	34	SF_SO	O	4mA	Data to serial flash
66	57		GPIO9 / DM_DATA	B	8mA	General-purpose I/O / DMIC data input
67	58		GPIO8 / DM_CLK	B	8mA	General-purpose I/O / DMIC clock output
68			LCD_IO19	B	4mA	LCD_IO
69			LCD_IO18	B	4mA	LCD_IO
70	59		LCD_IO17	B	4mA	LCD_IO
71	60	35	TEST	I	4mA	Test mode, if set high.
72	(SUB)	(SUB)	VSSA_DAC	P		AGND for video DAC
73	61	36	VDDA_DAC	P		AVDD fro video DAC
74			VDAC_REG	O		Regulator output for video DAC
75			VREF	O		REF for video DAC
76			I_OUTB	O		IOUTB for video DAC
77			I_OUT	O		IOUT for video DAC
78	62	37	XIN	I	12M	OSC input (12 MHz)
79	63	38	XOUT	B	12M	OSC output
80	64	39	RST	B	4mA, PD	Chip reset

SN93330 LQFP-100	SN93331 LQFP-80	SN93310 LQFP-48	Pin Name	DIR	PD/U FAST	Description
81	65	40	VDD3	P		3.3V I/O power
82 (SUB)	66 (SUB)	41 (SUB)	GND	P		Core & I/O ground
83	67	42	VDD18	B	8mA	General-purpose I/O
84	68		GPIO7	B	8mA	General-purpose I/O
85			LCD_IO27	B	4mA	LCD_IO
86			LCD_IO26	B	4mA	LCD_IO
87			LCD_IO25	B	4mA	LCD_IO
88	69	(SUB)	KEY	I		RC-OSC: Key input (H: 1.8V, L: 0V)
89	70		PWR_EN	O		RC-OSC: PWR_EN output (H: 1.8V, L: 0V)
90	71	43	VDD_RC	P		RC-OSC: VDD for RTC OSC (1.8V)
91	72		VCAPA	I		RC-OSC: Connect to CAP 2.5 nf
92	73		VCAPB	I		RC-OSC: Connect to CAP 2.5 nf
93	74	44	VSSA	P		GND for USB PHY, PLL and regulator
94	(SUB)	45	DN	B	12M	USB D-
95		46	DP	B	12M	USB D+
96	75	47	VDDA	P		Regulator input and power for USB PHY (3.3V)
97	76	48	VDDAL	P		Regulator output and PLL power (1.8V)
98	77	(SUB)	VGNDA1	I		Audio DAC ground
99	78	1	VDDA1	I		Audio DAC power, 3.3V
100	79		OUTR	O		Audio DAC output. Output range: 0V~VDDA1

9. Power Management Mode

	SN93300 Current consumption	Configuration			Wakeup condition		
		12MHz Crystal	Power		RC timer	KEY	GPIO
			ON	OFF			
Power down mode	Ultra low (<100uA)	OFF	VDD_RC	VDD18 VDD3 VDDA_ADC VDDA VDDA1	√	√	
Sleeping mode	Low (<300uA)	OFF	VDD_RC VDD18 VDD3	VDDA_ADC VDDA VDDA1	√	√	√
Normal mode	Normal	ON	VDD18 VDD3 VDDA_ADC VDDA VDDA1				

10. RF Transceiver Pin Mapping

Sonix SN93300	Muchip® MU2302	AMICCOM® A7121	Nordic® nRF24L01
RF_TXD, O	TX, I		

Sonix SN93300	Muchip® MU2302	AMICCOM® A7121	Nordic® nRF24L01
RF_RXD, I	DATA, O	TRXD, O	IRQ, O

Sonix SN93300	Muchip® MU2302	AMICCOM® A7121	Nordic® nRF24L01
RF_ANT1, O/I	ANT1, I	BB_CLK, O	
RF_ANT2, O	ANT2, I	CD_TXEN, I	
RF_SPI_OUT, I		SPI_TXD, O	MISO, O
RF_SPI_CLK, O	SCLK, I	SPI_CLK, I	SCK, I
RF_SPI_IN, O	SDATA, I	SPI_RXD, I	MOSI, I

Sonix SN93300	Muchip® MU2302	AMICCOM® A7121	Nordic® nRF24L01
RF_SPI_CS, O	SLE, I	SPI_CS, I	CSN, I
RF_CE, O	EN, I	MS0, I	CE, I
RF_PA, O	DEM_RST, I	MS1, I	
RF_TX_SEL, O	TX_SEL, I	TX_SEL, I	
RF_RX_SEL, O	RX_SEL, I	RX_SEL, I	

11. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
VDD3	Power Supply	-0.3 ~ 3.6	V
VDD18	Power Supply	-0.18 ~ 1.98	V
Vin	Input Voltage	-0.3 ~ VDD3 + 0.3	V
Vout	Output Voltage	-0.3 ~ VDD3 + 0.3	V

12. DC Characteristic

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDD3	Power Supply		3.0	3.3	3.6	V
VDD18	Power Supply		1.62	1.8	1.98	V
Topr	Operating Temperature		0		70	°C
Vil	Input low voltage	TTL	-0.3		0.8	V
Vih	Input high voltage	TTL	2.0		VDD3+0.3	V
Iil	Input low current	no pull-up or pull-down	-1		1	μA
Iih	Input high current	no pull-up or pull-down	-1		1	μA
Ioz	Tri-state leakage current		-1		1	μA
Vol	Output Low voltage	Iol=4mA / 8mA			0.4	V
Voh	Output high voltage	Ioh=4mA / 8mA	2.4			V
Cin	Input capacitance			10		pF
Cout	Output capacitance			10		pF
Cbid	Bi-directional buffer Capacitance			10		pF
Rpu	Pull-up resistor			70K		Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Rpd	Pull-down resistor			70K		Ω

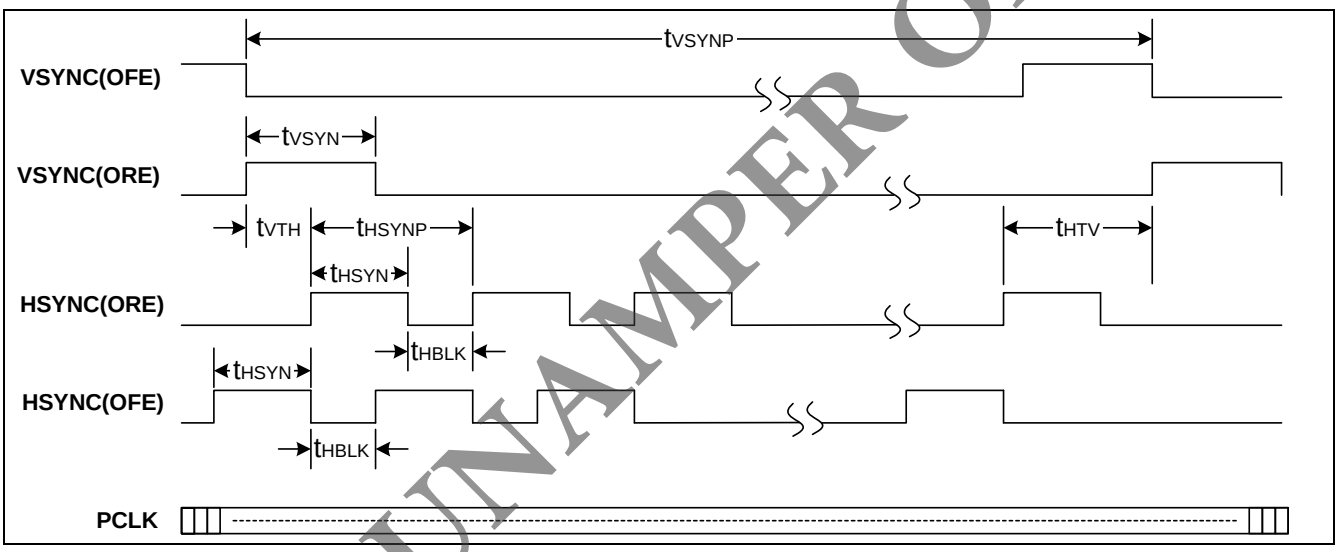
13. Timing Specifications

- Display panel interface

  SN93100 provides generic panel interface from LCD_IO0 to LCD_IO21 for most popular display panels. Timing of dedicate panel interface could be adjusted by register setting.

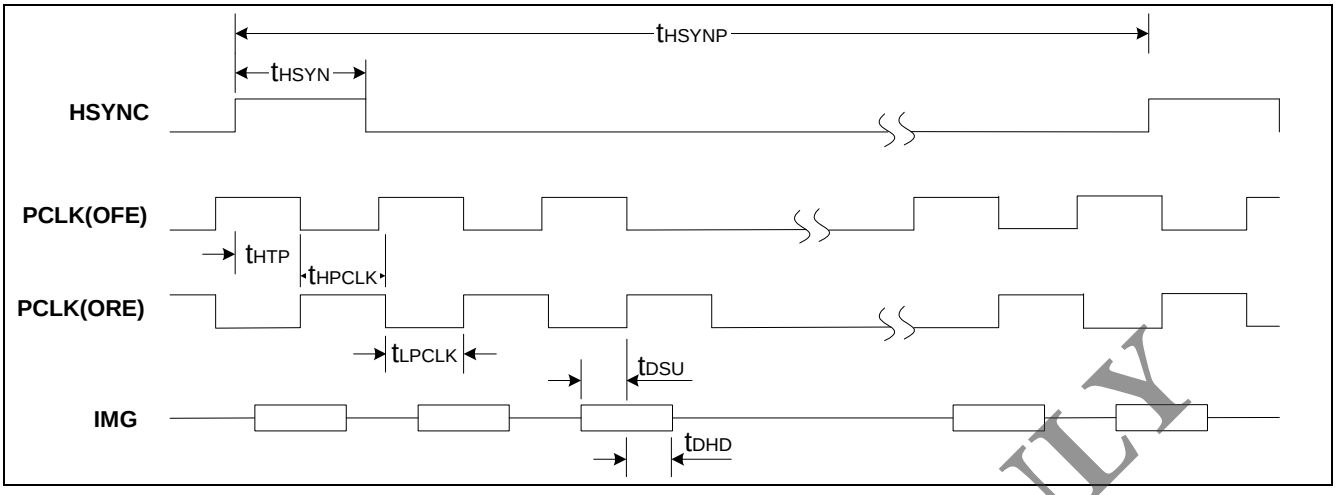
  For panel supporting information, please check with Sonix FAE.

- Sensor interface.



Parameter	Symbol	Min.	Typ.	Max.	Unit
VSYNC pulse width	t_{VSYNC}	t_{PCLK}	-	-	ns
VSYNC to HSYNC	t_{VTH}	0	-	t_{HBLK}	ns
VSYNC period	t_{VSYNP}	VSIZE * t_{HSYNP} + t_{VTH}			ns
HSYNC pulse width	t_{HSYN}	t_{PCLK}	-	-	ns
Blank time between two HSYNC	t_{HBLK}	t_{PCLK}	-	-	ns
HSYNC to VSYNC	t_{HTV}	t_{HSYNP}			ns
HSYNC period	t_{HSYNP}	HSIZE * t_{PCLK} + t_{HTP}			ns

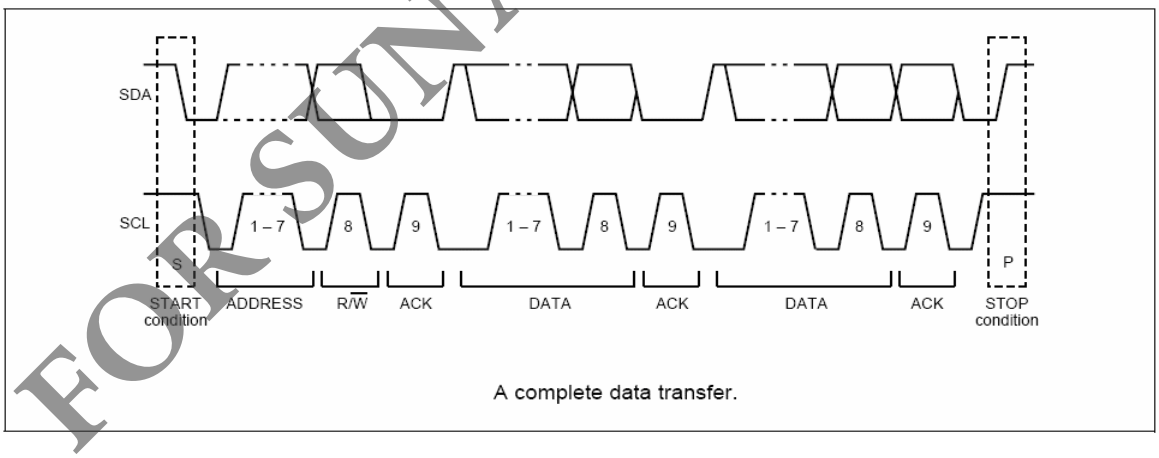
Note 1: t_{SENCK} is period of internal clock for sensor post processing.
2: HVD (High Valid), LVD (Low Valid).



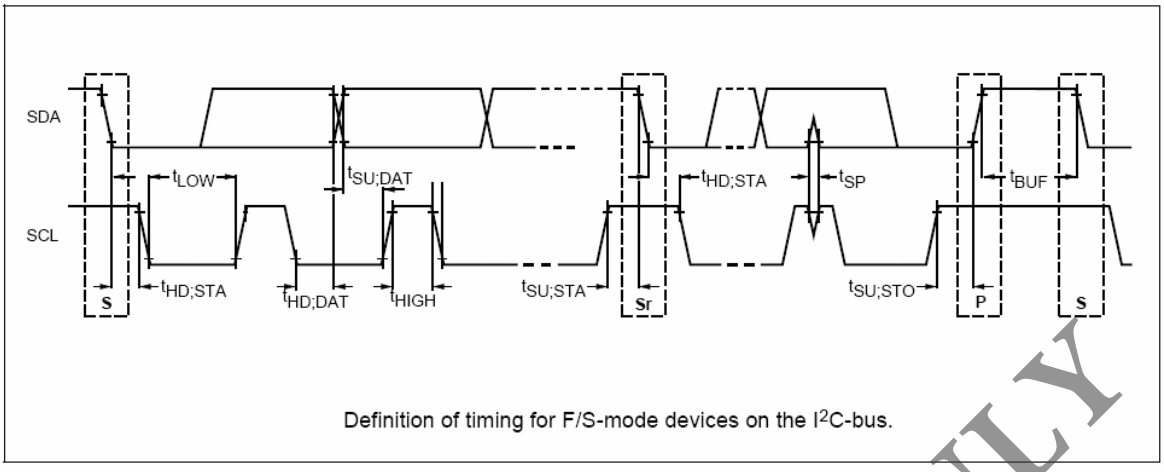
Parameter	Symbol	Min.	Typ.	Max.	Unit
HSYNC pulse width	t_{HSYN}	t_{PCLK}	-	-	ns
Frequency of pixel clock	f_{PCLK}	-	-	48	MHz
Image data setup time	t_{DSU}	2.0	-	-	ns
Image data hold time	t_{DHD}	2.0	-	-	ns
Sensor master clock	f_{SEN_CLK}	0.5	-	48	MHz

Note 1: f_{SENCK} is period of internal clock for sensor post processing.
2: ORE (On Rising Edge) means the timing act on rising edge.
OFE (On Falling Edge) means the timing act on falling edge.

■ Sensor control interface (I^2C)



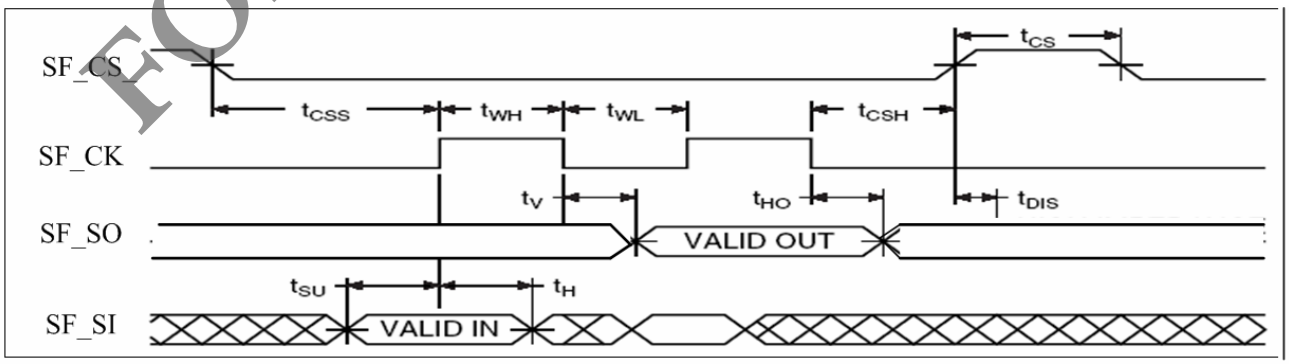
A complete data transfer.



Definition of timing for F/S-mode devices on the I^2C-bus.

Parameter	Symbol	Standard mode			Fast mode			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	-	98.7	-	-	394.7	-	kHz
Hold time START condition	$t_{HD;STA}$	-	5067	-	-	1267	-	ns
LOW period of the SCL clock	t_{LOW}	-	5067	-	-	1267	-	ns
HIGH period of the SCL clock	$t_{HD;STA}$	-	5067	-	-	1267	-	ns
Setup time for a repeated START condition	$t_{SU;STA}$	-	5067	-	-	1267	-	ns
Data hold time: Write	$t_{HD:DAT}$	-	2533	-	-	633	-	ns
Data hold time: Read	$t_{HD:DAT}$	10	-	-	10	-	-	ns
Data setup time: Write	$t_{SU:DAT}$	-	2533	-	-	633	-	ns
Data setup time: Read	$t_{SU:DAT}$	10	-	-	10	-	-	ns
Setup time for STOP condition	$t_{SU:STO}$	-	5066	-	-	1267	-	ns
Bus free time between a STOP and START condition	t_{BUF}	4.8	-	-	1.4	-	-	us

■ Serial flash interface



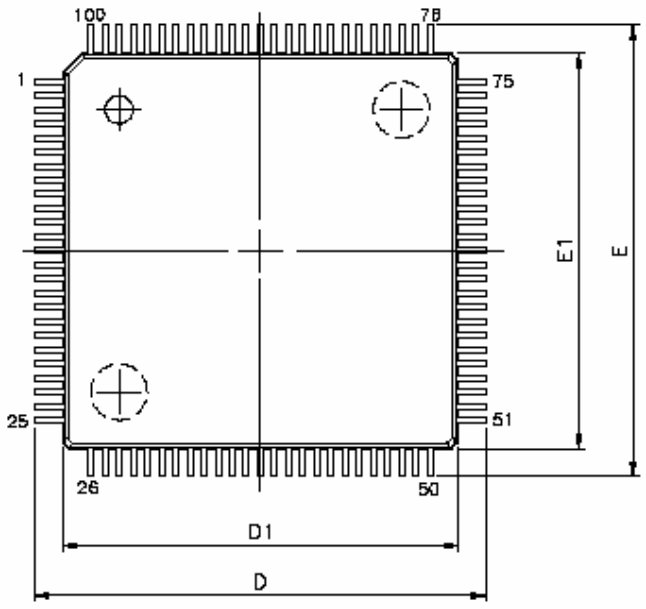
↳ When f_{SCK} = 24 Mhz (SPEED=1)

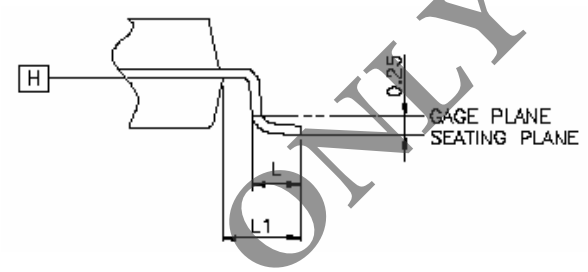
Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	-	24	-	MHz
Chip Select low to SF_CK Edge	t_{CSS}	36		-	ns
SF_CK Edge to Chip Select High	t_{CSH}	36		-	ns
Chip High period	t_{CS}	41.67		-	ns
Clock high period	t_{WH}	20.83	-	-	ns
Clock low period	t_{WL}	20.83	-	-	ns
Input Data setup time	t_{SU}	10	-	-	ns
Input Data hold time	t_H	10	-	-	ns
Output Data Valid time @ CL=20pF	t_V	-	-	5	ns
Output Data Hold time @ CL=20pF	t_{HO}	36	-	-	ns

↳ When f_{SCK} = 12 Mhz (SPEED=3)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	-	12	-	MHz
Chip Select low to SF_CK Edge	t_{CSS}	36	-	-	ns
SF_CK Edge to Chip Select High	t_{CSH}	36	-	-	ns
Chip High period	t_{CS}	41.67	-	-	ns
Clock high period	t_{WH}	41.67	-	-	ns
Clock low period	t_{WL}	41.67	-	-	ns
Input Data setup time	t_{SU}	10	-	-	ns
Input Data hold time	t_H	10	-	-	ns
Output Data Valid time @ CL=20pF	t_V	-	-	5	ns
Output Data Hold time @ CL=20pF	t_{HO}	78	-	-	ns

14. Package Outline

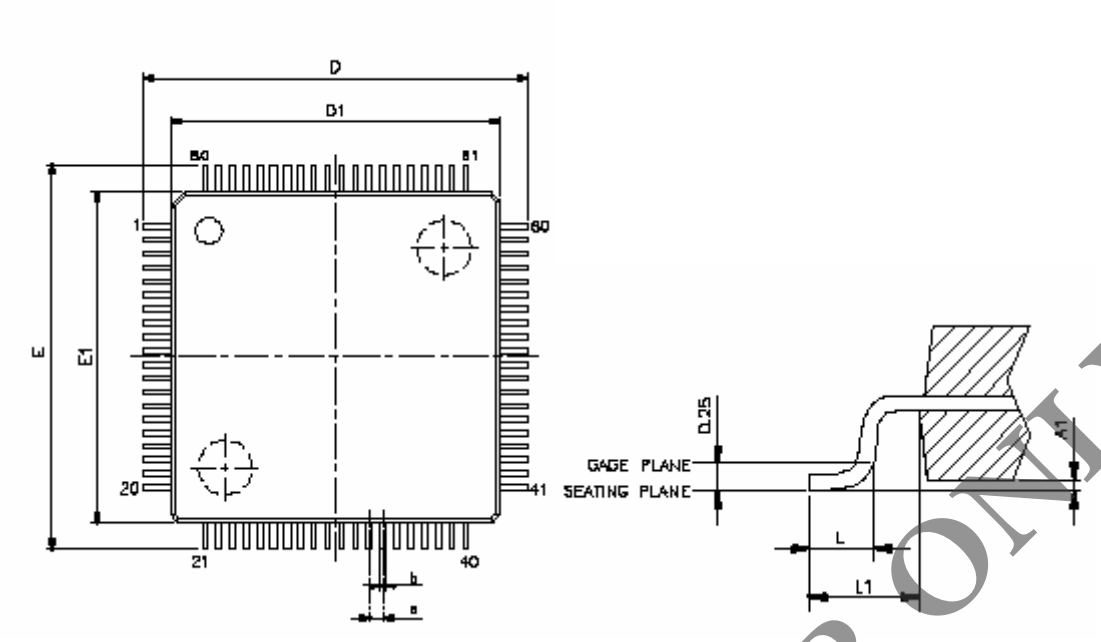


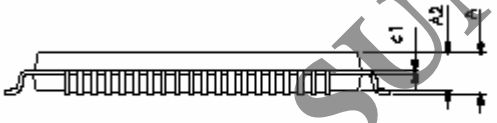


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	0.127	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		

Package Outline LQFP-100 (14X14)

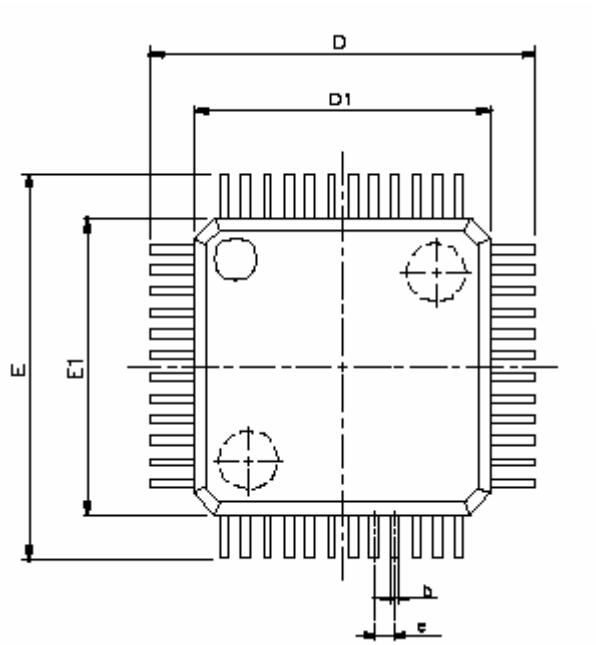


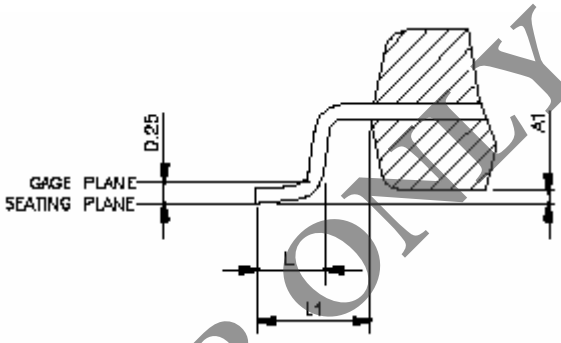


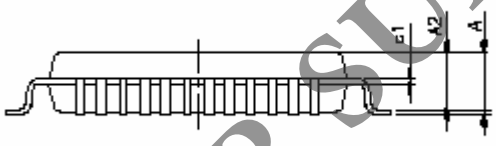
VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	—	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	12 BSC	
D1	10 BSC	
E	12 BSC	
E1	10 BSC	
e	0.4 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

Package Outline LQFP-80 (10X10)







VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

Package Outline LQFP-48 (7X7)

15. Liability Disclaimer

Sonix Technology reserves the right to make changes without further notice to the product to improve reliability, function or design. Sonix Technology does not assume any liability arising out of the application or use of any product or circuits described herein.

All application information is advisory and does not form part of the specification.

16. Update Information

V1.1 Update pin order, add one more pin for VDD18, remove GPIO13.