USB 2.0 Video
PC Camera Controller
SN9C258C
Datasheet

Released Version: v1.00

Revision	Date	Description	Adult
1.00	2008-04-30	Initial draft	Ocean
Apply to		SN9C258C	

Table of Contents

1 General Description

SN9C258C is a USB 2.0 High-Speed (HS) and Full-Speed (FS) compatible PC Camera controller. The built-in extreme low-power transceiver provides the superior compatibility with various USB host and the best quality for image applications. It is fully compliant with USB Video. With the integrated sensor interface and color processing engine, it can support most available VGA CMOS ISP sensors. The high performance Motion-JPEG compression engine makes variant compression ratio to satisfy bandwidth requirement which output MJPG data format and reach 30fps or higher at VGA on both HS and FS.

SN9C258C is controlled by the embedded micro-controller, and the statistics for Auto Exposure and Auto White Balance are built-in. The flexible architecture is consisted of mask ROM, internal RAM and external serial-flash which can store the customized codes and parameters. It's also possible to store all the program code in the external flash memory for special design purpose. With the highly-integrated firmware architecture and the developing kit provided by SONiX, it's easy for 3rd party to fulfill any specific feature.

2 Features

2.1 System

- 3.3V single power supply, 1.8V Core (generated by internal regulator) and 3.3V I/O
- Extreme low power consumption, < 43mA when standby and < 400uA when suspend (Power consumption of sensor is not included)
- Built-in PLL for internal clock generation with input crystal frequency of 12MHz
- Using external serial flash to store customized code and data
- No external RAM needed

2.2 USB Controller

- USB 2.0 high-speed and full-speed compatible
- USB Video Class 1.1 compliant
- USB2.0 HS/FS auto sense and switch
- USB FS mode and USB disconnection are programmable
- 4 endpoints: CONTROL pipe, Interrupt IN and 2 Isochronous-IN (Video Out and Audio Out)
- 6 alternate settings for Video Streaming Interface

2.3 Sensor Interface

- Support VGA CMOS ISP sensor
- Support YUY2 and RAW (Bayer-Pattern) image data format from sensor
- Output clock: Programmable output clock on variant options, 48/30/28/27/26/25/24Mhz
- Input clock: Maximum acceptable Pixel Clock is 30Mhz
- Support industrial standard 2-wire serial interface for sensor control

2.4 Image Processing (Bayer)

- Input windowing
- Static defect-pixel correction (127 dots, stored in serial flash)
- On-the fly defect-pixel concealment
- Lens shading compensation for R/G/B channel
- Individual digital color gain control for R/Gb/Gr/B channel
- Pixel offset (optical black) compensation for R/Gb/Gr/B channel
- Programmable gamma table for R/G/B channel
- Configurable noise reduction
- Configurable edge enhancement

2.5 Color processing

- AE window statistics
- AWB window statistics
- Individual digital color gain control for Y/Cb/Cr channel
- Programmable color correction matrix (RGB to YUV)
- Programmable gamma table for Y channel
- Configurable windowing function after processed image

2.6 Scaling Engine

- 1/2, 1/4 smooth scaling on Y/Cb/Cr
- 3/5, 4/5 bilinear scaling on Y/Cb/Cr

2.7 JPEG Encoder

- JPEG YUV422 baseline format
- Built-in JPEG encoder support USB Video Class MJPEG payload
- 128 bytes quantization tables for Y and C provide programmable compression ratio
- The JPEG encoder is capable of compressing VGA video at 45fps.

2.8 Video / Still Image

- Output video / still image format:
  - USB Video Class Uncompressed YUY2 payload (16bits/pixel)
  - USB Video Class MJPG payload
- Still Image capturing support UVC still image capture method 0/1/2

2.9 Frame rate

- Frame rate considering USB bandwidth limitation

Full-speed mode					
Output format	VGA	CIF	QVGA	QCIF	QQVGA
YUY2	1.5fps	4.5fps	6.5fps	19.5fps	26fps
MJPEG	30fps	30fps	30fps	30fps	30fps

High-speed mode					
Output format	VGA	CIF	QVGA	QCIF	QQVGA
YUY2	30fps	30fps	60fps	60fps	60fps
MJPEG	45fps	60fps	60fps	60fps	60fps

- Frame rate considering sensor characteristic

The maximum frame rate is limited by how many fps that sensor can output under acceptable maximum pixel clock

2.10 Audio

- Build-In one channel Cyclic ADC
- Programmable audio sampling frequency: 8, 16, 24 and 48 kHz
- Audio bit resolution is 16 bits/stereo

2.11 GPIO

- Maximum 3 GPIO available
- GPIO action is able to link to the built-in HID class

2.12 Micro Controller and USB Device Features

- Built-in 8032 micro controller with 3K bytes data memory, and maximum CPU clock rate is 24MHz
- Total 64K bytes code memory include 48K bytes mask ROM and 16K bytes SRAM
- Load extended 16KB F/W from external serial flash.
- Load VID/PID, manufacturer, product and serial number string from external serial flash.
- Load UVC parameter definition from external serial flash.
- F/W is upgradeable from PC
- Force USB at FS mode/ Force USB disconnect
- Interrupt at the end of H/W windowing
- CPU watch dog
- Abnormal voltage self-protection

2.13 Pre-Defined for USB Video Class

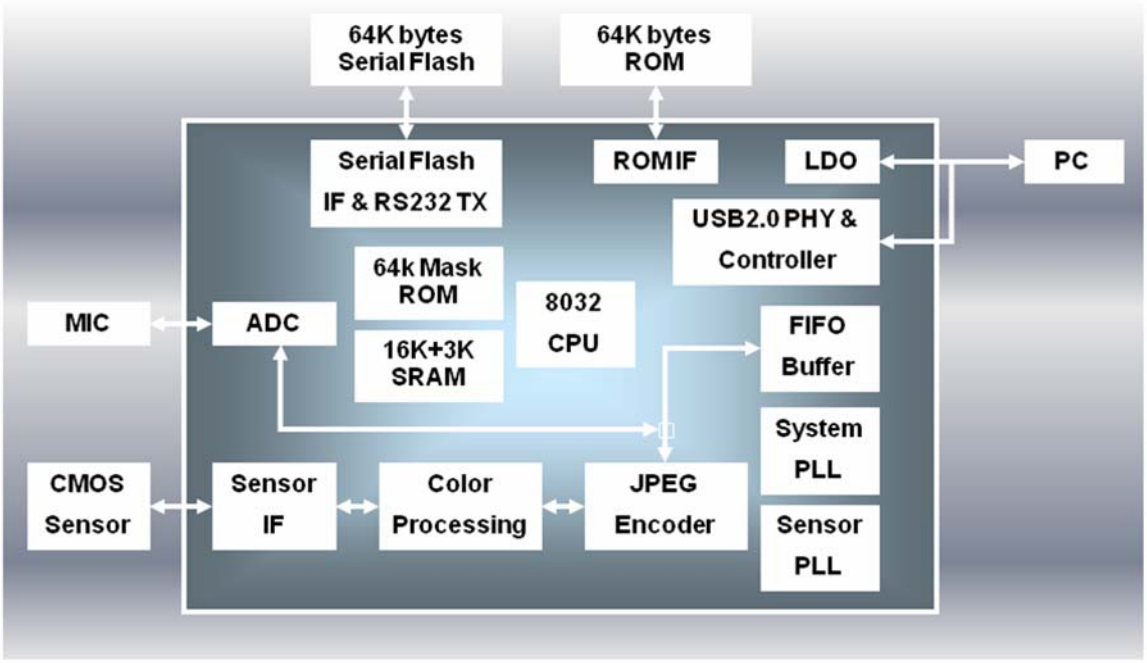
- Brightness control (UVC defined)
- Contrast control (UVC defined)
- Hue control (UVC defined)
- Saturation control (UVC defined)
- Sharpness control (UVC defined)
- Gamma control (UVC defined)
- Privacy control (UVC defined)
- Image auto-flip control triggered by GPIO
- LED indicator on video streaming
- Extension unit support

2.14 Platform Support

- Microsoft Windows XP 32bit SP2, Microsoft Windows XP 64bit, Microsoft Windows Vista 32bit, Microsoft Windows Vista 64bit
- Mac - OS X 10.4.8 or later
- Linux with UVC driver (open source available at http://linux-uvc.berlios.de/)

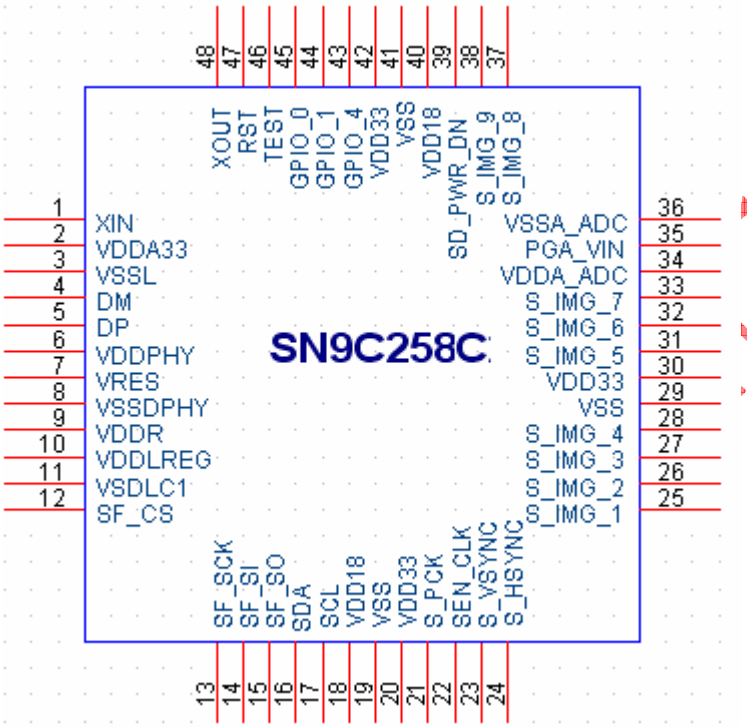
3 Function Block Diagram

3.1 Block Diagram



4 Pin Assignment

4.1 Pin-out Diagram



4.2 Pin Description

PIN# (SN9C258C)	PIN NAME	DIR	Description
1	XIN	I	OSC input (Rf=1M) (12MHz)
2	VDDA33	P	3.3v digital PWR for PLL/USB receiver
3	VSSL	P	Digital GND for PLL/USB receiver
4	DM	A	D- for USB
5	DP	A	D+ for USB
6	VDDPHY	P	3.3v analog PWR for USB driver
7	VRES	A	Reference for USB driver(2.4K to GND)
8	VSSDPHY	P	Digital GND for USB driver
9	VDDR	P	3.3v digital PWR for USB driver

10	VDDLREG	P	1.8V regulator output
11	VSDLC1	P	GND for PHY digital logic
12	SF_CS	OH	Serial flash chip select
13	SF_SCK	OL	Serial flash clock
14	SF_SI	I	Data from serial flash
15	SF_SO	OL	Data to serial flash
16	SDA	I	SDA for I2C interface (data)
17	SCL	OU	SCL for I2C interface (clock)
18	VDD18	P	core VDD 1.8
19	VSS	P	Ground
20	VDD33	P	IO power 3.3v
21	S_PCK	I	Sensor pixel clock
22	SEN_CLK	O	Sensor clock
23	S_VSYNC	I	Sensor VSYNC
24	S_HSYNC	I	Sensor HSYNC
25	S_IMG_1	I	Sensor image data
26	S_IMG_2	I	Sensor image data
27	S_IMG_3	I	Sensor image data
28	S_IMG_4	I	Sensor image data
29	VSS	P	Ground
30	VDD33	P	VDD IO 3.3v
31	S_IMG_5	I	Sensor image data
32	S_IMG_6	I	Sensor image data
33	S_IMG_7	I	Sensor image data
34	VDDA_ADC	I	Analog power of ADC block 3.3V.
35	PGA_VIN	I	PGA input.
36	VSSA_ADC	P	Analog ground of ADC block.
37	S_IMG_8	I	Sensor image data
38	S_IMG_9	I	Sensor image data
39	SD_PWR_DN	I	Sensor power down
40	VDD18	P	core VDD 1.8
41	VSS	P	Ground
42	VDD33	P	IO power 3.3v
43	GPIO_4	I	General purpose I/O
44	GPIO_1	I	General purpose I/O
45	GPIO_0	I	General purpose I/O

46	TEST	I	Test mode
47	RST	I	Chip reset
48	XOUT	O	OSC output (Rf=1M)

5 Electrical Characteristics

5.1 DC operating Condition

5.1.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
VDD33	Power Supply	-0.3 ~ 3.6	V
VDD18	Power Supply	-0.18 ~ 1.98	V
Vin	Input Voltage	-0.3 ~ VDD33 + 0.3	V
Vout	Output Voltage	-0.3 ~ VDD33 + 0.3	V

5.1.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
VDD33	Power Supply	3.0	3.3	3.6	V
VDD18	Power Supply	1.62	1.8	1.98	V
Vin	Input voltage	0		VDD33	V
Topr	Operating Temperature	0		70	°C

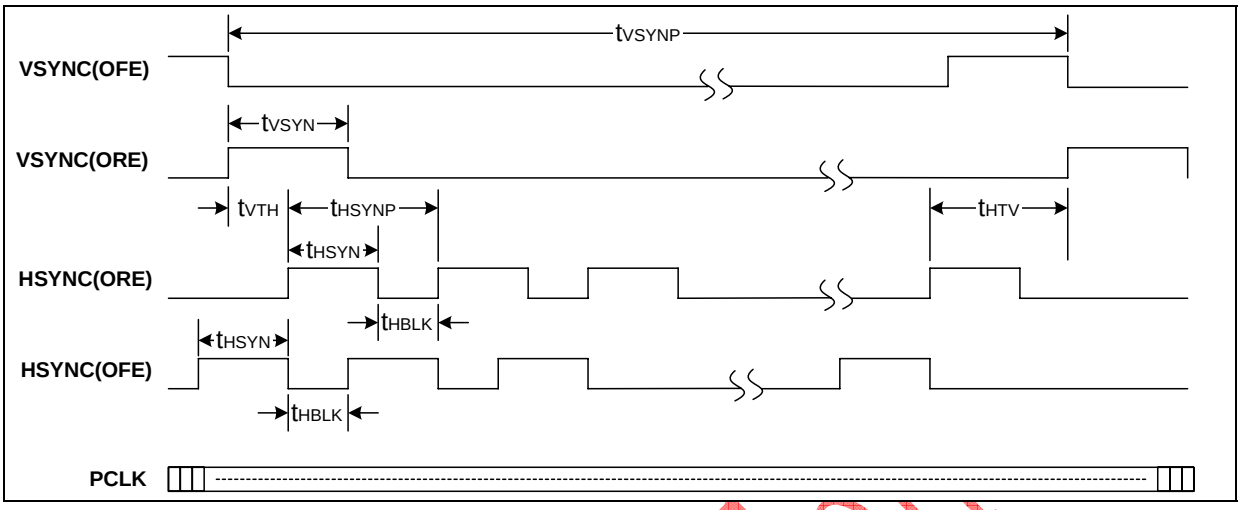
5.1.3 DC Electrical Characteristics

(Under Recommended Operating Conditions and VDD33=3.0 ~ 3.6V, Tj=0 to +70 °C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vil	Input low voltage	TTL	-0.3		0.8	V
Vih	Input high voltage	TTL	2.0		VDD33+0.3	V
Iil	Input low current	no pull-up or pull-down	-1		1	μA
Iih	Input high current	no pull-up or pull-down	-1		1	μA
Ioz	Tri-state leakage current		-1		1	μA
Vol	Output Low voltage	Iol=4mA / 8mA			0.4	V
Voh	Output high voltage	Ioh=4mA / 8mA	2.4			V
Cin	Input capacitance			10		pF
Cout	Output capacitance			10		pF
Cbid	Bi-directional buffer Capacitance			10		pF
Rpu	Pull-up resistor			70K		Ω
Rpd	Pull-down resistor			70K		Ω

5.2 AC operating Condition

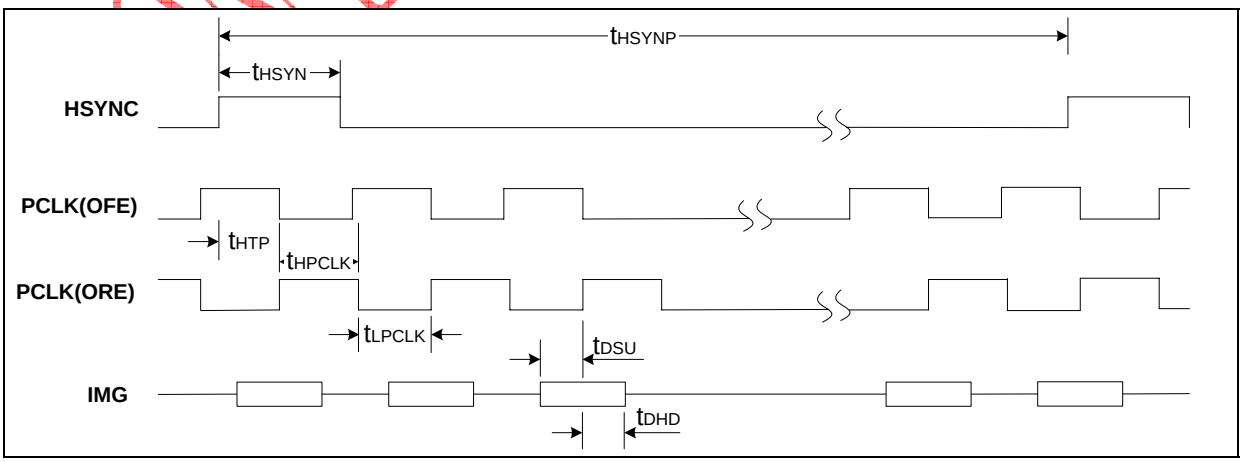
5.2.1 Sensor Interface



Parameter	Symbol	Min.	Typ.	Max.	Unit
VSYNC pulse width	t_{VSYNC}	t_{SENCK}	-	-	ns
VSYNC to HSYNC	t_{VTH}	t_{SENCK}	-	-	ns
VSYNC period	t_{VSYNP}	VSIZE * t_{HSYN} + t_{VTH}			ns
HSYNC pulse width	t_{HSYN}	t_{SENCK}	-	-	ns
Blank time between two HSYNC	t_{HBLK}	t_{SENCK}	-	-	ns
HSYNC to VSYNC	t_{HTV}	t_{HSYNP}			ns
HSYNC period	t_{HSYNP}	HSIZE * t_{PCLK} + t_{HTP}			ns

Note:

1. t_{SENCK} is period of internal clock for sensor post processing
2. ORE (On Rising Edge) means the timing act on rising edge
3. OFE (On Falling Edge) means the timing act on falling edge

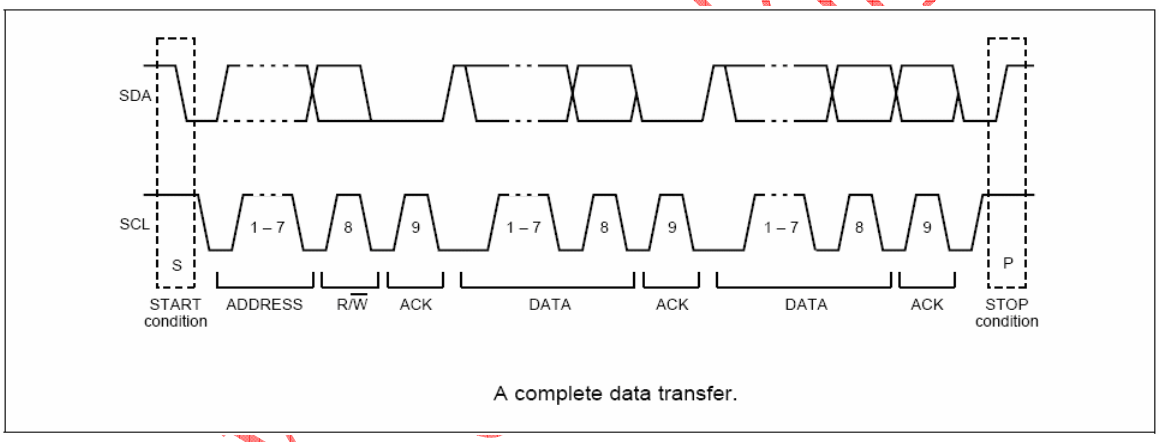


Parameter	Symbol	Min.	Typ.	Max.	Unit
HSYNC pulse width	t_{HSYN}	t_{SENCK}	-	-	ns
HSYNC to 1st valid PCLK	t_{HTP}	t_{SENCK}	-	-	ns
High period of pixel clock	t_{HPCLK}	t_{SENCK}	-	-	ns
Low period of pixel clock	t_{LPCLK}	t_{SENCK}	-	-	ns
Image data setup time	t_{DSU}	0.52	0.70	-	ns
Image data hold time	t_{DHD}	0.48	0.66	-	ns

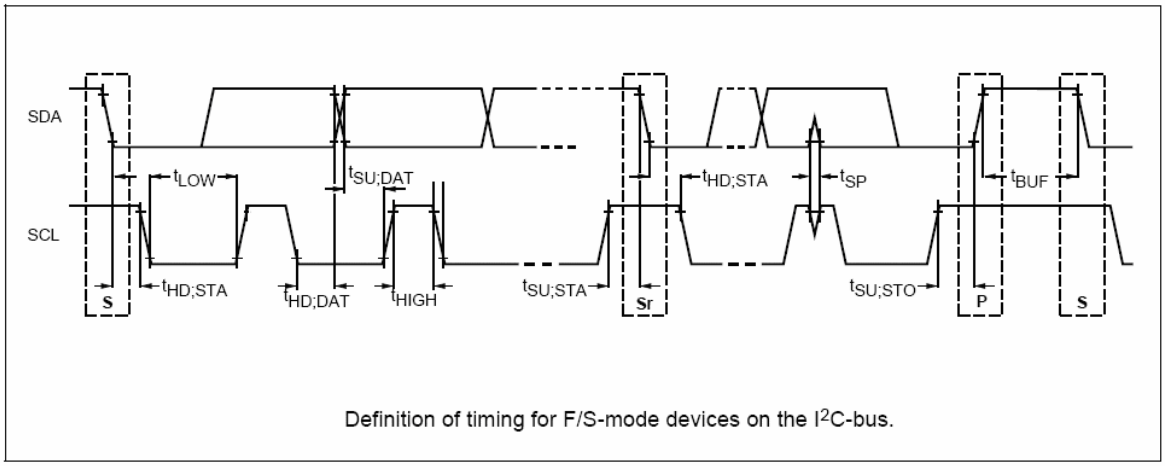
Note:

1. t_{SENCK} is period of internal clock for sensor post processing
2. ORE (On Rising Edge) means the timing act on rising edge
3. OFE (On Falling Edge) means the timing act on falling edge

5.2.2 Sensor Control Interface



A complete data transfer.

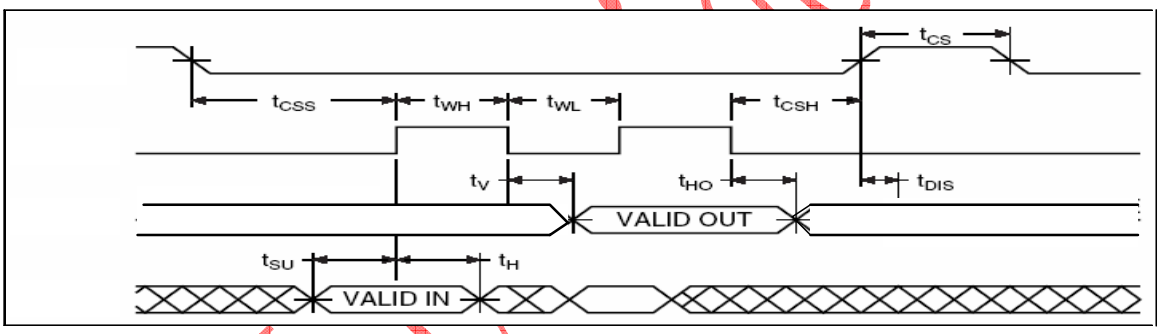


Definition of timing for F/S-mode devices on the I^2C-bus.

Parameter	Symbol	Standard mode			Fast mode			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	

SCL clock frequency	f_{SCL}	-	98.7	-	-	394.7	-	kHz
Hold time START condition	$t_{HD;STA}$	-	5067	-	-	1267	-	ns
LOW period of the SCL clock	t_{LOW}	-	5067	-	-	1267	-	ns
HIGH period of the SCL clock	$t_{HD;STA}$	-	5067	-	-	1267	-	ns
Setup time for a repeated START condition	$t_{SU;STA}$	-	5067	-	-	1267	-	ns
Data hold time: Write Data hold time: Read	$t_{HD:DAT}$ $t_{HD:DAT}$	- 10	2533 -	- -	- 10	633 -	- -	ns ns
Data setup time: Write Data setup time: Read	$t_{SU:DAT}$ $t_{SU:DAT}$	- 10	2533 -	- -	- 10	633 -	- -	ns ns
Setup time for STOP condition	$t_{SU:STO}$	-	5066	-	-	1267	-	ns
Bus free time between a STOP and START condition	t_{BUF}	4.8	-	-	1.4	-	-	us

5.2.3 Serial Flash Interface



When f_{SCK} = 24 Mhz (SPEED=1)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	-	24	-	MHz
Chip Select low to SF_CK Edge	t_{CSS}	36		-	ns
SF_CK Edge to Chip Select High	t_{CSH}	36		-	ns
Chip High period	t_{CS}	41.67		-	ns
Clock high period	t_{WH}	20.83	-	-	ns
Clock low period	t_{WL}	20.83	-	-	ns
Input Data setup time	t_{SU}	10	-	-	ns
Input Data hold time	t_H	10	-	-	ns
Output Data Valid time @ CL=20pF	t_V	-	-	5	ns
Output Data Hold time @ CL=20pF	t_{HO}	36	-	-	ns

When f_{SCK} = 12 Mhz (SPEED=3)

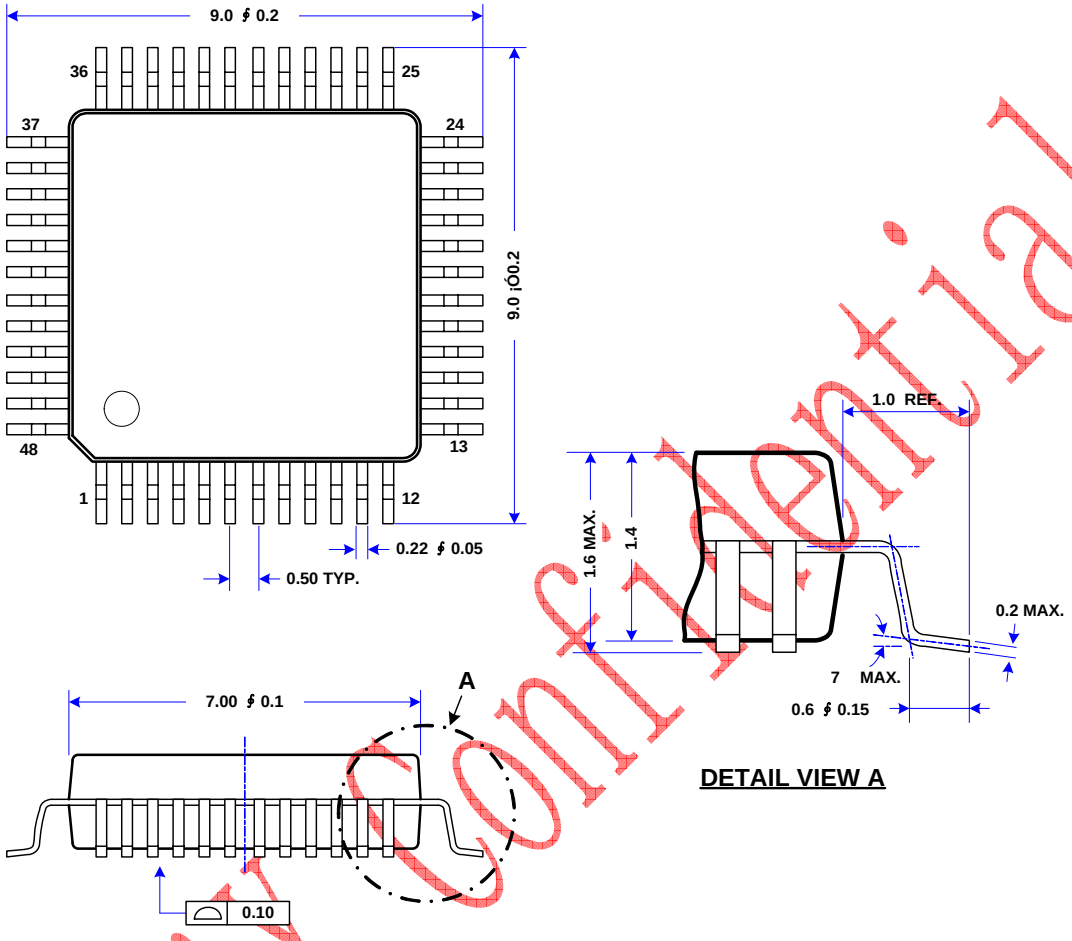
SF_CS

SF_CK

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	-	12	-	MHz
Chip Select low to SF_CK Edge	t_{CSS}	36	-	-	ns
SF_CK Edge to Chip Select High	t_{CSH}	36	-	-	ns
Chip High period	t_{CS}	41.67	-	-	ns
Clock high period	t_{WH}	41.67	-	-	ns
Clock low period	t_{WL}	41.67	-	-	ns
Input Data setup time	t_{SU}	10	-	-	ns
Input Data hold time	t_H	10	-	-	ns
Output Data Valid time @ CL=20pF	t_V	-	-	5	ns
Output Data Hold time @ CL=20pF	t_{HO}	78	-	-	ns

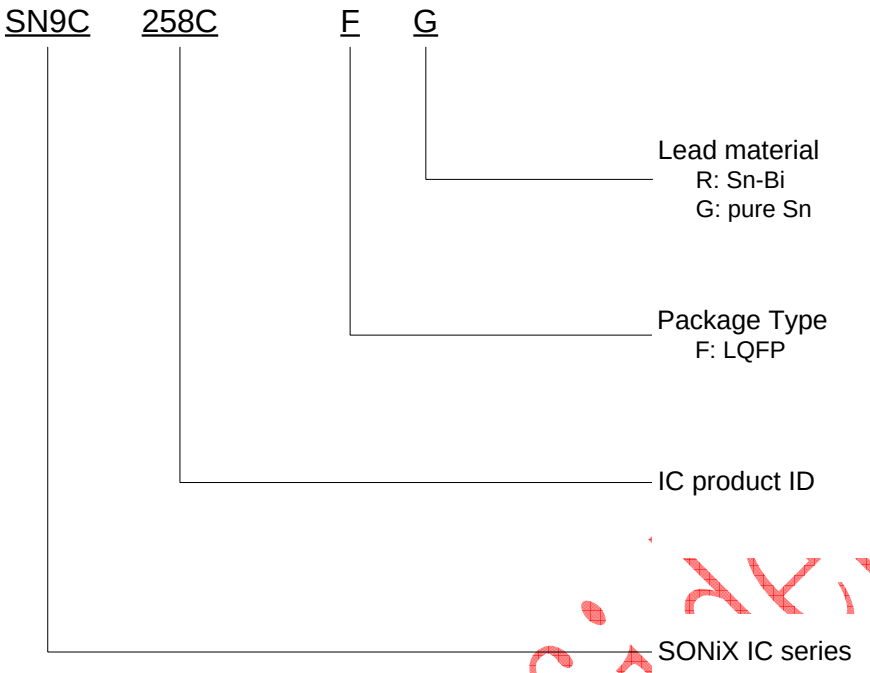
6 Package Dimensions

6.1 48 pin LQFP



(All dimensions are in Millimeters)

6.2 Nomenclature



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