



===== **CONTENTS** =====

| | |
|--|----------|
| 1. INTRODUCTION..... | 3 |
| 2. FEATURES | 3 |
| 3. PIN ASSIGNMENT | 4 |
| 4. BLOCK DIAGRAM | 4 |
| 5. FUNCTION DESCRIPTIONS | 5 |
| 5.1 OSCILLATOR | 5 |
| 5.2 ROM | 5 |
| 5.3 RAM | 5 |
| 5.4 POWER DOWN MODE..... | 5 |
| 5.5 SAMPLING RATE COUNTER | 5 |
| 5.6 I/O PORTS | 6 |
| 5.7 IR FUNCTION | 6 |
| 5.8 PWM IO CONTROL | 6 |
| 5.9 WATCH DOG TIMER..... | 6 |
| 5.10 PUSH-PULL OUTPUT | 7 |
| 5.11 MARK REGISTER | 7 |
| 5.12 LOW VOLTAGE HOLD | 7 |
| 6. ABSOLUTE MAXIMUM RATING | 8 |
| 7. ELECTRICAL CHARACTERISTICS | 8 |
| 8. APPLICATION CIRCUIT | 9 |



AMENDENT HISTORY

| Version | Date | Description |
|----------------|-------------------|--------------------|
| Ver 1.0 | November 08, 2006 | First issue |

1. INTRODUCTION

SNC21085 is a one-channel voice synthesizer IC with Push-Pull direct drive circuit. It built in a 4-bit tiny controller with three 4-bit I/O ports. By programming through the tiny controller in SNC21085, user's varied applications including voice section combination, key trigger arrangement, output control, and other logic functions can be easily implemented.

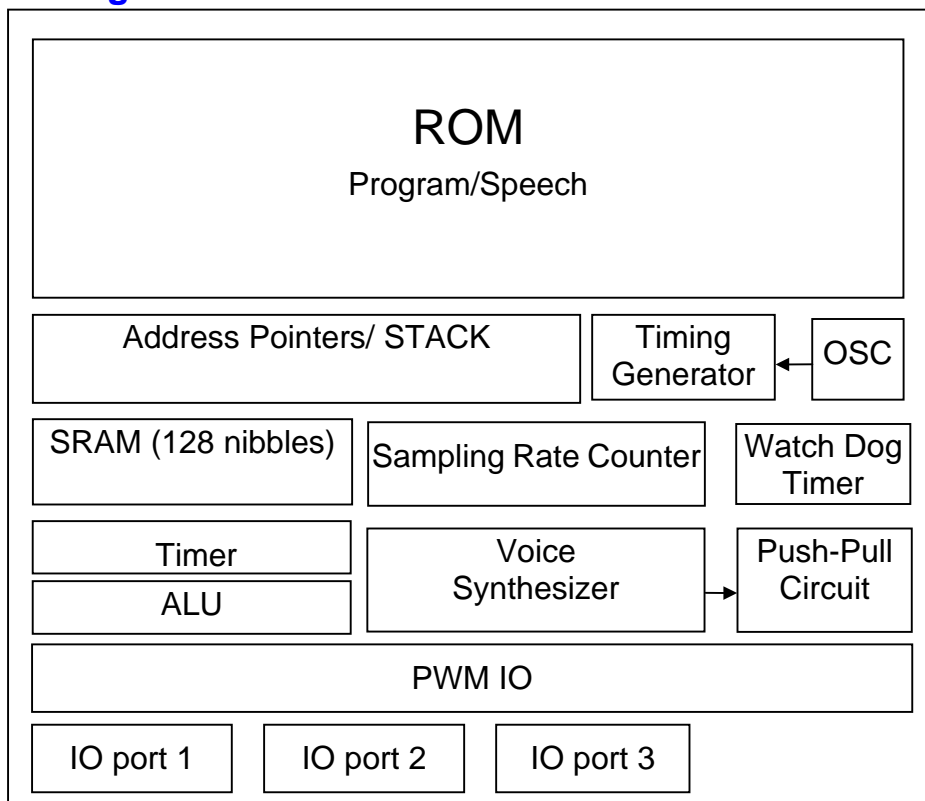
2. FEATURES

- ◆ Single power supply 2.4V – 5.5V
- ◆ System Clock is 2MHz, the instruction cycle is 4us
- ◆ 85 seconds voice capacity are provided (@6KHZ sample rate)
- ◆ Built in a 4-bit tiny controller
- ◆ I/O Port
 - Three 4-bit I/O ports P1, P2 and P3 are provided
 - The driving/sink current of P3.2 & P3.3 is up to 8mA/16mA
 - The IO pins P3.3 or P2.3 can be modulated with 38.5Khz carry signal to implement IR function.
 - PWM output for IO (P3.0~P3.3)
- ◆ 128*4 bits RAM are provided
- ◆ Maximum 16k program ROM is provided
- ◆ 256K*10 shared ROM for voice data and program
- ◆ Readable ROM code data
- ◆ Built-in one channel High Quality speech synthesizer
- ◆ Adaptive playing speed from 2.5k-20kHz is provided
- ◆ Automatic repetition
- ◆ Support 5-bit ADPCM and 10 bit PCM format
- ◆ Built in an 8-level volume control Push-Pull Direct Drive circuit output, can directly connected to Speaker for sound output
- ◆ Push-Pull DAC with 12 bits resolution (Direct Drive)
- ◆ Event Mark function supported
- ◆ Low-Voltage Detect circuit
- ◆ Watch Dog Timer Reset function.

3. PIN ASSIGNMENT

| Symbol | I/O | Function Description |
|---------|-----|--------------------------------------|
| P10~P13 | I/O | I/O port 1: IO |
| P20~P23 | I/O | I/O port 2: IO |
| P30~P33 | I/O | I/O port 3: IO |
| RST | I | Reset Chip (Active H) |
| TEST | I | Test pin |
| FUSEPAD | I | Fuse mode selection pad |
| OSC | I | The test mode clock input pad or OSC |
| RCSEL | I | Ring OSC R selection |
| DAON | O | Push-Pull output 1 |
| DAOP | O | Push-Pull output 2 |
| VDD | P | Positive power supply |
| GND | P | Negative power supply |

4. Block Diagram





5. FUNCTION DESCRIPTIONS

5.1 Oscillator

System clock define 2 Mhz, the souce provided by internal R-type ring oscillator or external resistor ring oscillator. This option is controlled by pin, RCSEL.

RCSEL = 1 using the external R 180Kohm

RCSEL = 0 using the internal R

5.2 ROM

SNC21085 contains a substantial maximum 256K words (10-bit) internal ROM, which is shared by program and resource data. Program, voice and data are shared within this same 256K words ROM.

5.3 RAM

SNC21085 contains maximum 128 nibble RAM (128 x 4-bits). The 128 nibble RAM is divided into eight pages (page 0 to page 7, 16 nibble RAM on each page). In our programming structure, users can use the instructions, PAGE n (n=0 to 7) to switch and indicate the RAM page. Besides, users can use direct mode, M0 ~ M15 in the data transfer type instructions, to access all 16 nibbles of each page.

5.4 Power Down Mode

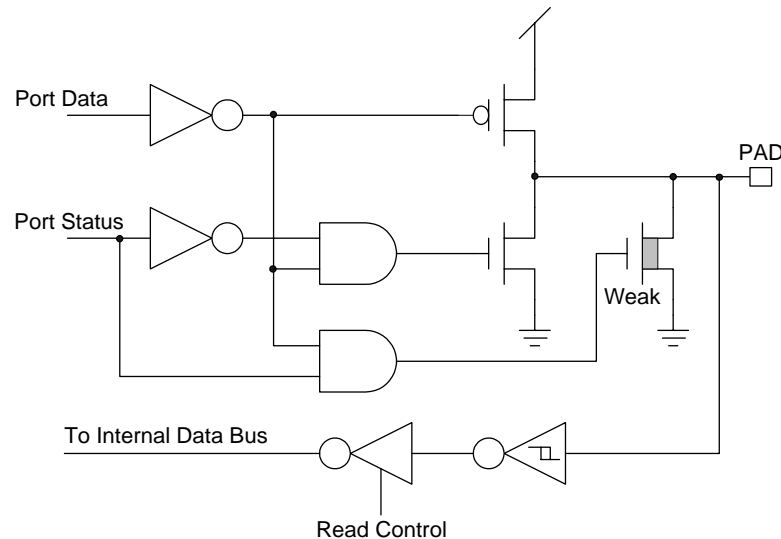
“End” instruction makes the IC entering into Stop Mode will stop the system clock for power savings (<3uA @VDD=3V and <6uA @VDD=4.5V.) Any valid data transition (L→H or H→L) occurring on any IO pin can be used to start the system clock and return to normal operating mode.

5.5 Sampling Rate Counter

The unique sampling rate counter is designed in voice channel to be able to play diverse voices at different sample playing rates. The playing rate can be adaptively set up among from the wide ranges of 2.5KHz to 20KHz. This architecture yields a high-quality voice synthesis that sounds very close to its original source when played through the same amplifier and speaker circuitry.

5.6 I/O Ports

There are three 4-bit I/O ports P1, P2 and P3. Any I/O can be individually programmed as either input pull low or output. Any valid data transition (H→L or L→H) of P1, P2 and P3 can reactivate the chip when it is in power-down stage.



I/O Port Configuration

Note:

- (1) **Weak N-MOS can serve as pull-low resistor.**
- (2) **The driving/sink current of P3.3 & P3.2 is up to 8mA/16mA**

5.7 IR Function

Bit 3 of Mode Register is applied to control the IR function. P33 can be modulated with 38.5KHz square wave before sent out to P3.3 or P2.3 pin. P3.3 and P2.3 out is controlled by Mode1.1. If Mode1.1 set 1 IR is use P2.3, set "0" is use P3.3. The IR signal can be achieved by this modulated signal.

5.8 PWM IO control

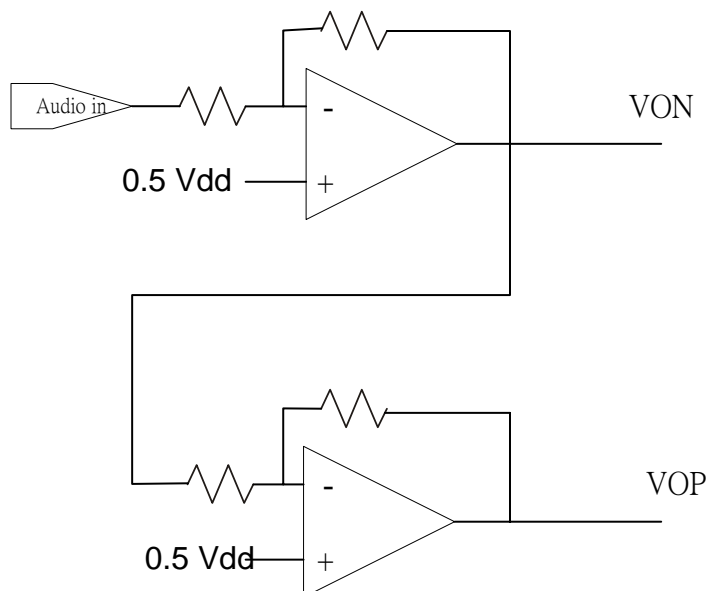
SNC21085 have support 4 PWM IO (P30~P33). Each I/O has 8 bits independent duty register.

5.9 Watch Dog Timer

SNC21085 built an internal WDT (Watch Dog Timer). This Watchdog timer would issue resets signal to this chip if it is not cleared before reaching terminal count (1sec). The watchdog timer is enabled at reset and cannot be disabled.

5.10 Push-Pull Output

An 8-level volume control Push-Pull Direct Drive circuit is built-in SNC21085. The maximum resolution of Push-Pull is 12 bits. Two huge output stage circuits are designed in SNC21085. With this advanced circuit, the chip is capable of driving speaker directly without external transistors.



Push-Pull Output

5.11 Mark register

If user had insert Mark into wave file. The Mark data will be fetched into this register during voice playing. The content of this register will be cleared to "0" automatically once user accesses this register.

5.12 Low Voltage Hold

This function enables chips entering Hold mode when voltage is below 2.1V and will back to work after voltage rise up to 2.1V. Chip will not entering hold mode before current Instruction finish. When chip in Hold mod, ROSC will keep running, and all the content of Latch/Register/SRAM will keep unchanged.

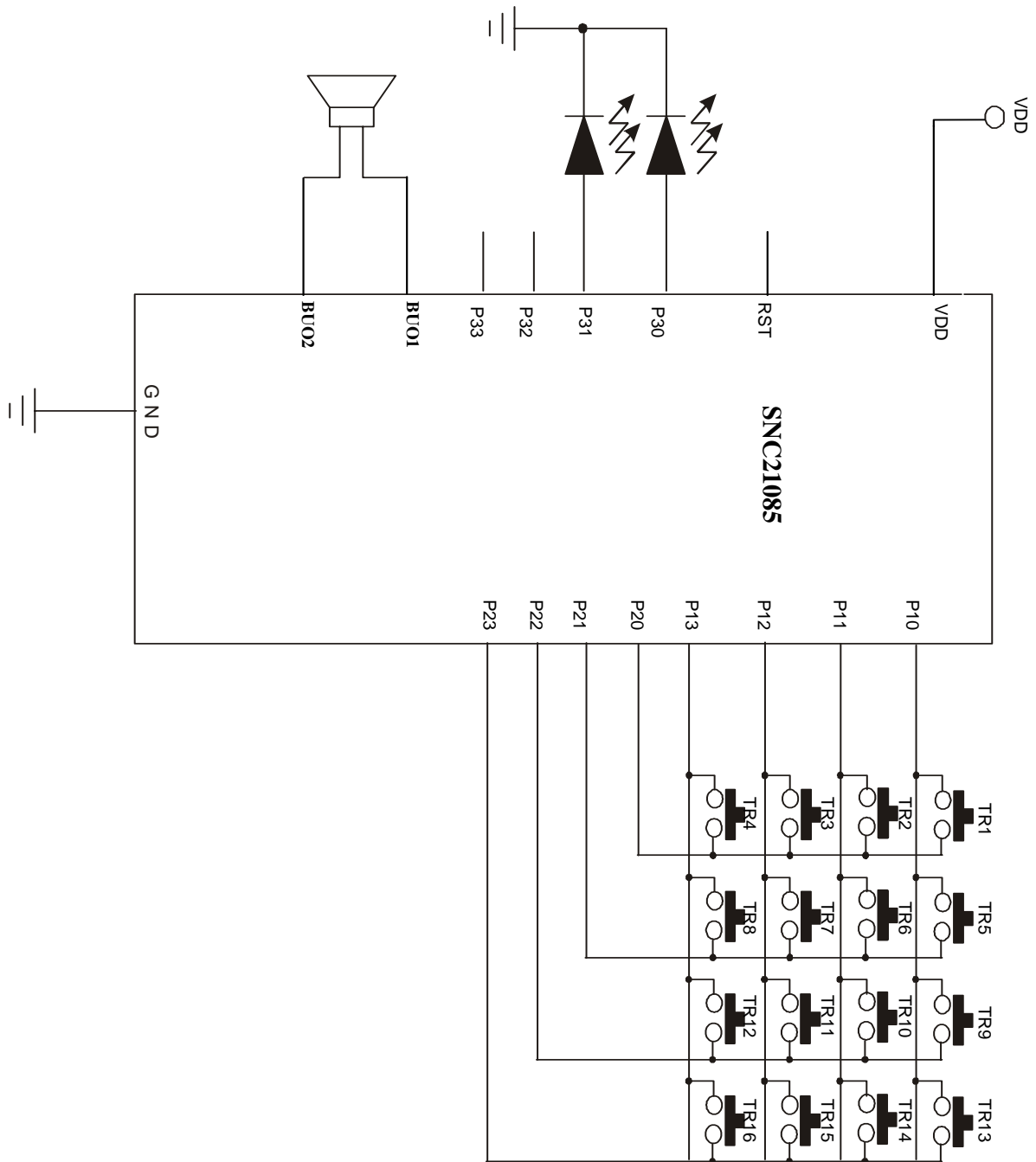
6. ABSOLUTE MAXIMUM RATING

| Items | Symbol | Min | Max | Unit. |
|-----------------------|------------|--------------|--------------|-------|
| Supply Voltage | $V_{DD}-V$ | -0.3 | 6.0 | V |
| Input Voltage | V_{IN} | $V_{SS}-0.3$ | $V_{DD}+0.3$ | V |
| Operating Temperature | T_{OP} | 0 | 55.0 | °C |
| Storage Temperature | T_{STG} | -55.0 | 125.0 | °C |

7. ELECTRICAL CHARACTERISTICS

| Item | Sym. | Min. | Typ. | Max. | Unit | Condition |
|-------------------------------------|-----------|------|------------|------|---------|--|
| Operating Voltage | V_{DD} | 2.4 | 3.0 | 5.5 | V | |
| Standby current | I_{SBY} | - | 3.0 5.0 | - | μA | $V_{DD}=3V$, no load $V_{DD}=4.5V$, no load |
| Operating Current | I_{OPR} | - | 300 | - | μA | $V_{DD}=3V$, no load |
| Input current of P1, P2, P3 | I_{IH} | - | 3.0 | - | μA | $V_{DD}=3V, V_{IN}=3V$ |
| Drive current of P1, P2, P3.0, P3.1 | I_{OD} | 3 | 4 | - | mA | $V_{DD}=3V, V_O=2.4V$ |
| Sink Current of P1, P2, P3.0, P3.1 | I_{OS} | 4 | 6 | - | mA | $V_{DD}=3V, V_O=0.4V$ |
| Drive current of P3.2, P3.3 | I_{OD} | 6 | 8 | - | mA | $V_{DD}=3V, V_O=2.4V$ |
| Sink current of P3.2, P3.3 | I_{OS} | 10 | 16 | - | mA | $V_{DD}=3V, V_O=2.4V$ |
| Push-Pull current | I_{PP} | - | 70 | - | mA | $V_{DD}=3V$, Output 1K Sin wave. |
| Push-Pull current | I_{PP} | - | 100 | - | mA | $V_{DD}=4.5V$, Ouput 1K Sin wave. |
| Oscillation Freq. | F_{OSC} | - | 2.0 | - | MHz | $V_{DD}=3V$ |

8. APPLICATION CIRCUIT



DISCLAIMER

The information appearing in SONiX web pages (“this publication”) is believed to be accurate.

However, this publication could contain technical inaccuracies or typographical errors. The reader should not assume that this publication is error-free or that it will be suitable for any particular purpose. SONiX makes no warranty, express, statutory implied or by description in this publication or other documents which are referenced by or linked to this publication. In no event shall SONiX be liable for any special, incidental, indirect or consequential damages of any kind, or any damages whatsoever, including, without limitation, those resulting from loss of use, data or profits, whether or not advised of the possibility of damage, and on any theory of liability, arising out of or in connection with the use or performance of this publication or other documents which are referenced by or linked to this publication.

This publication was developed for products offered in Taiwan. SONiX may not offer the products discussed in this document in other countries. Information is subject to change without notice. Please contact SONiX or its local representative for information on offerings available. Integrated circuits sold by SONiX are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. The application circuits illustrated in this document are for reference purposes only. SONiX DISCLAIMS ALL WARRANTIES, INCLUDING THE WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. SONiX reserves the right to halt production or alter the specifications and prices, and discontinue marketing the Products listed at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders.

Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by SONiX for such application.