========== CONTENTS ==========

AMENDENT HISTORY

Version	Date	Description
Ver 1.0	2012/07/19	First Version.
Ver 1.1	2012/08/06	Modify Section 15 “Electrical Characteristics”
Ver 1.2	2013/01/31	Remove UART related word (Chapter 9)

1. Introduction

The SNP70032 is a 16-bit DSP processor with SONiX OID decoder function. It runs at 48MHz with 48MIPS high performance processing speed. SNP70032 built-in 64KW ROM, 16KW Program RAM and 16KW Working RAM. However, it allows run code at external SPI flash.

Peripherals embedded in the SNP70032 include OID sensor interface, XtraROM interface, SD/MMC controller, USB device, MSP, SPI Master/Slave interface, PWM Output, Audio ADC SAR ADC, Stereo DAC and I2S.

2. Features

- Built-in 16-bit DSP core
- 48 MIPS CPU Performance under 48MHz, 1 Clock per 1 Instruction.
- Clock Type:
  - 48MHz for system clock
  - 32KHz for system clock
- High Speed Clock Source (pumping from 12MHz → 48MHz by PLL circuit)
  - 12MHz crystal oscillator
- Low Speed Clock Source:
  - 32KHz clock is be generated from 12MHz (The actually is 31250Hz)
- Operation Mode:
  - Normal mode (hi-speed clock enable)
  - Slow mode (hi-speed clock enable, PLL disable, slow-speed clock disable)
  - Watch mode (chip entry power-down mode and wake-up per 0.5/1 sec automatically)
  - Power-down mode (both hi-speed and low-speed clock disable)
- Three 16-bit Timers, 1 Watch Dog Timer, 1 RTC
  - Timers with Individual pre-scalar and auto-reload function
  - Event Counter (Combine Timer and Input Pin P0.0~P0.2)
  - Watch Dog Timer (WDT) with 0.25/0.5/1/2-sec period
  - RTC with 0.5/1-sec period
- Interrupt Sources
  - 1 for ADC, 3 for Timers, 1 for RTC, 1 for SPI, 1 for AD, 1 for DA, 1 for I2S, 1 for MSP
  - 3 for External (P0.0~P0.2), 1 for USB, 1 for XtraROM, 4 for DMA
- 64K*16 ROM and 16K*16 Program RAM
- Total 16K*16 Internal RAM memory configuration for Program or Working RAM
  - Mode 0: 8K*16 Program RAM + 8K*16 Working RAM
  - Mode 1: 4K*16 Program RAM + 12K*16 Working RAM
  - Mode 2: 12K*16 Program RAM + 4K*16 Working RAM (default)
  - Mode 3: 16K*16 Working RAM
- Support Barrel Shifter and 16×16 to 32-bit multiplier
- DMA provided (USB/XtraROM/SD/SPI)
- Built-in ICE Debug Function

2.1 SNP70032 Series Features

Device	SNP70032XXB2FG	SNP70032XXB1FG
Pins	100	80
Communication SPI	Yes	No 4-bit Mode
Huffman Decoder	Yes	Yes
ICE	Yes	Yes
GPIO INT	3	1
MSP	Yes	No
OID	Yes	Yes
Program SPI	Yes	Yes
PWM	4	1
RTC	1	1
SAR ADC	4	2
SD ADC	Yes	Yes
SD DAC	Yes	Yes
SD Card 1	Yes	Yes
SD Card 2	Port 1 or Port 3	Port 3
Timer	3	3
USB	Yes	Yes
WDT	Yes	Yes
XtraROM	Yes	Yes

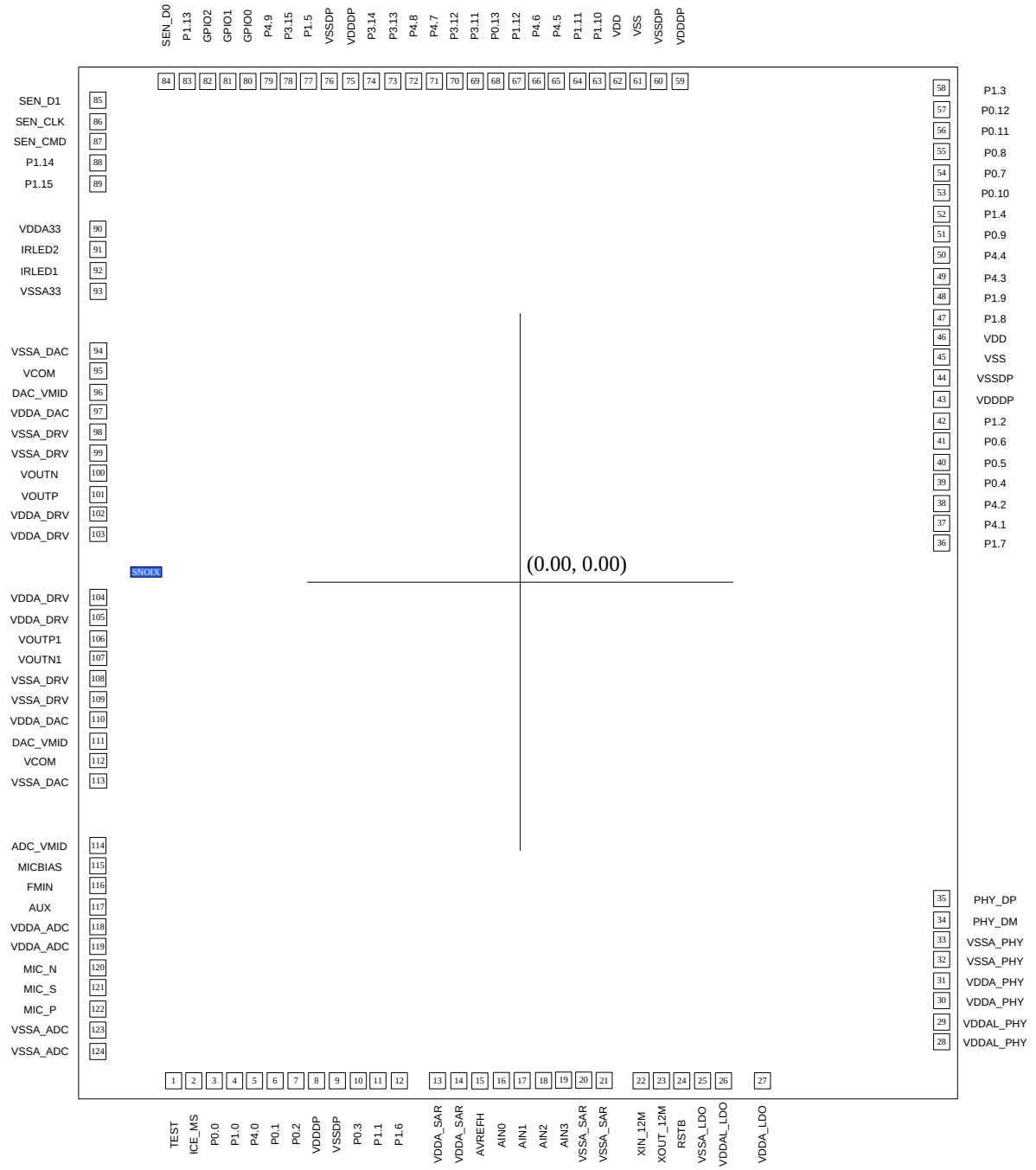
《Note》：

The bit7 (SYSCONF) of register 0x7C can be selected SD Card 2 output pin. 0: SD Card 2 pinout at Port3; 1: SD Card 2 pinout at Port 1.

2.2 Pin Diagrams

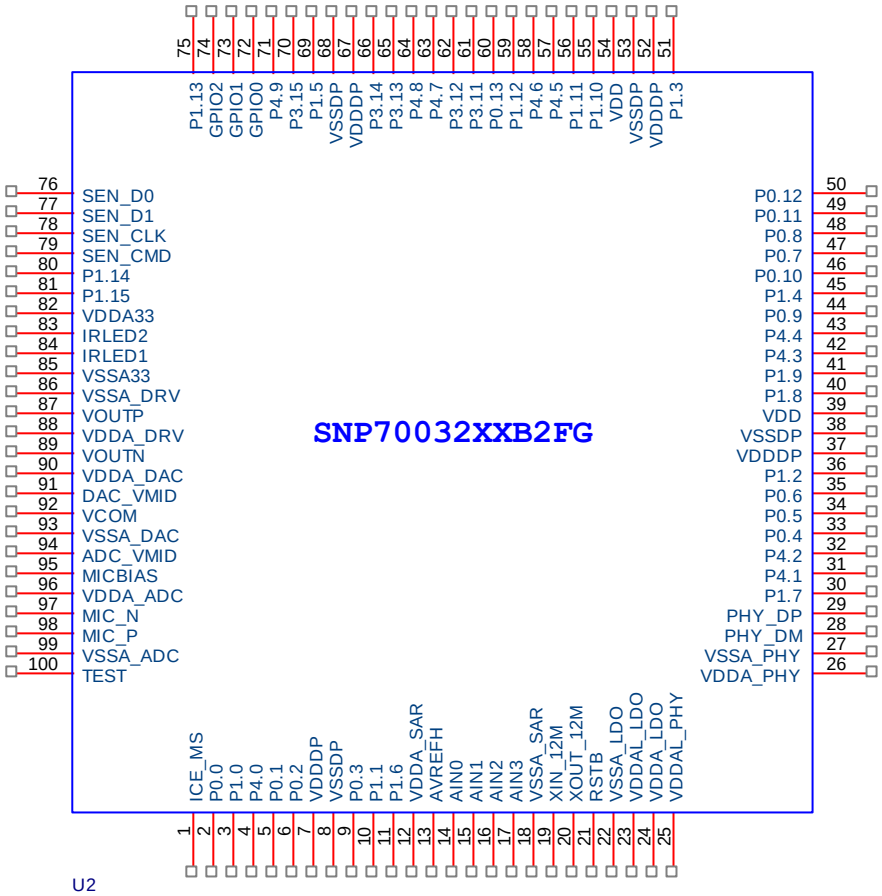
Dice

SONIX TECHNOLOGY CO., LTD.
BONDING PAD LOCATION

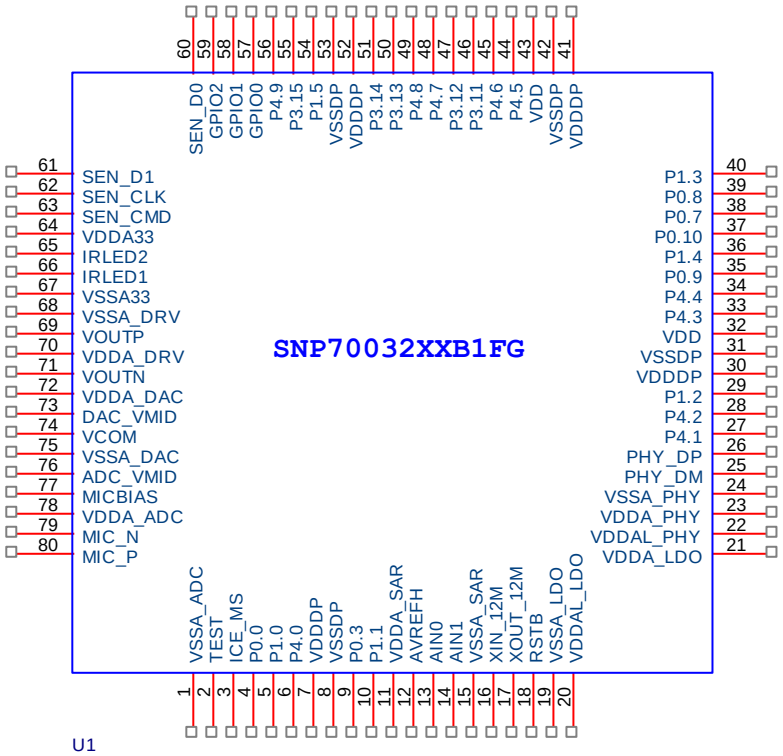


SNP70032XXBH

LQFP100



LQFP80



3. Multi-Function of I/O

	Pin	Multi-Function of I/O				LQFP100 SNP70032XXB2FG	LQFP80 SNP70032XXB1FG	Remark
PORT0	P0.0	INT	INT0			●	●	USB_Plug In
	P0.1		INT1			●		
	P0.2		INT2			●		
	P0.3	PWM	PWMIO#0			●	●	SD1_Power
	P0.4		PWMIO#1			●		SD2_Power
	P0.5		PWMIO#2			●		
	P0.6		PWMIO#3			●		
	P0.7	Communication SPI	SPISCK2	ICE	ICE_SCK	●	●	
	P0.8		SPIMISO2		ICE_CSB	●	●	
	P0.9		SPIMOSI2		ICE_MOSI	●	●	
	P0.10		SPICS2		ICE_MISO	●	●	
	P0.11		SPID2			●		
	P0.12		SPID3			●		
	P0.13					●		
PORT1	P1.0	Program SPI	SPICS1			●	●	
	P1.1		SPISCK			●	●	
	P1.2		SPIMISO			●	●	
	P1.3		SPIMOSI			●	●	
	P1.4		SPIED2			●	●	
	P1.5		SPIED3			●	●	
	P1.6	MSP	MSP_CLK			●		
	P1.7		MSP_DAT			●		
	P1.8					●		
	P1.9					●		
	P1.10	SD Card 2	SDCLK#2			●		
	P1.11		SDCMD#2			●		
	P1.12		SDD0#2			●		
	P1.13		SDD1#2			●		
	P1.14		SDD2#2			●		
	P1.15		SDD3#2			●		

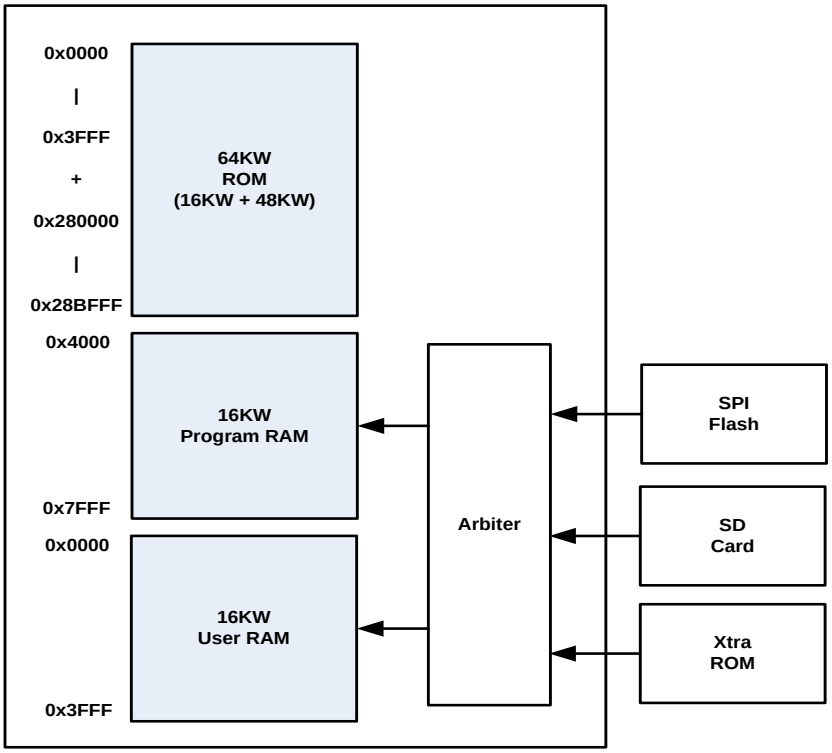
PORT3	P3.11		NFCS	SD Card 2	SDCLK#2	●	●	
	P3.12		R/B		SDCMD#2	●	●	
	P3.13		NFALE		SDD0#2	●	●	
	P3.14				SDD1#2	●	●	
	P3.15		NFRE		SDD2#2	●	●	
PORT4	P4.0	Xtra ROM	NFWP	SD Card 1	SDCLK	●	●	
	P4.1		NFCLE		SDCMD	●	●	
	P4.2		NFD0		SDD0	●	●	
	P4.3		NFD1		SDD1	●	●	
	P4.4		NFD2		SDD2	●	●	
	P4.5		NFD3		SDD3	●	●	
	P4.6		NFD4		SDD3#2	●	●	
	P4.7		NFD5			●	●	
	P4.8		NFD6			●	●	
	P4.9		NFD7			●	●	
	P4.12	SAR ADC	ADC0			●	●	
	P4.13		ADC1			●	●	
	P4.14		ADC2			●		
	P4.15		ADC3			●		

4. Pin Assignments

Symbol	Descriptions	No. of Pin	Pin Count
VDDA_LDO	Power for Regulator	1	1
VDDAL_LDO	Regulator voltage output	1	2
VSSA_LDO	Regulator Ground	1	3
VDD	Power + for core	2	5
VSS	Power - for core	2	7
VDDDP	Power for IO	4	11
VSSDP	GND for IO	4	15
VDDA_DAC	Power for Audio DAC	2	17
VSSA_DAC	GND for Audio DAC	2	19
VCOM	Audio DAC Common mode output	2	21
DAC_VMID	Audio DAC VMID output	2	23
VDDA_DRV	Audio DAC Driver Power	4	27
VSSA_DRV	Audio DAC Driver GND	4	31
VOUTP	Audio DAC output (+)	2	33
VOUTN	Audio DAC output (-)	2	35
ADC_VMID	SD ADC VMID output	1	36
MICBIAS	SD ADC Microphone Bias Voltage output	1	37
FMIN	SD ADC FM signal input pin	1	38
AUX	SD ADC AUX signal input pin	1	39
VDDA_ADC	Power for SD ADC	2	41
VSSA_ADC	GND for SD ADC	2	43
MIC_N	SD ADC MIC difference input (-)	1	44
MIC_S	SD ADC MIC single input	1	45
MIC_P	SD ADC MIC difference input (+)	1	46
VDDA_SAR	Power for SAR ADC	2	48
VSSA_SAR	GND for SAR ADC	2	50
AVREFH	Reference Voltage for SAR ADC	1	51
AIN[3:0]	SAR ADC Anlong input pin	4	55
XIN_12M	High speed clock crystal input	1	56
XOUT_12M	High speed clock crystal output	1	57
RSTB	Chip reset	1	58
TEST	For test only	1	59
PHY_DM	USB Data +	1	60
PHY_DP	USB Data -	1	61
VDDA_PHY	USB power + (3.3V)	2	63
VDDAL_PHY	USB power + (1.8V)	2	65
VSSA_PHY	USB power -	2	67
GPIO[2:0]	OID GPIO	3	70
SEN_CLK	OID Sensor CLK	1	71
SEN_CMD	OID Sensor CMD	1	72
SEN_D[1:0]	OID Sensor DATA	2	74
VDDA33	Power for IRLED	1	75
VSSA33	GND for IRLED	1	76
IRLED1	IRLED1 Output Current	1	77
IRLED2	IRLED2 Output Current	1	78
P0.0~P0.13	General I/O port P0.0~P0.13	14	92
P1.0~P1.15	General I/O port P1.0~P1.15	16	108
P3.11~P3.15	General I/O port P3.11~P3.15	5	113
P4.0~P4.9	General I/O port P4.0~P4.9	10	123
ICE_MS	ICE Function	1	124

5. Memory

In SNP70032, it includes 64KW ROM, 16KW Program RAM and 16KW User RAM. The following is the detailed description.



5.1 Internal Program Memory

In SNP70032 program memory, we provide SONiX standard code in the 64KW ROM, it includes MP3, FAT, SD Card/XtraROM, ADC, DAC and so on function, the detailed function and usage please refer to Application Note. Moreover, the 16KW Program RAM is reserved for user to run their function which is from external storage, for example, SPI Flash, SD Card or XtraROM.

Address Range	Size (word)	Usage	DSP	DMA
0x000000 ~ 0x003FFF	16K	Program ROM	R	--
0x280000 ~ 0x28BFFF	48K	Program ROM	R	--
0x004000 ~ 0x007FFF	16K	Program RAM	R	R/W

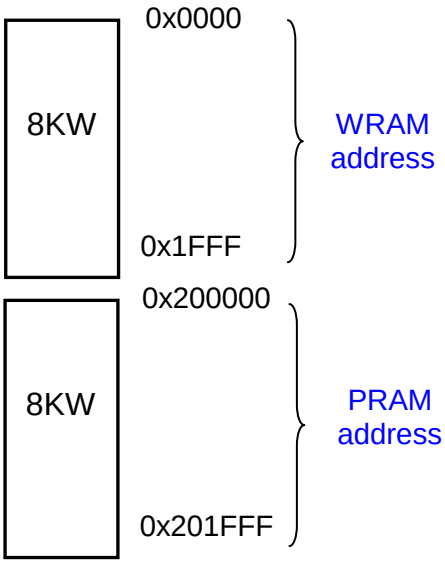
5.2 Internal User RAM

Total 16K*16 Internal RAM memory configuration for Program and Working RAM

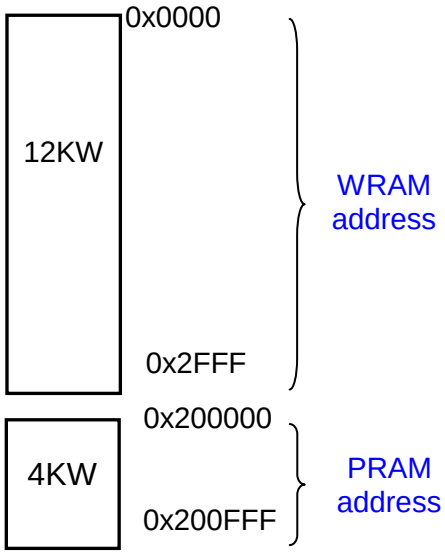
- Mode 0: 8K*16 Program RAM + 8K*16 Working RAM
- Mode 1: 4K*16 Program RAM + 12K*16 Working RAM
- Mode 2: 12K*16 Program RAM + 4K*16 Working RAM (default)
- Mode 3: 16K*16 Working RAM

※ SONiX standard ROM code has set it as Mode 3 (16KW Working RAM)

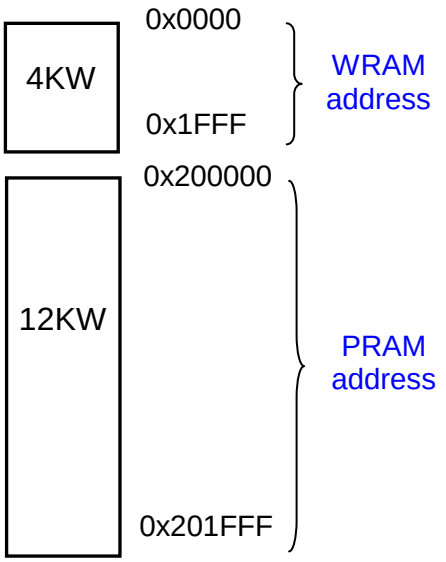
Mode 0



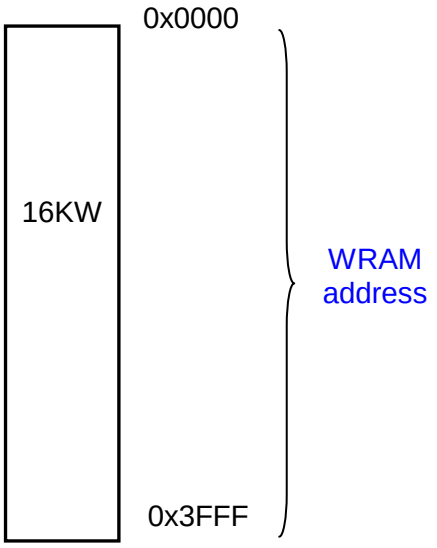
Mode 1



Mode 2



Mode 3



5.3 External Program Memory

Address Range	Size (word)	Usage	DSP	DMA
0x400000 ~ 0xBFFFFF	8M	CS1 SPI Flash	R	R/W

6. System Clock

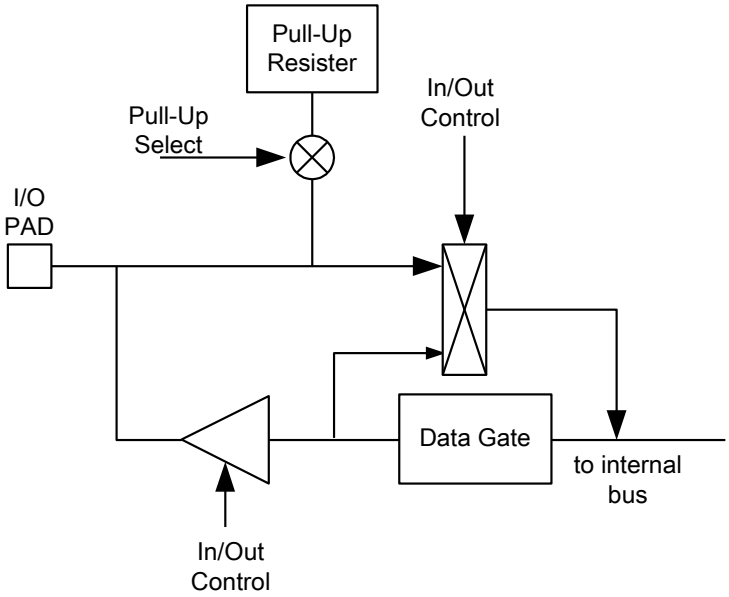
SNP70032 is a dual clock system that provides high-speed clock (12MHz crystal up to 48MHz) and low-speed clock (12MHz or 32KHz). The SN9P70031A uses an internal PLL to up sample clock speed to 48MHz.

7. I/O Port

SNP70032 provides total of 45 I/O pins (P0.0 ~ P0.13, P1.0 ~ P1.15, P3.11 ~ P3.15, P4.0 ~ P4.9). The input pull-high resistor of each pin can be individually programmed by port pull-high register and the direction of I/O port is selected by port direction register. The I/O port P0.0~P0.13 and P1.0~P1.15 can wake up the chip from the standby mode.

These 45 programmable I/O pins provide not only a simply input/output function but also can configure to be chip select pins of extension bus and multi-function peripheral interfaces. For details please refer to the following sections. However, analog input pins (AIN0~AIN3) of SAR ADC can be selected to act as digital input only.

The internal structure of I/O pins is showed in Figure-1.



I/O Configuration

Figure-1

8. Timer/Counter

SNP70032 provides three 16-bit timer/event counters (T0/T1/T2). Each timer is 16-bit binary up-count timer with pre-scalar and auto-reload function.

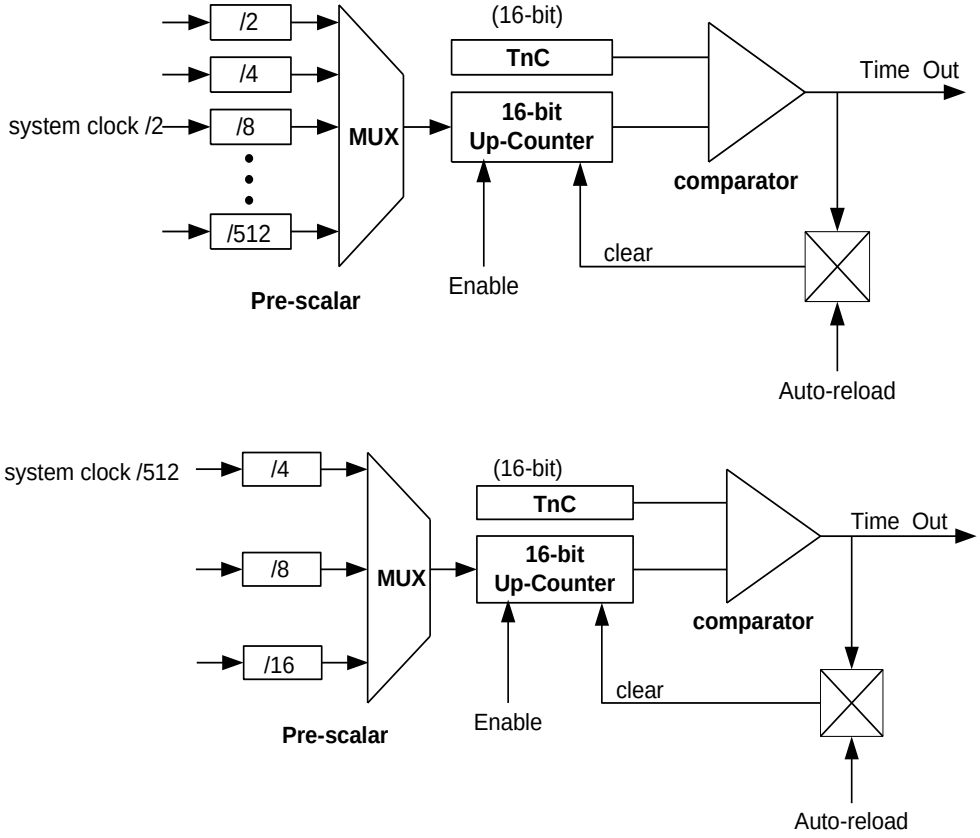


Figure-2

9. Interrupt

At the moment when SNP70032 enters the interrupt service routine, the GIE bit (in INTEN) will be cleared to "0“for blanking other interrupts. However, during this stage, other enabled interrupt sources still can issue their requests but the requests are queued in INTRQ. GIE will be restored to “1” while DSP exits ISR. Then the other valid interrupt can be granted and served immediately.

Interrupt Vector	Priority	Entry Location	Descriptions
Reset	x	0x000000	Reset
Reserved		0x000010	
AD	4	0x000014	AD FIFO full
T0	5	0x000018	T0 overflow
P0.0	6	0x00001C	Falling/Raising edge of P0.0
T1	7	0x000020	T1 overflow
P0.1	8	0x000024	Falling/Raising edge of P0.1
T2	9	0x000028	T2 overflow
P0.2	10	0x00002C	Falling/Raising edge of P0.2
Reserved	9	0x000030	
DA	11	0x000034	DA FIFO empty
SPI	3	0x000038	SPI Interrupt
MSP(I2C)	2	0x00003C	MSP Interrupt
I2S	1	0x000040	I2S Interrupt
Reserved		0x000044	
Reserved		0x000048	
Reserved		0x00004C	
USB	12	0x000050	USB Interrupt
Reserved		0x000054	
RTC	13	0x000058	RTC overflow
SD	14	0x00005C	SD Card Interrupt
Reserved		0x000060	
DMA_SD_RW	15	0x000064	DMA_SD_R & DMA_SD_W Interrupt
SAR_AD	16	0x000068	SAR ADC interrupt
DMA_SD2_RW	17	0x00006C	DMA_SD2_R & DMA_SD2_W Interrupt
Reserved		0x000070	
Reserved		0x000074	
DMA_DEV_RW	18	0x000078	DMA_DEV_R & DMA_DEV_W nterrupt

10. External Storage Devices

10.1 SPI Flash Controller

SNP70032 has a built-in SPI Flash controller interface to support 1/2/4 bit read/write mode, it can run 6/12/24/48 MHz clock frequency. In additional, SNP70032 can run programs from SPI Flash (at a much reduced rate).

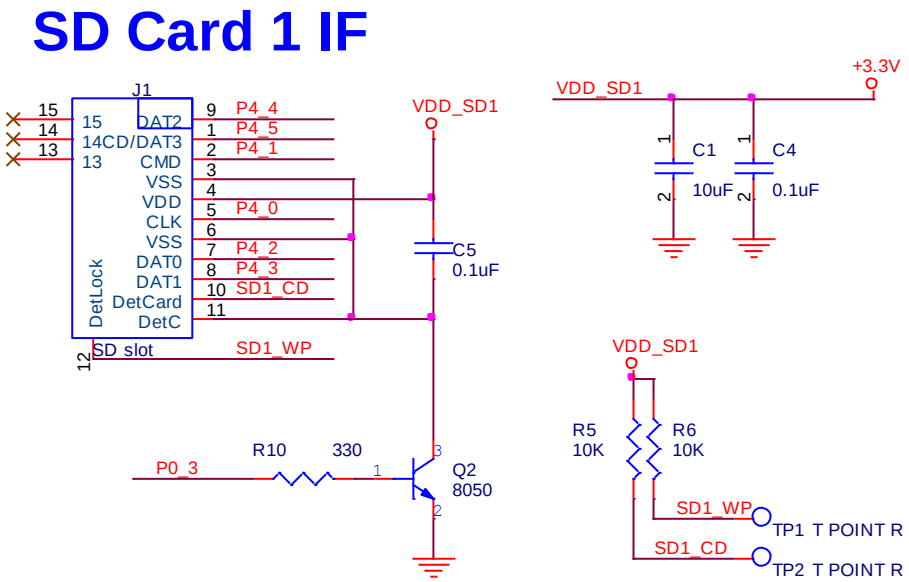
10.2 XtrROM / SD Card Interface

The flash memory (Mass-storage) interface provides an interface between Mass storage and SNP70032 DSP core. It supports 2 types of storage memory: XtraROM and SD Card.

- XtraROM (NAND read only)
- SD Card Controller support SD Card1.0/2.0 commands (SDSC/SDHC)

Function \ Device	LQFP100	LQFP80
Support 1 SD Card	●	●
Support 2 SD Card	●	●
Support 1 XtraROM	●	●
Support 1 XtraROM + 1 SD Card	●	

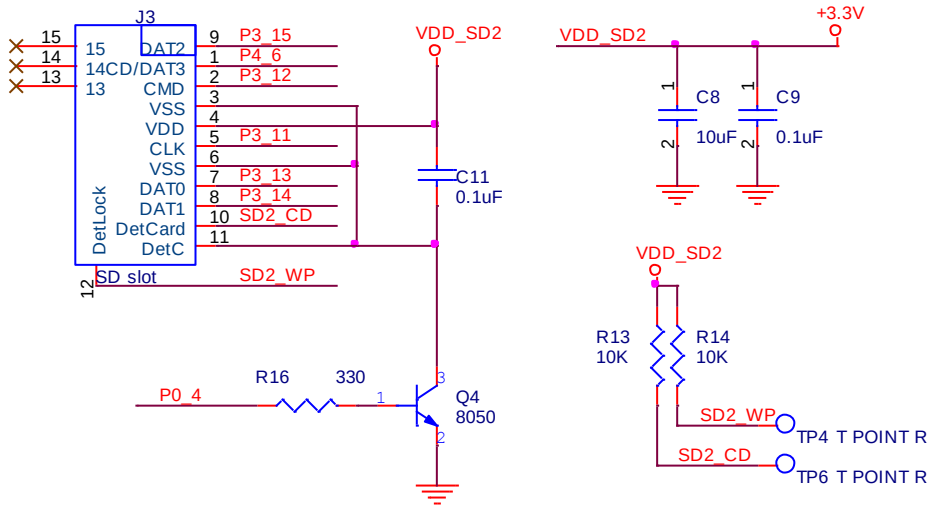
Support only one SD Card application circuit



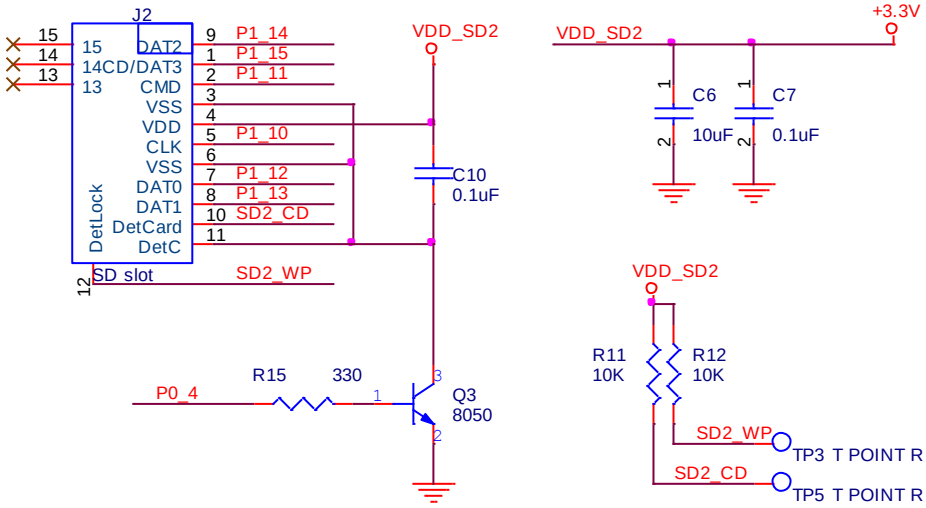
Support two SD Card application circuit

In SNP70032, it allows to access two SD Card at the same time, and the following is the 2nd set SD Card application circuit. And its pinout is option for user's application.

SD Card 2 IF(Port 3)



SD Card 2 IF(Port 1)

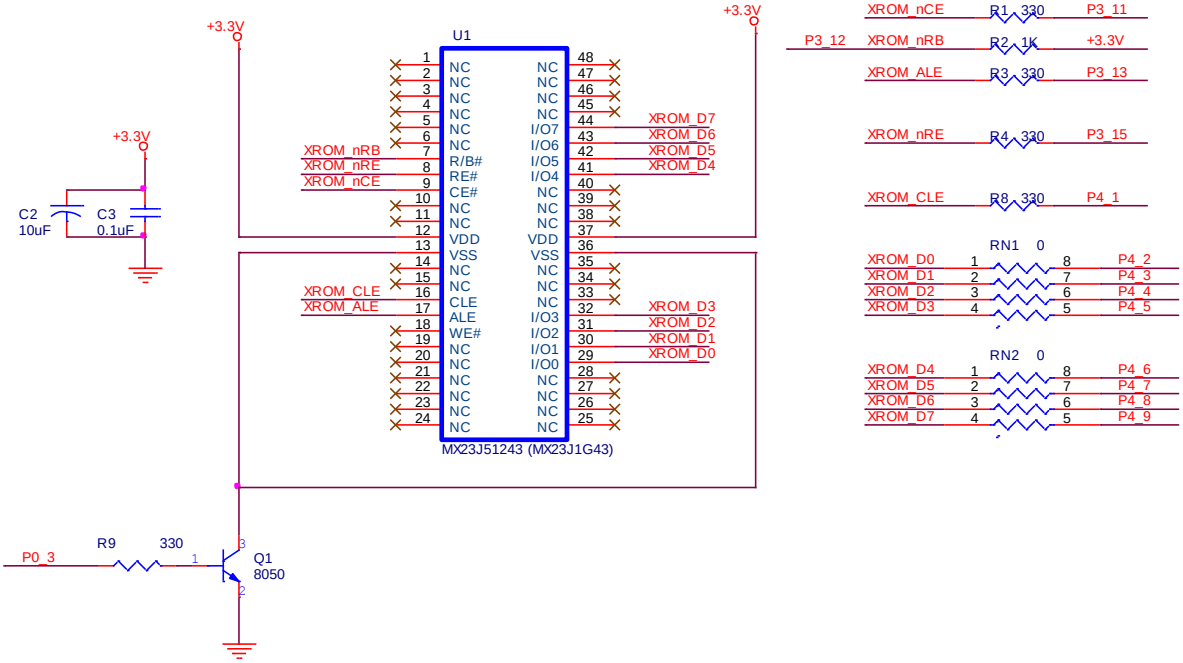


《Note》:

The bit7 (SYSCONF) of register 0x7C can be selected SD Card 2 output pin. 0: SD Card 2 pinout at Port3; 1: SD Card 2 pinout at Port 1.

Support only one XtraROM application circuit

XtraROM



Support one XtraROM and one SD Card application circuit

Just LQFP100 has support one XtraROM and one SD Card function.

《Note》:

The bit7 (SYSCONF) of register 0x7C must be set as “1”.

11. Audio CODEC

11.1 ADC

In SNP70032, we provide one set of high performance one channel Analog-to-Digital Converter (ADC) for microphone applications with typical SNR at 90dB. This Analog-to-Digital Converter has a built-in PGA(-12dB ~ +33dB), BOOST(0 ~ +30dB) and true AGC control. It supports 8/12/16/22.05/24/32/44.1/48KHz sample rates.

11.2 Stereo Audio DAC

In SNP70032, we provide a 16-bit stereo DAC + Class AB embedded, and its typical SNR is 90dB. It can drive L/R channel Earphone. A 16x16 FIFO is used to prevent the sound glitch when CPU is busy. They all support 8/12/16/22.05/24/32/44.1/48KHz sample rates.

12. 10-bit SAR ADC

SNP70032 has built-in SAR ADC, which has 4-input sources with up to 1024-step resolution to transfer analog signal into 10-bits digital data. The sequence of ADC operation is to select input source (AIN0 ~ AIN3) first, then set CHS and START bit to “1” to start conversion. When the conversion is complete, the ADC circuit will set START bit to “0” and final value output will reside in the ADR register. In SNP70032, we provide an interrupt to inform user program that the ADC result is ready. However, the interrupt event is optional.

13. Communication Interface

13.1 USB Interface

The SNP70032 provides a USB 2.0 High Speed (480MHz) interface (includes 4 endpoint); user can download/upload data from/to PC through this USB interface. It supports control transfer, interrupt transfer and bulk transfer. SNP70032 provides twin 512byte buffers for bulk in/out transition, one 64-byte buffer for control transition and one 16byte buffer for interrupt transition.

- EP0: Control transfer
- EP1: bulk-in (mass-storage, DSP→PC)
- EP2: bulk-out (mass-storage, PC→DSP)
- EP3: interrupt-in (HID, DSP→PC)

13.2 I2S Interface

Built-in I2S interface. Digital audio data to external audio DAC. One L/R channel 16x16 FIFO is used to prevent sound glitches when the CPU is busy.

13.3 MSP Interface

The MSP (Main Serial Port) is a serial communication interface for data exchanging from one MCU to another MCU or other hardware peripherals. These peripheral devices may be serial EEPROM, A/D converters, Display device, etc. The MSP module can operate in one of two modes

- Full Master Mode
- Slave Mode (with general address call)

13.4 SPI Interface

The SPI (serial peripheral interface) is a synchronous serial bus that provides good support for communication with SPI-compatible peripheral devices. The SPI peripheral is a synchronous, 7-wire interface consisting of two data pins (SPITxD and SPIRxD); two additional pins (SPIED3 and SPIED2) for 4-bit mode access, two slave select pins (/SS1, /SS2); and a synchronous clock pin (SCLK). The two data pins permit full-duplex and half-duplex operation to other SPI-compatible devices. The SPI also includes programmable baud rates, clock phase (CPHA), and clock polarity (CPOL).

13.5 OID Sensor Interface

SNP70032 also built-in SONiX OID decoder for ELA application.

- Support dot pattern format : OID_Code_v2
- Embedded 16 bit-DSP for sensor control and image pattern recognition
- Light source timing control

14. Regulator

The SNP70032 built-in a linear regulator for core power (CVDD). The accuracy output voltage is 1.8V±0.18V and it can be power downed by software.

15. Electrical Characteristics

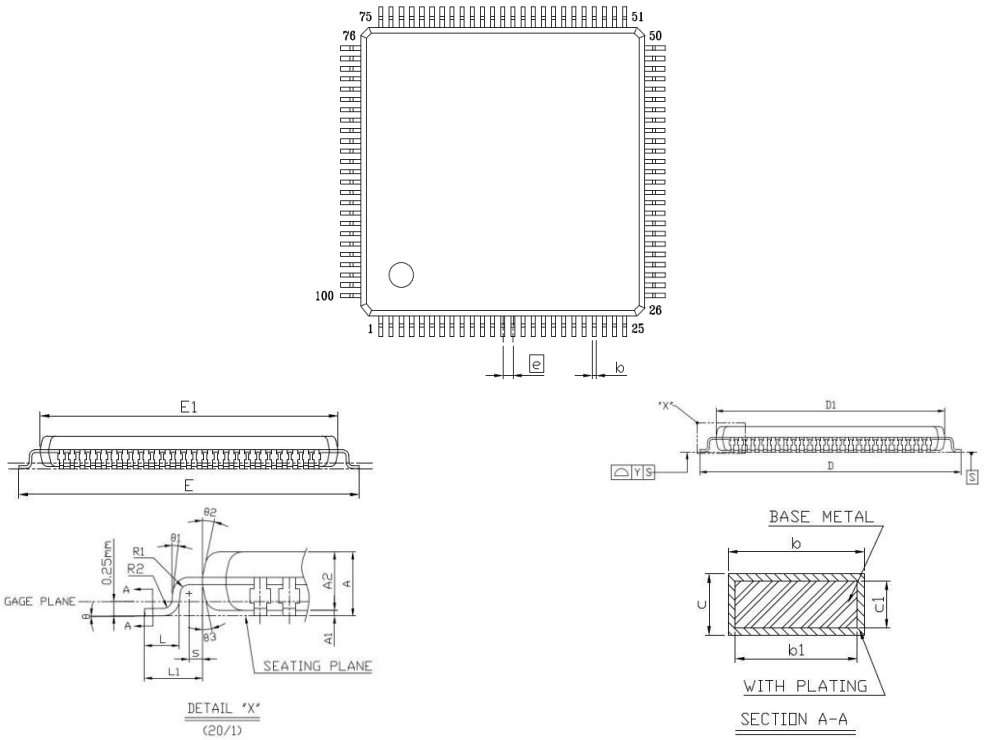
Item	Sym.	Min.	Typ.	Max.	Unit	Condition (TA=25℃, V_{DD}=3.3V)
Operating Voltage VDD	V_{DD}	2.7	3.3	3.6	V	
Operating Voltage CVDD	CV_{DD}	1.62	1.8	1.98	V	
Standby current	I_{SBY}	-	30	60	uA	V_{DD}=3.3V, No load
SAR ADC ENOB	ENOB	-	9	-	bit	
SAR ADC INL	INL	-	1	-	bit	
SAR ADC DNL	DNL	-	1	-	bit	
SD-ADC SNR	SNR	-	90	-	dB	
SD-DAC SNR	SNR	-	90	-	dB	
Drive current of P0, P1.0, P1.6~P1.15, P3, P4.0~P4.9	I_{OD}	-	6	-	mA	V_O=2.4V
Sink Current of P0, P1.0, P1.6~P1.15, P3, P4.0~P4.9	I_{OS}	-	4	-	mA	V_O=0.4V
Drive current of P1.1~P1.5	I_{OD}	-	16	-	mA	V_O=2.4V
Sink Current of P1.1~P1.5	I_{OS}	-	16	-	mA	V_O=0.4V
Sink Current of P1.1~P1.5	I_{OS}	-	4	-	mA	V_O=0.4V(Note1)
Oscillation Freq. (crystal)	F_{OSC}	-	12	-	MHz	

Note1: P4.12~P4.15 (input only) are shared pin with “SAR ADC”AIN0~AIN3.

16. Package Details

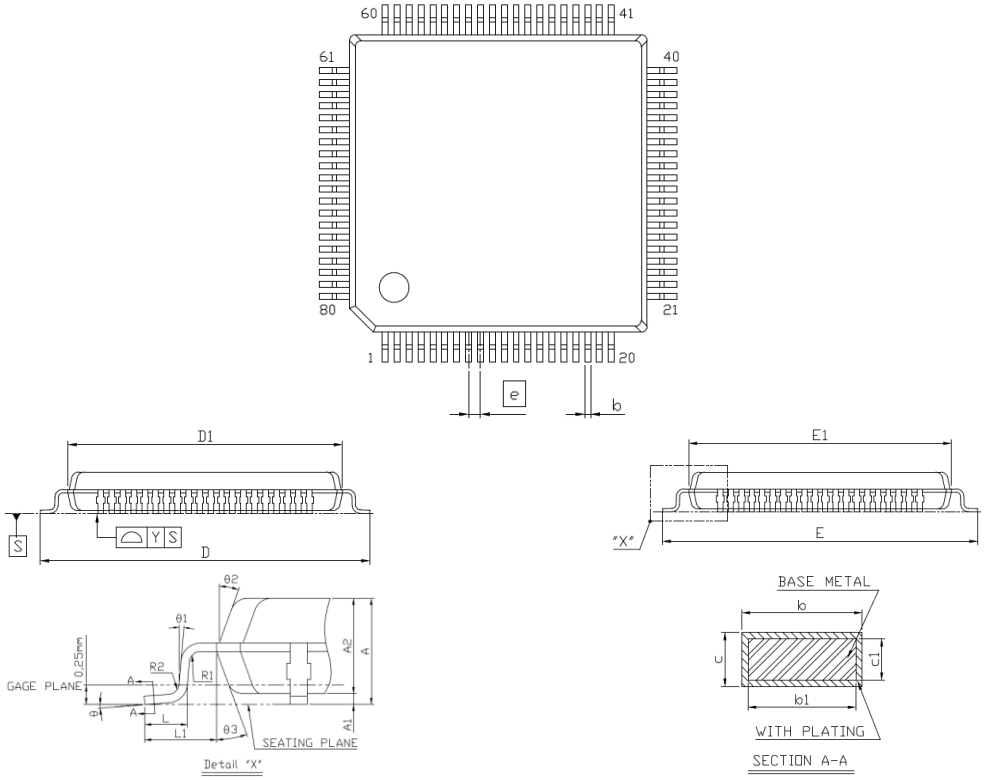
The following sections give the technical details of the packages.

LQFP 100 (14x14x1.4mm)



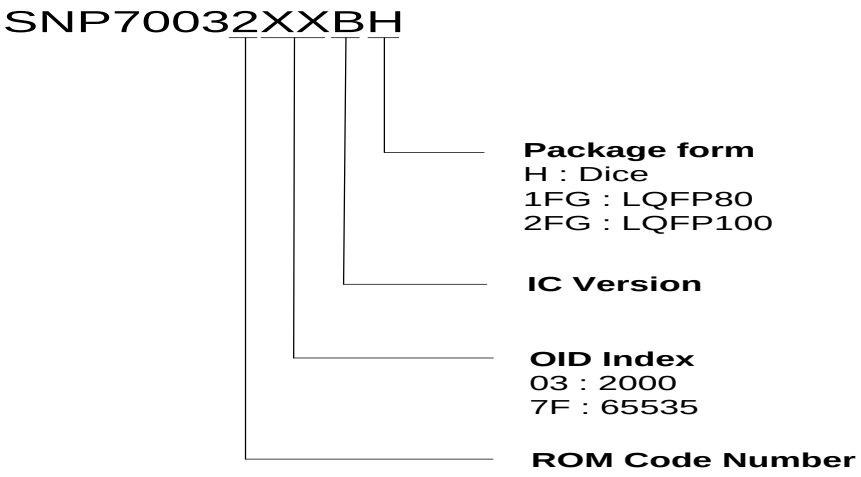
SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.17	0.22	0.27	7	9	11
b1	0.17	0.20	0.23	7	8	9
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D	15.90	16.00	16.10	626	630	634
D1	13.90	14.00	14.10	547	551	555
E	15.90	16.00	16.10	626	630	634
E1	13.90	14.00	14.10	547	551	555
e	0.50 BSC			20 BSC		
L	0.45	0.60	0.75	18	24	30
L1	1.00 REF			39 REF		
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.08			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
s	0.20			8		

LQFP 80 (10x10x1.4mm)



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.13	0.18	0.23	5	7	9
b1	0.13	0.16	0.19	5	6	7
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D	11.90	12.00	12.10	368	472	476
D1	9.90	10.00	10.10	390	394	398
E	11.90	12.00	12.10	368	472	476
E1	9.90	10.00	10.10	390	394	398
e	0.40 BSC			16 BSC		
L	0.45	0.60	0.75	18	24	30
L1	1.00 REF			39 REF		
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.08			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ 1	0°			0°		
θ 2	11°	12°	13°	11°	12°	13°
θ 3	11°	12°	13°	11°	12°	13°

17. Part Name Description



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