ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{D1}, V_{DD} .... −0.3V to +12V

Storage Temperature .... −25°C to +125°C

Clock

Crystal Frequency 3.12MHz

DC CHARACTERISTICS

Operating Temperature T_A = 0°C to +70°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.6	—	7	V	
Standby Supply Voltage	V_{D1}	4.6	—	7	V	
Primary Supply Current	I_{DD}	—	—	90	mA	V_{D1}, V_{DD} = 7.0V, T_A = 25°C
Standby Supply Current	I_{D1}	—	—		mA	V_{SS} = 0.0V, T_A = 25°C
Inputs A1-A8, $\overline{ALD}$, SER IN, TEST, SE						
Logic 0	V_{IL}	0	—	0.6	V	
Logic 1	V_{IH}	2.4	—	V_{D1}	V	
Capacitance	C_{IN}	—	—	10	pf	
Leakage	I_{LC}	—	—	±10	µA	
$\overline{RESET}$, $\overline{SBY\ RESET}$ Logic 0	V_{IL1}	0	—	0.6	V	
Logic 1	V_{IH1}	3.6	—	V_{D1}	V	
Oscillator Leakage OSC 1	—	1.0	—	10	µA	No Load, OSC1 = 7.0V
Outputs SBY, DIGITAL OUT, C1, C2, C3, $\overline{LRQ}$, ROM DISABLE, ROM CLOCK, SER OUT Logic 0	V_{OL}	0	—	0.6	V	0.72mA (2 LS TTL Loads)
Logic 1	V_{OH}	3.5	—	V_{D1}	V	−50µA (2 LS TTL Loads)

AC CHARACTERISTICS

Operating Temperature: T_A = 0°C to +70°C

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Clock Frequency	—	—	3.120	—	MHz	Crystal
$\overline{Reset}$, $\overline{SBY\ Reset}$	t_{pw1}	100	—	—	µs	
$\overline{ALD}$ (<800ns)	t_{pw2}	200	—	800	ns	
A1-A8 Set Up	t_{s2}	160	—	—	ns	
A1-A8 Hold	t_{h2}	160	—	—	ns	
$\overline{ALD}$ (≥800ns)	t_{pw3}	800	—	—	ns	
A1-A8 Set Up	t_{s3}	0	—	—	ns	
A1-A8 Hold	t_{h3}	1200	—	—	ns	
$\overline{LRQ}$	t_{pd0}	—	—	640	ns	
SBY	t_{pd0}	—	—	640	ns	

AUDIO
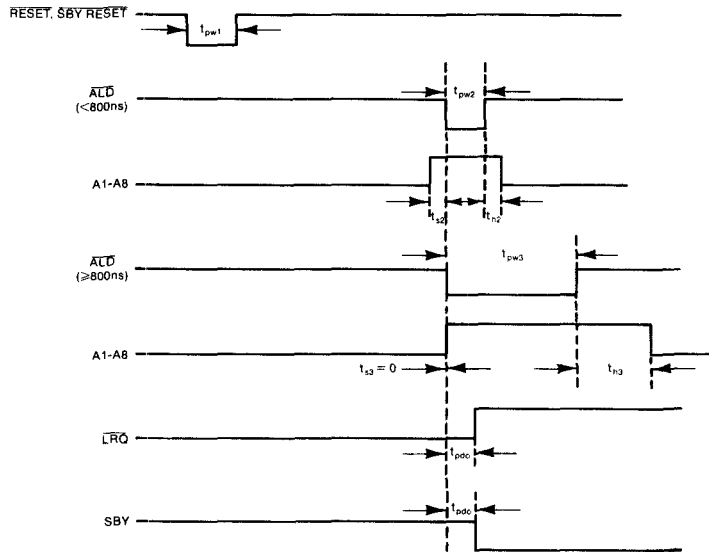
Fig. 1 TIMING DIAGRAM

PIN FUNCTIONS

| Pin Number	Name	Function
1	V_{SS}	Ground
2	$\overline{RESET}$	A logic 0 resets the SP. Must be returned to a logic 1 for normal operation.
3	ROM DISABLE	For use with an external serial speech ROM. A logic 1 disables the external ROM.
4,5,6	C1,C2,C3	Output control lines used by an external serial speech ROM.
7	V_{DD}	Primary power supply.
8	SBY	STANDBY. A logic 1 output indicates that the SP is inactive (i.e., not talking) and V_{DD} can be powered down externally to conserve power. When the SP is reactivated by an address being loaded, SBY will go to a logic 0.
9	$\overline{LRQ}$	LOAD REQUEST. $\overline{LRQ}$ is a logic 1 output whenever the input buffer is full. When $\overline{LRQ}$ goes to a logic 0, the input port is loaded by placing the 8 address bits on A1-A8 and pulsing the $\overline{ALD}$ input.
10,11,13,14, 15,16,17,18	A8,A7,A6,A5, A4,A3,A2,A1	8-bit address which defines any one of 256 speech entry points.
12	SER OUT	SERIAL ADDRESS OUT. This output transfers a 16-bit address serially to an external speech ROM.
19	SE	STROBE ENABLE. Normally held in a logic 1 state. When tied to ground, ALD is disabled and the SP will automatically latch in the address on the input bus approximately $1\mu s$ after detecting a logic 1 on any address line.
20	$\overline{ALD}$	ADDRESS LOAD. A negative pulse on this input loads the 8 address bits into the input port. The leading edge of this pulse causes $\overline{LRQ}$ to go high.
21	SER IN	SERIAL IN. This is an 8-bit serial data input from an external speech ROM.
22	TEST	A logic 1 places the SP in test mode. This pin should normally be grounded.
23	V_{D1}	Standby power supply for the interface logic and controller.
24	DIGITAL OUT	Pulse width modulated digital speech output which, when filtered by a 5kHz low pass filter and amplified, will drive a loudspeaker.
25	$\overline{SBY\ RESET}$	STANDBY RESET. A logic 0 resets the interface logic. Normally should be a logic 1.
26	ROM CLOCK	1.56MHz clock for an external serial speech ROM.
27	OSC 1	XTAL IN. Input connection for a 3.12MHz crystal.
28	OSC 2	XTAL OUT. Output connection for a 3.12MHz crystal.

AUDIO
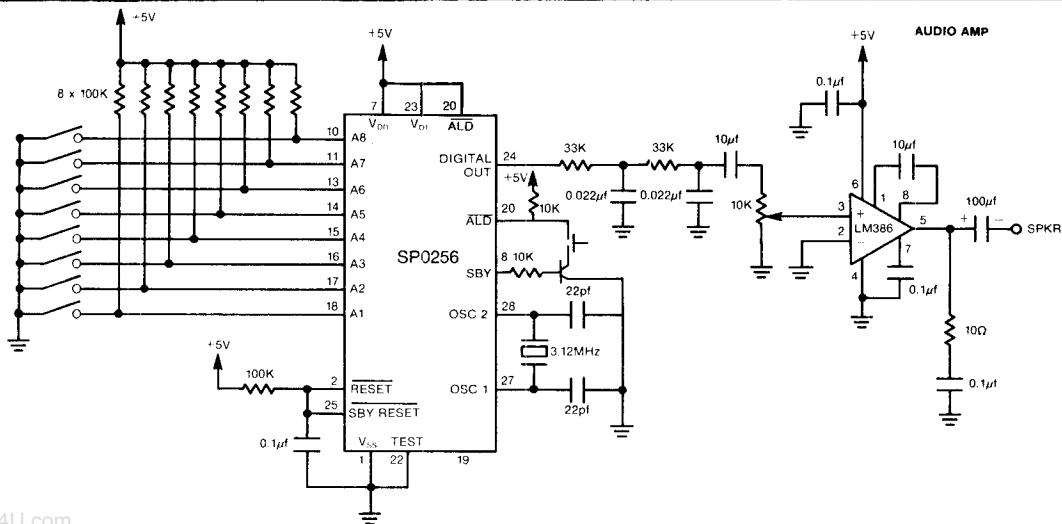
Fig. 2 TYPICAL APPLICATION STAND ALONE CONFIGURATION

MICROCOMPUTER   SPEECH PROCESSOR   EXTERNAL SERIAL SPEECH ROM (OPTIONAL)
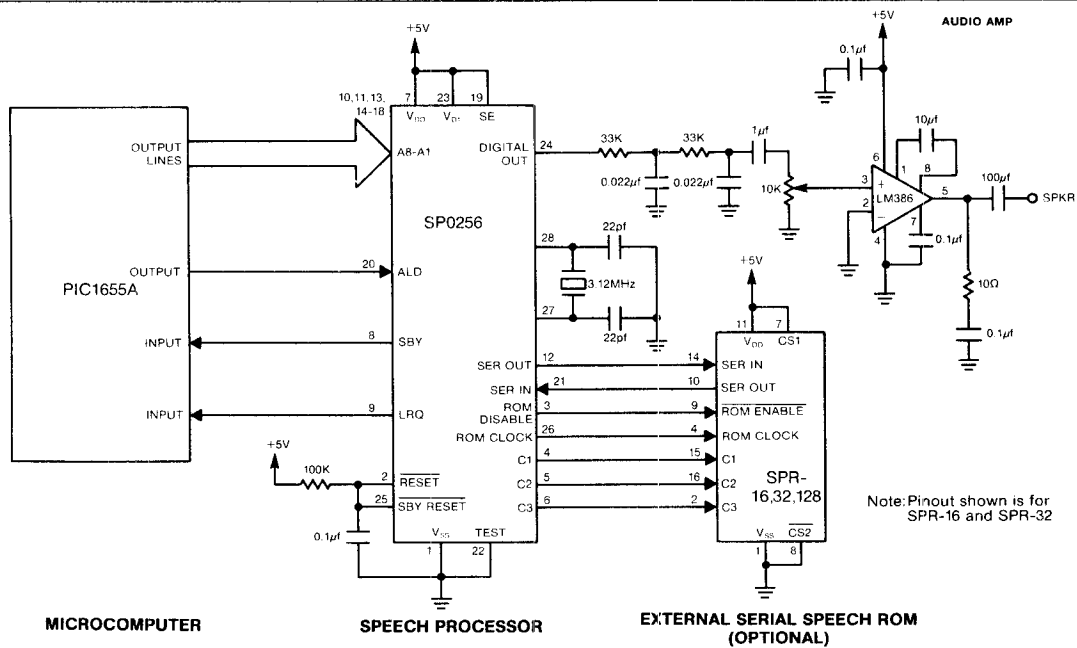
Fig. 3 TYPICAL APPLICATION MICROCOMPUTER INTERFACE

AUDIO

GENERAL INSTRUMENT **SP0256-AL2**

Allophone Based Speech Processor

DESCRIPTION
This product is the SP0256 Speech Processor preprogrammed with a standard ROM Pattern containing 64 allophones. Through the concatenation of selected allophones the user can construct any word in the English language, thereby providing an unlimited vocabulary at a data rate of less than 100 bits/second.

DATA MANUAL
A complete description of the SP0256-AL2 is contained in the Allophone Speech Synthesis Manual.

GENERAL INSTRUMENT **†SP0232**

32K Speech Processor

DESCRIPTION
This product is pin for pin compatible with the SP0256 Speech Processor. This enhanced version of the SP0256 contains 32K of internal ROM.

†For future release.

GENERAL INSTRUMENT **SPR000**

Speech Interface Chip

DESCRIPTION
The SPR000 is designed to interface a standard ROM, PROM, or EPROM to the SP0256 Speech Processor to provide a large amount of vocabulary expansion. This interface contains all the logic necessary to allow data communication under control of the Speech Processor. Two chip selects are provided, (CS1 and CS2), for use in systems where it is desirable to bank blocks of memory under external control. With the capability of addressing 64K bytes of memory the SPR000 is ideal for applications such as SP0256 testing, and speech ROM emulation.

AUDIO