



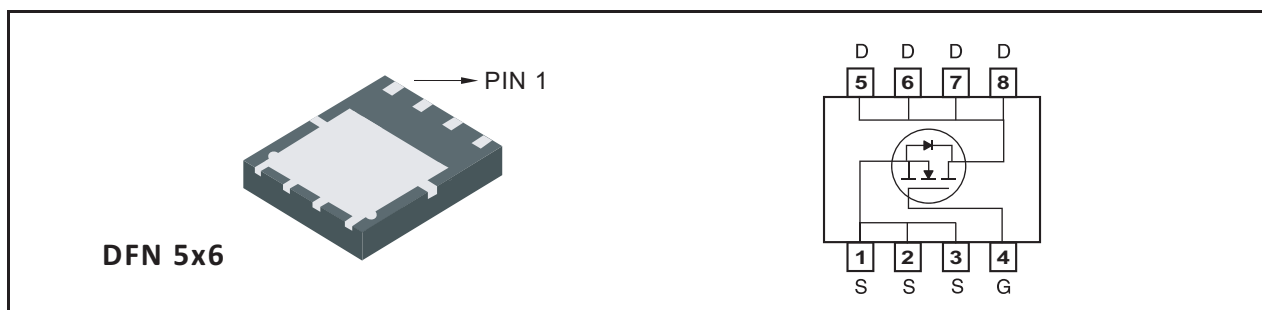
N-Channel Logic Level Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY

V _{DSS}	I _D	R _{DS(ON)} (Ω) Max
650V	1A	1.68 @ V _{GS} =10V

FEATURES

- Super high dense cell design for low R_{DS(ON)}.
- Rugged and reliable.
- Surface Mount Package.



ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

Symbol	Parameter	Limit	Units
V _{DS}	Drain-Source Voltage	650	V
V _{GS}	Gate-Source Voltage	±20	V
I _D	Drain Current-Continuous ^{a c}	T _A =25°C	1
		T _A =70°C	0.8
I _{DM}	-Pulsed ^c	3.5	A
P _D	Maximum Power Dissipation ^a	T _A =25°C	3.1
		T _A =70°C	2
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C

THERMAL CHARACTERISTICS

R _{θJA}	Thermal Resistance, Junction-to-Ambient	40	°C/W
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SP07N65

Ver 1.0

ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =250uA	650			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =520V , V _{GS} =0V			1	uA
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±30V , V _{DS} =0V			±100	nA
ON CHARACTERISTICS						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	2	2.8	4	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V , I _D =0.5A		1.34	1.68	ohm
g _{FS}	Forward Transconductance	V _{DS} =10V , I _D =0.5A		2.3		S
DYNAMIC CHARACTERISTICS ^b						
C _{iss}	Input Capacitance	V _{DS} =25V,V _{GS} =0V f=1.0MHz		902		pF
C _{oss}	Output Capacitance			90		pF
C _{rSS}	Reverse Transfer Capacitance			11		pF
SWITCHING CHARACTERISTICS ^b						
t _{D(ON)}	Turn-On Delay Time	V _{DD} =325V I _D =0.5A V _{GS} =10V R _{GEN} = 6 ohm		30		ns
t _r	Rise Time			16.5		ns
t _{D(OFF)}	Turn-Off Delay Time			52		ns
t _f	Fall Time			39		ns
Q _g	Total Gate Charge	V _{DS} =325V,I _D =0.5A,V _{GS} =10V		16.5		nC
Q _{gs}	Gate-Source Charge	V _{DS} =325V,I _D =0.5A, V _{GS} =10V		2.7		nC
Q _{gd}	Gate-Drain Charge			6		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
V _{SD}	Diode Forward Voltage	V _{GS} =0V,I _S =2A		0.78	1.2	V

Notes

- a.Surface Mounted on FR4 Board of 1 inch² , 1oz.
- b.Guaranteed by design, not subject to production testing.
- c.Drain current limited by maximum junction temperature.

May,26,2014

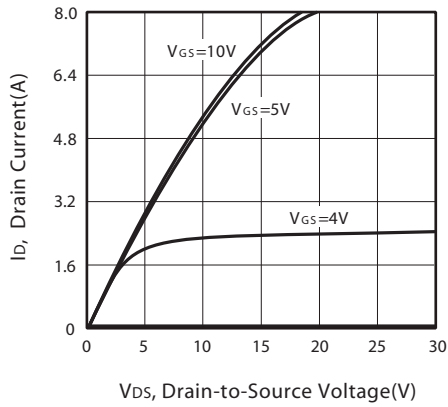


Figure 1. Output Characteristics

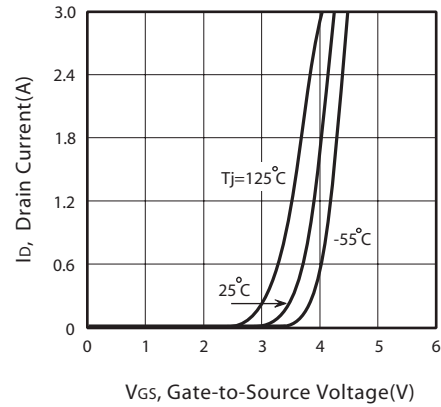


Figure 2. Transfer Characteristics

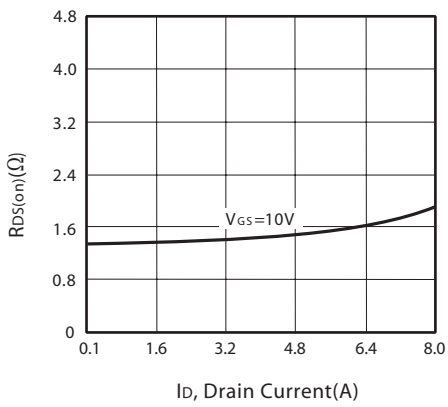


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

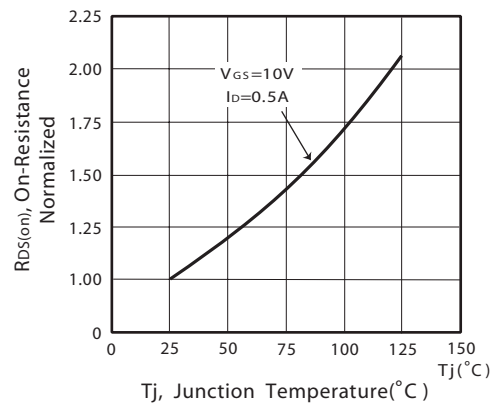


Figure 4. On-Resistance Variation with Drain Current and Temperature

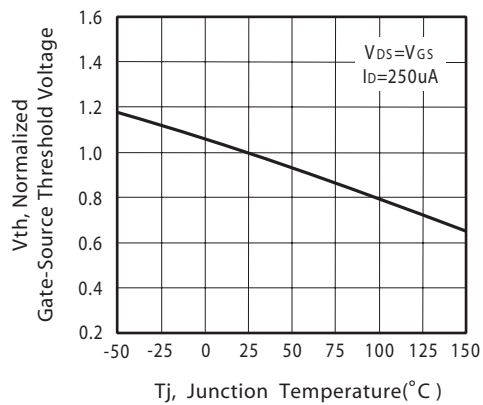


Figure 5. Gate Threshold Variation with Temperature

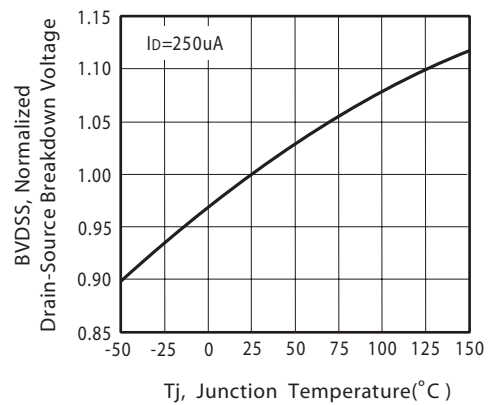


Figure 6. Breakdown Voltage Variation with Temperature

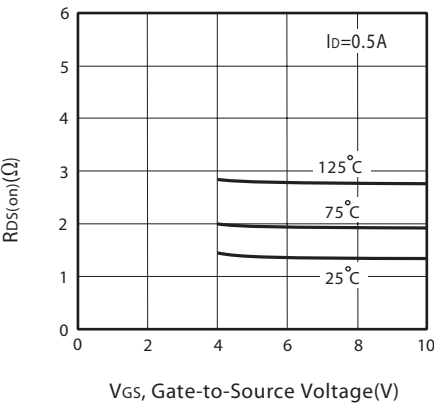


Figure 7. On-Resistance vs. Gate-Source Voltage

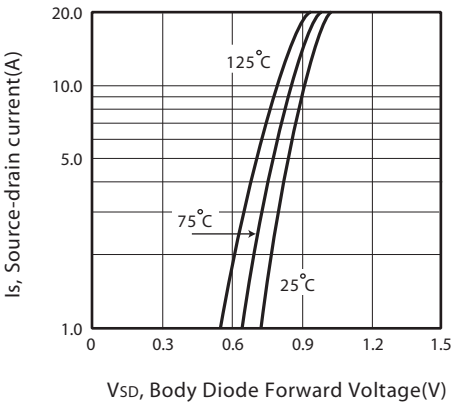


Figure 8. Body Diode Forward Voltage Variation with Source Current

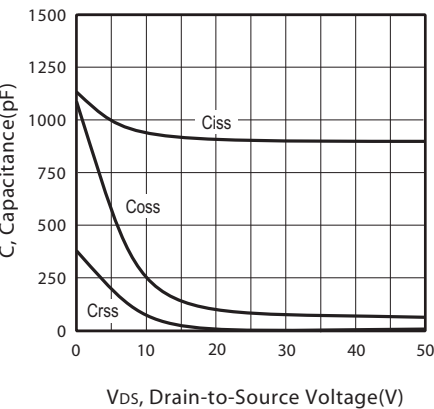


Figure 9. Capacitance

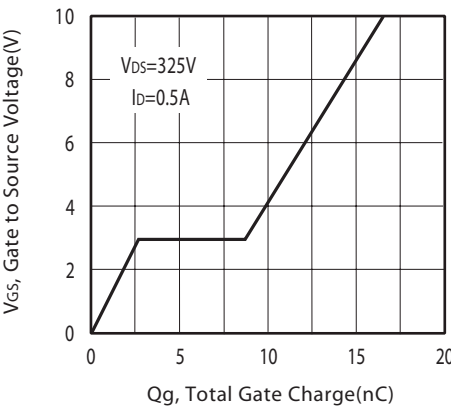


Figure 10. Gate Charge

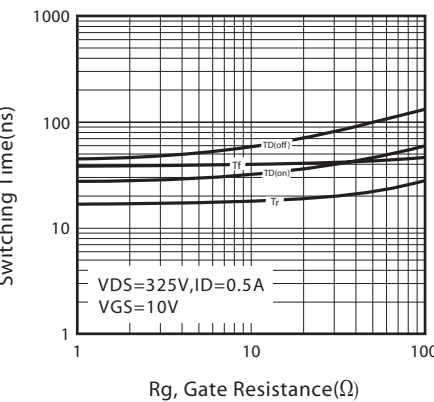


Figure 11. switching characteristics

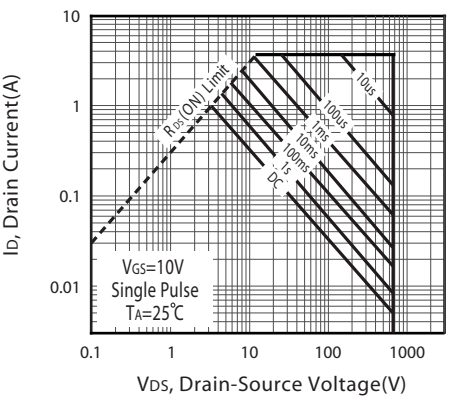
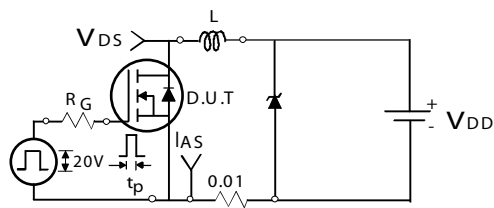
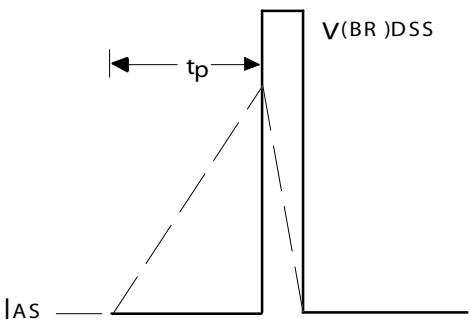


Figure 12. Maximum Safe Operating Area



Unclamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

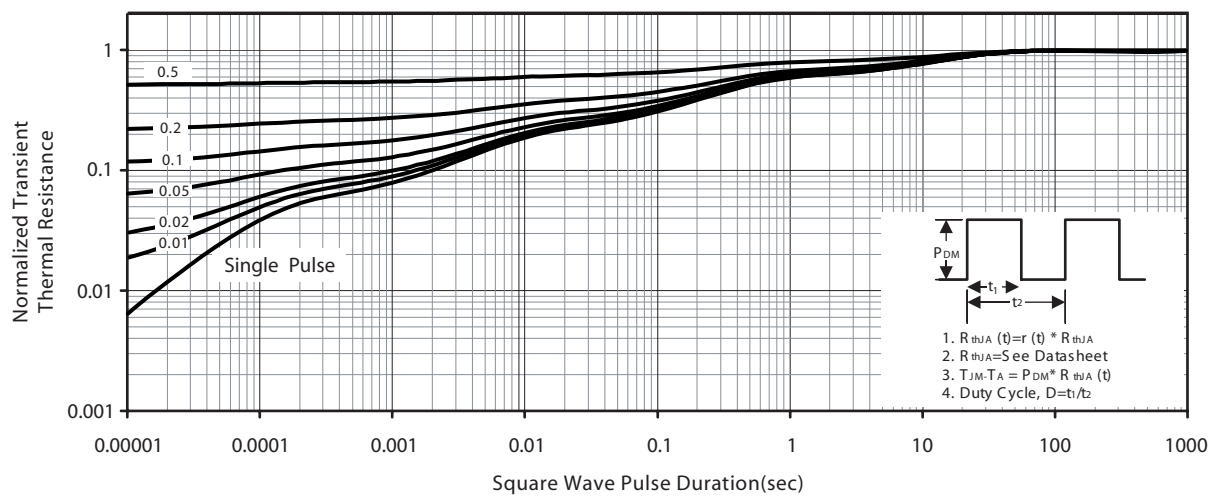
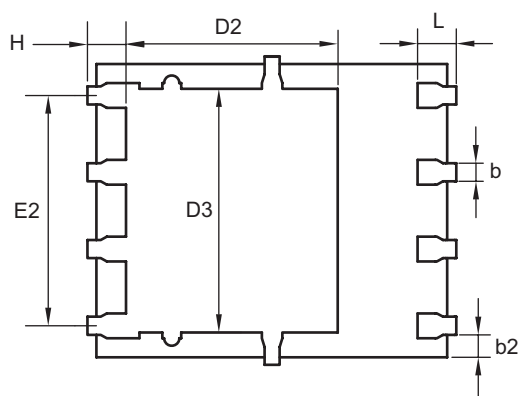
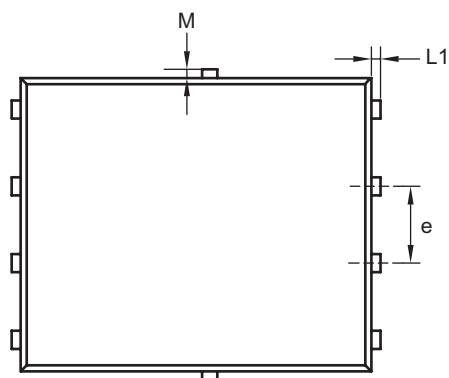


Figure 13. Normalized Thermal Transient Impedance Curve

PACKAGE OUTLINE DIMENSIONS

DFN 5x6



SYMBOLS	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
b	0.20	0.30	0.40
b2	0.25	0.35	0.45
C	0.15	0.25	0.35
D	5.90	6.10	6.30
D1	5.60	5.80	6.00
D2	3.50 REF.		
D3	4.00 REF.		
E	5.00	5.20	5.40
E1	4.70	4.90	5.10
E2	3.61	3.81	4.01
e	1.17	1.27	1.37
H	0.63 REF.		
L	0.53	0.63	0.73
L1	0.05	0.15	0.25
M	0.05	0.15	0.25
θ	8°	10°	12°

