

# HITACHI

FOR MESSRS: \_\_\_\_\_

DATE : Oct.31,2007

## CUSTOMER'S ACCEPTANCE SPECIFICATIONS

### SP09Q02L0CLZZ

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\* When product will be discontinued, customer will be informed by HITACHI with twelve months prior to discontinuation.

\* This product is inhibited to apply in any life support instrument.

ACCEPTED BY: \_\_\_\_\_

PROPOSED BY: Dan Cheng

|                                           |            |                              |      |       |
|-------------------------------------------|------------|------------------------------|------|-------|
| KAOHSIUNG HITACHI<br>ELECTRONICS CO.,LTD. | Sh.<br>No. | 7B64PS 2701- SP09Q02L0CLZZ-1 | PAGE | 1-1/1 |
|-------------------------------------------|------------|------------------------------|------|-------|

## RECORD OF REVISION

| DATE | SHEET No. | SUMMARY |
|------|-----------|---------|
|      |           |         |

KAOHSIUNG HITACHI  
ELECTRONICS CO.,LTD.

DATE

Oct.31,'07

Sh.  
No.

7B64PS 2702- SP09Q02L0CLZZ-1

PAGE

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### 3. GENERAL SPECIFICATIONS

|                        |                                                                                          |
|------------------------|------------------------------------------------------------------------------------------|
| (1) Part Name          | SP09Q02L0CLZZ                                                                            |
| (2) Module Size        | 89.0 (W)mm x 66.5 (H)mm x 5.5 (D)mm                                                      |
| (3) Active Area        | 71.985(W)mm x 47.985(H)mm                                                                |
| (4) Dot Size           | 0.30 (W)mm x 0.30 (H)mm                                                                  |
| (5) Dot Pitch          | 0.285 (W)mm x 0.285 (H)mm                                                                |
| (6) Resolution         | 240 (W) x 160 (H) dots                                                                   |
| (7) Duty Ratio         | 1/160                                                                                    |
| (8) Bias Ratio         | 1/9                                                                                      |
| (9) LCD Type           | Transmissive type B/W F-STN (Negative Mode)<br>with anti-glare type upper polarizer      |
| (10) Viewing Direction | 12 O'clock                                                                               |
| (11) Backlight         | White LED<br>Life time : 35khr @25°C<br>Note : Life time for half of initial brightness. |

#### 4. ABSOLUTE MAXIMUM RATINGS

##### 4.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS.

VSS=0V:STANDARD

| ITEM                      | SYMBOL  | MIN. | MAX.    | UNIT | COMMENT    |
|---------------------------|---------|------|---------|------|------------|
| Power Supply for Logic    | VDD-VSS | -0.3 | 7.0     | V    |            |
| Power Supply for LC Drive | VLCD    | 0    | 30.0    | V    |            |
| Input Voltage             | Vi      | -0.3 | VDD+0.3 | V    | (Note 1,2) |

Note 1 :  $\overline{\text{DOFF}}$  , FLM , CL1, CL2 , D0~D3 , M.

Note 2 : Make certain you are grounded when handling LCM.

##### 4.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS.

| I T E M             | OPERATING      |                                 | STORAGE        |                                             | COMMENT              |
|---------------------|----------------|---------------------------------|----------------|---------------------------------------------|----------------------|
|                     | MIN.           | MAX.                            | MIN.           | MAX.                                        |                      |
| Ambient Temperature | 0°C            | 70°C                            | -20°C          | 80°C                                        | (Note 2,3,6)         |
| Humidity            | (Note 1)       |                                 | (Note 1)       |                                             | Without condensation |
| Vibration           | -              | 2.45m/s <sup>2</sup><br>(0.25G) | -              | 11.76m/s <sup>2</sup><br>(1.2G)<br>(Note 5) | 1h max.<br>(Note 4)  |
| Shock               | -              | 29.4m/s <sup>2</sup><br>(3 G)   | -              | 490.0m/s <sup>2</sup><br>(50 G)<br>(Note 5) | X · Y · Z Directions |
| Corrosive Gas       | Not acceptable |                                 | Not acceptable |                                             |                      |

Note 1 : Ta ≤ 40°C : 85%RH max.

Ta > 40°C : Absolute humidity must be lower than the humidity of 85%RH at 40°C

Note 2 : Ta at -20°C < 48h , at 80°C < 168h.

Note 3 : Background color changes slightly depending on ambient temperature.  
This phenomenon is reversible.

Note 4 : 5Hz~100Hz (Except resonance frequency)

Note 5 : This module should be operated normally after finish the test.

Note 6 : The operating temperature only guarantee the display can be operated ; regarding the contrast , response time , brightness and other features related to the quality are judged by Ta=25°C condition .

## 5. ELECTRICAL CHARACTERISTICS

### 5.1 ELECTRICAL CHARACTERISTICS OF LCD

| I T E M                                        | SYMBOL   | CONDITION                        | MIN.   | TYP. | MAX.   | UNIT |
|------------------------------------------------|----------|----------------------------------|--------|------|--------|------|
| Power Supply Voltage for Logic                 | VDD-VSS  | -                                | 2.5    | 3.3  | 4.5    | V    |
| Power Supply Voltage for LCD Driving           | VLCD-VSS | -                                | -      | -    | 30.0   | V    |
| Input Voltage (Note 1)                         | Vi       | H level                          | 0.8VDD | -    | VDD    | V    |
|                                                |          | L level                          | 0      | -    | 0.2VDD | V    |
| Power Supply Current For Logic , (Note 2)      | IDD      | VDD-VSS=3.3V<br>VLCD-VSS=(16.2)V | -      | 0.02 | -      | mA   |
| Power Supply Current for LC Driving , (Note 2) | ILCD     | VDD-VSS=3.3V<br>VLCD-VSS=(16.2)V | -      | 0.1  | -      | mA   |
| Recommended LC Driving Voltage (Note 3)        | VLCD-VSS | Ta= 0°C , $\phi=0^\circ$         | -      | 17.2 | -      | V    |
|                                                |          | Ta=25°C , $\phi=0^\circ$         | -      | 16.2 | -      | V    |
|                                                |          | Ta=50°C , $\phi=0^\circ$         | -      | 15.2 | -      | V    |
| Frame Frequency (Note 4)                       | fFLM     | -                                | 70     | 75   | 80     | Hz   |

Note 1 :  $\overline{\text{DOFF}}$  , FLM , CL1 , CL2, D0~D3,M.

Note 2 : fFLM=75Hz , Test pattern is all "Q".

VLCD-VSS=16.2V, Ta=25°C.

Note 3 : Recommended LC driving voltage change about  $\pm 1.0\text{V}$  by each module.  
Test pattern is all "Q".

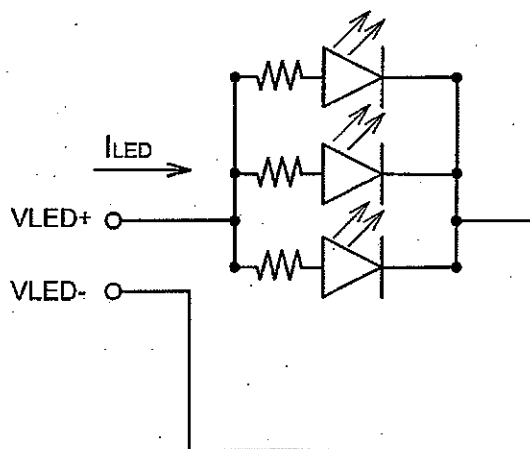
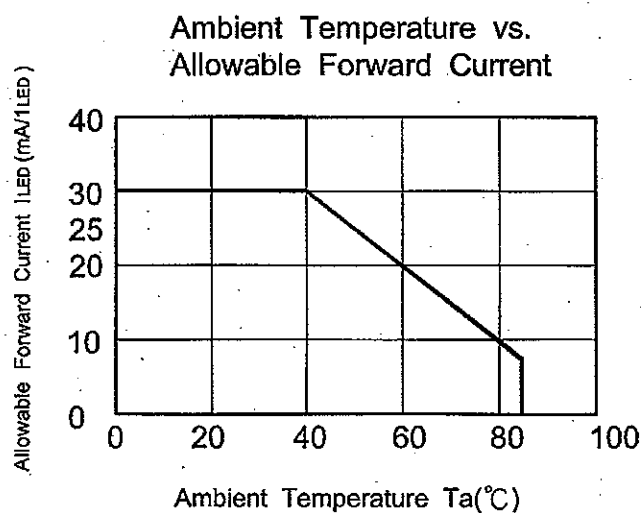
Note 4 : Need to make sure of flicking and rippling of display when setting the frame frequency in your set.

## 5.5 ELECTRICAL CHARACTERISTICS OF LED BACKLIGHT

$T_a=25^{\circ}\text{C}$  (Backlight on)

| ITEM                         | SYMBOL | CONDITION | MIN. | TYP. | MAX.           | UNIT |
|------------------------------|--------|-----------|------|------|----------------|------|
| Power Supply Voltage for LED | VLED   | -         | -    | 5.0  | 5.2            | V    |
| Power Supply Current for LED | ILED   | VLED=5.0V | -    | (60) | 75<br>(Note 1) | mA   |

Note 1 : The ILED changes depending on ambient temperature.



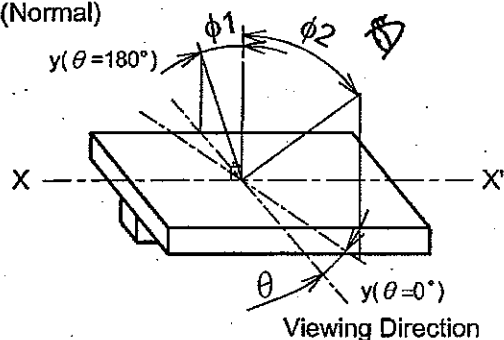
## 6. OPTICAL CHARACTERISTICS

### 6.1 OPTICAL CHARACTERISTICS OF LCD

Ta=25°C (Backlight on)

| ITEM                 | SYMBOL            | CONDITION                          | MIN. | TYP. | MAX. | UNIT | NOTE |
|----------------------|-------------------|------------------------------------|------|------|------|------|------|
| Viewing Angle        | $\phi_2 - \phi_1$ | $K \geq 2.0$                       | -    | 80   | -    | deg. | 1,2  |
| Contrast Ratio       | K                 | $\phi = 0^\circ, \theta = 0^\circ$ | -    | 30   | -    | -    | 3    |
| Response Time (Rise) | tr                | $\phi = 0^\circ, \theta = 0^\circ$ | -    | 150  | -    | ms   | 4    |
| Response Time (Fall) | tf                | $\phi = 0^\circ, \theta = 0^\circ$ | -    | 350  | -    | ms   | 4    |

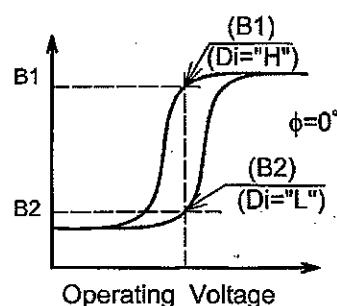
Note 1 : Definition of  $\theta$  and  $\phi$   
(Normal)



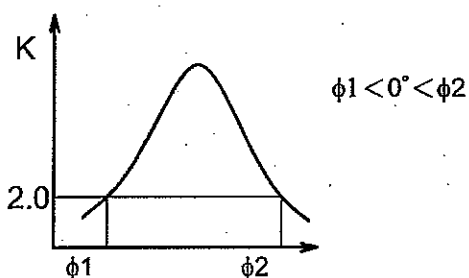
(Measure condition by HITACHI)

Note 3 : Definition of contrast "K"

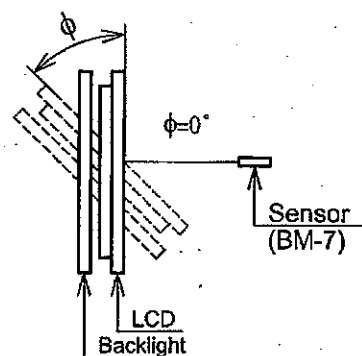
$$K = \frac{\text{Brightness on selected dot (B1)}}{\text{Brightness on non-selected dot (B2)}}$$



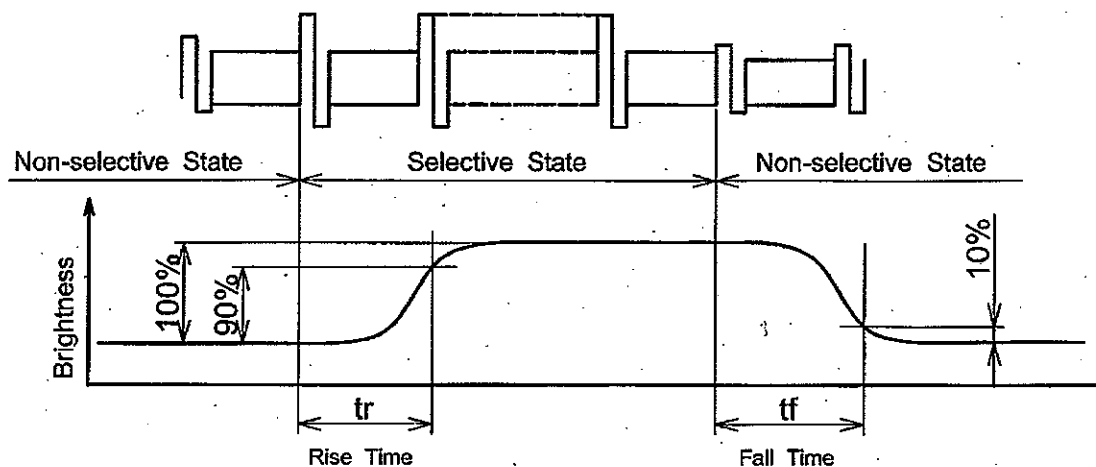
Note 2 : Definition of viewing angle  $\phi_1$  and  $\phi_2$



Contrast ratio K vs viewing angle  $\phi$



Note 4 : Definition of optical response

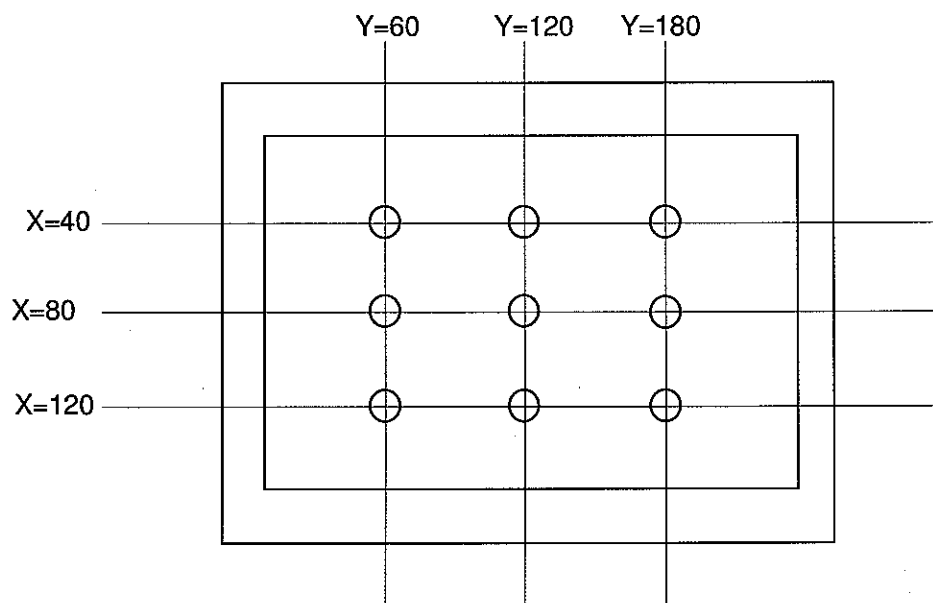


## 6.2 OPTICAL CHARACTERISTICS OF BACKLIGHT

(LCM, BACKLIGHT ON, Ta=25°C)

| ITEM                  | MIN. | TYP. | MAX. | UNIT              | NOTE                    |
|-----------------------|------|------|------|-------------------|-------------------------|
| Brightness Uniformity | -    | -    | ±35  | %                 | (Note 1,2)              |
| Brightness            | -    | 90   | -    | cd/m <sup>2</sup> | I <sub>LED</sub> =60 mA |

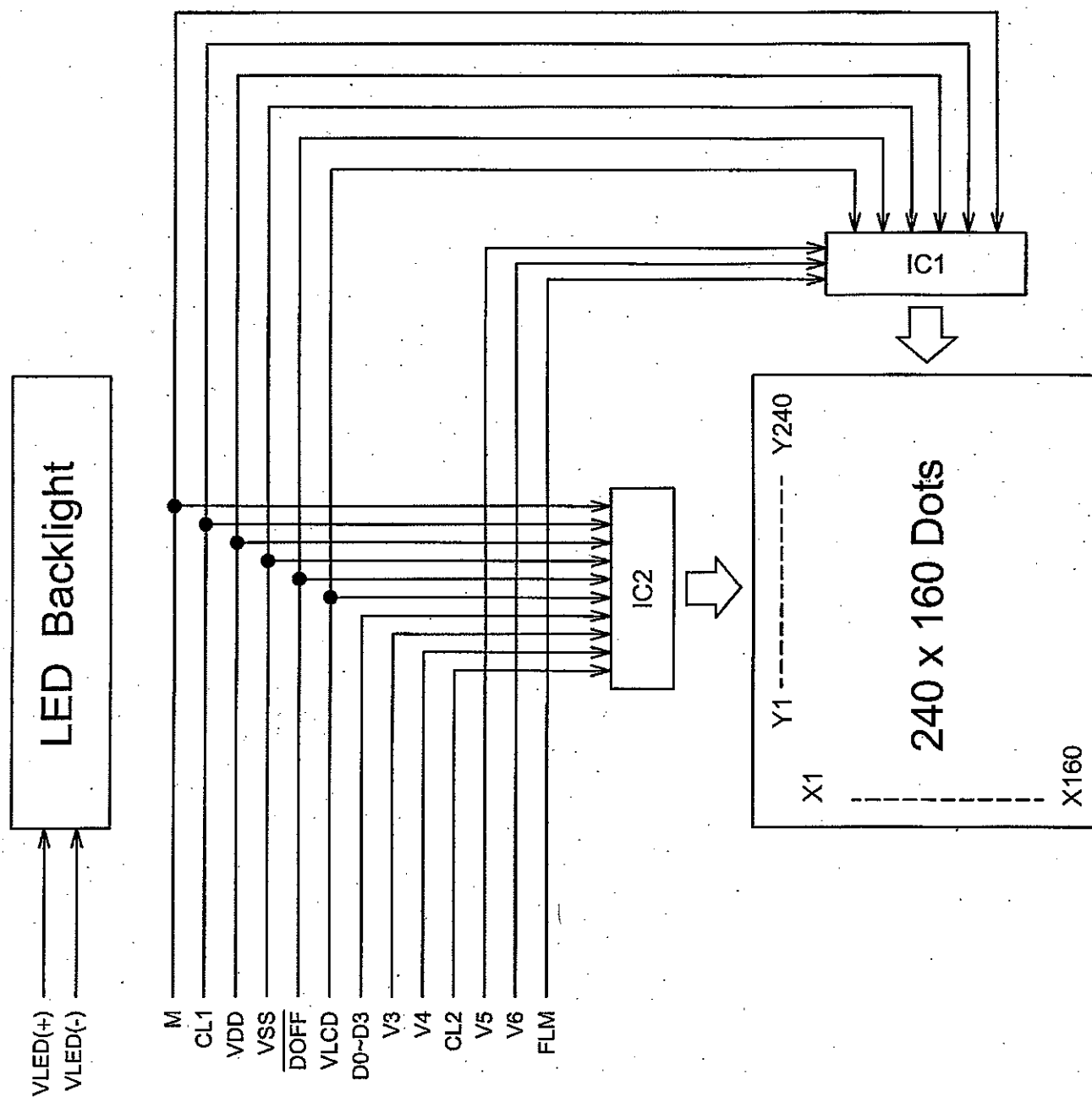
Note 1 : Measure of the following 9 places on the display.



Note 2 : Definition of brightness tolerance.

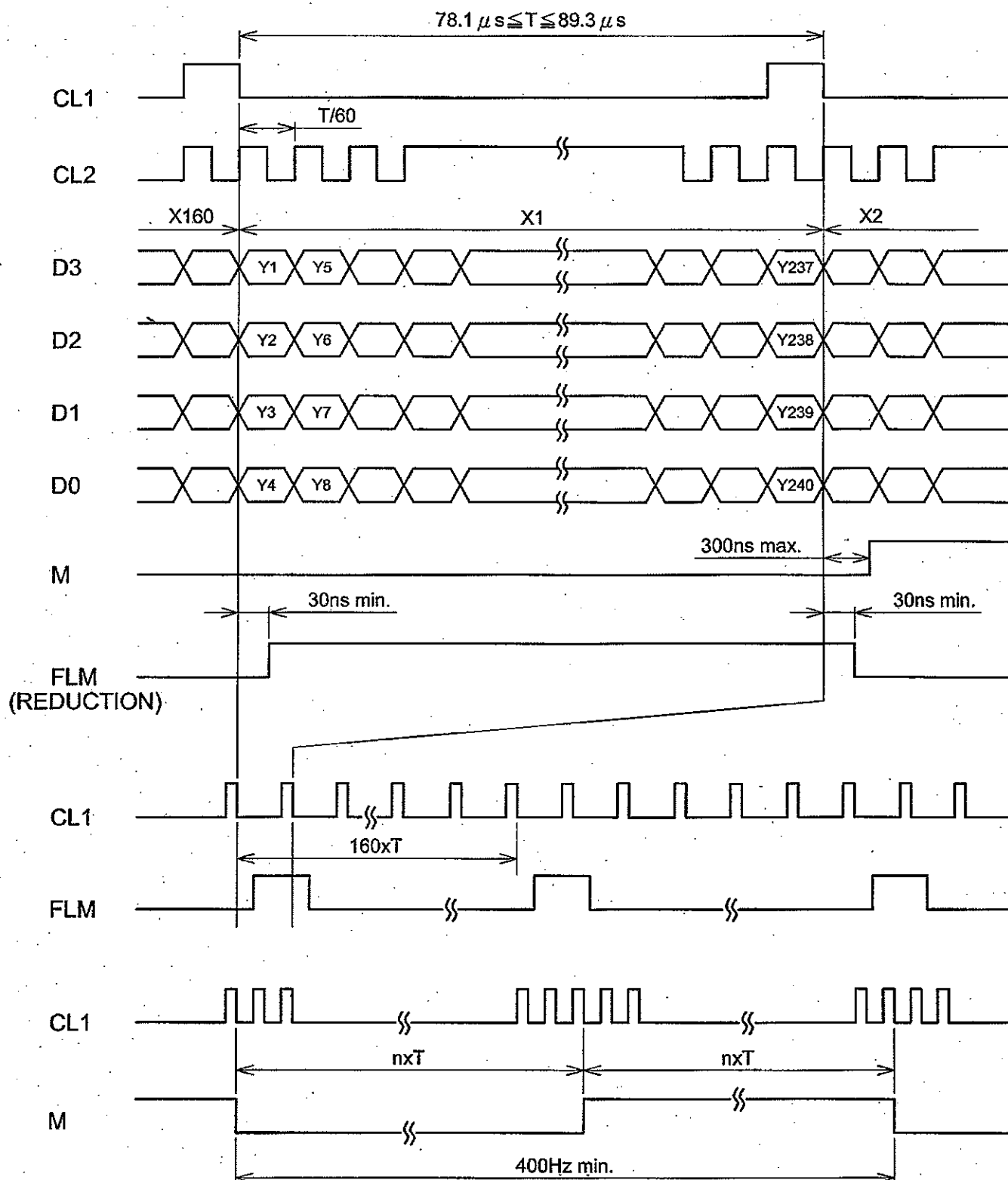
$$\left( \frac{\text{Max. or Min. Brightness} - \text{Average Brightness}}{\text{Average Brightness}} \right) \times 100\%$$

## 7. BLOCK DIAGRAM



## 8. INTERFACE TIMING

### 8.1 TIMING CHART (4-BITS PARALLEL DATA INPUT)



Note 1 : M signal should be kept 400Hz min. and 50% duty.

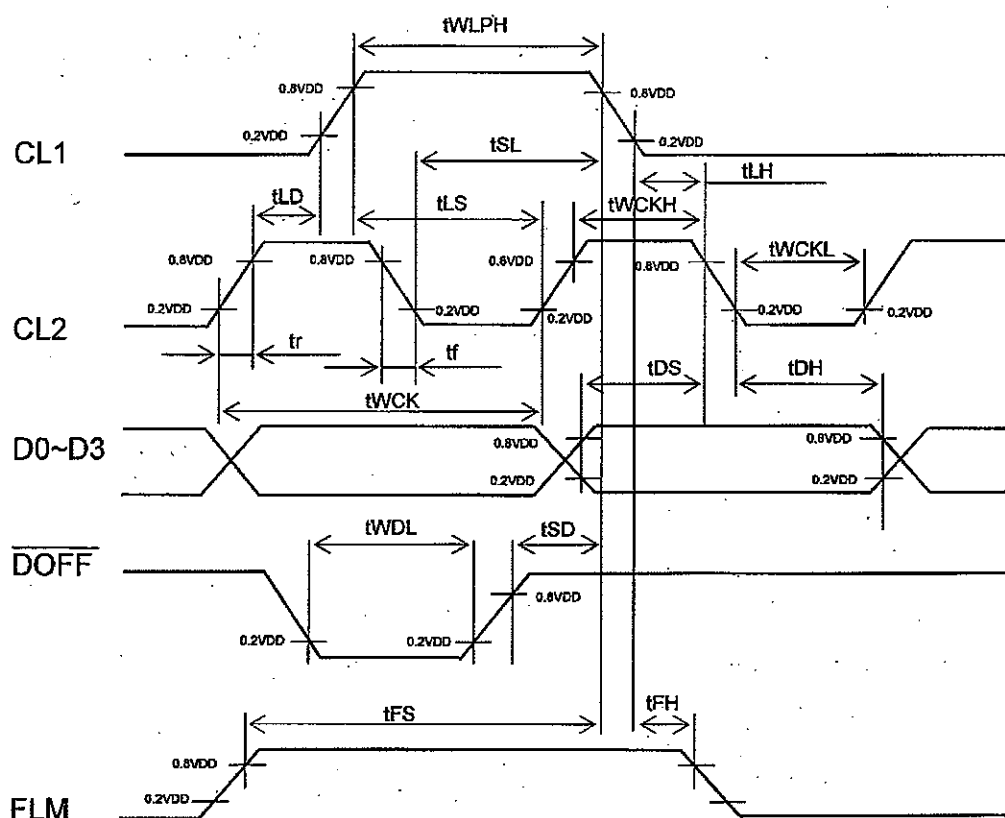
Note 2 : HITACHI recommend  $nxCL1$  pulses of M signal 50%.

$n=13$

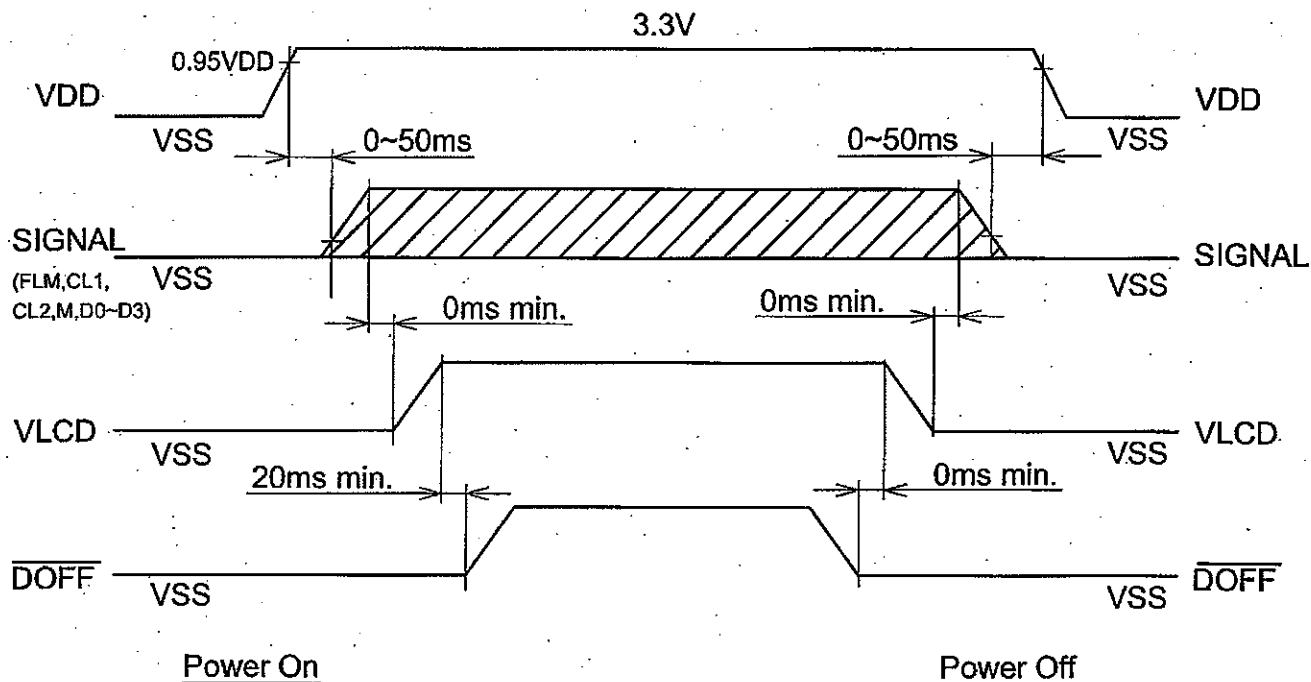
## 8.2 TIMING CHARACTERISTICS

| PARAMETER                                 | SYMBOL | MIN. | TYP. | MAX. | UNIT          | CONDITION                   |
|-------------------------------------------|--------|------|------|------|---------------|-----------------------------|
| Shift Clock Period                        | tWCK   | 125  | -    | -    | ns            | $t_r, t_f \leq 11\text{ns}$ |
| Shift Clock "H" Pulss Width               | tWCKH  | 51   | -    | -    | ns            |                             |
| Shift Clock "L" Pulss Width               | tWCKL  | 51   | -    | -    | ns            |                             |
| Data Setup Time                           | tDS    | 30   | -    | -    | ns            |                             |
| Data Hole Time                            | tDH    | 40   | -    | -    | ns            |                             |
| Latch Pulse "H" Pulse Width.              | tWLPH  | 51   | -    | -    | ns            |                             |
| Shift Clock Rise to Latch Pulse Rise Time | tLD    | 0    | -    | -    | ns            |                             |
| Shift Clock Rise to Latch Pulse Fall Time | tSL    | 51   | -    | -    | ns            |                             |
| Latch Pulse Rise to Shift Clock Rise Time | tLS    | 51   | -    | -    | ns            |                             |
| Latch Pulse Fall to Shift Clock Fall Time | tLH    | 51   | -    | -    | ns            |                             |
| Input Signal Rise Time                    | $t_r$  | -    | -    | 50   | ns            | (Note 1)                    |
| Input Signal Fall Time                    | $t_f$  | -    | -    | 50   | ns            | (Note 1)                    |
| DOFF Removal Time                         | tSD    | 100  | -    | -    | ns            |                             |
| DOFF Enable Pulse Time                    | tWDL   | 1.2  | -    | -    | $\mu\text{s}$ |                             |
| "FLM" Set Up Time                         | tFS    | 100  | -    | -    | ns            | -                           |
| "FLM" Hold Time                           | tFH    | 30   | -    | -    | ns            | -                           |

Note 1 :  $(t_{WCK} - t_{WCKH} - t_{WCKL}) / 2$  is the maximum in the case of high speed operation.



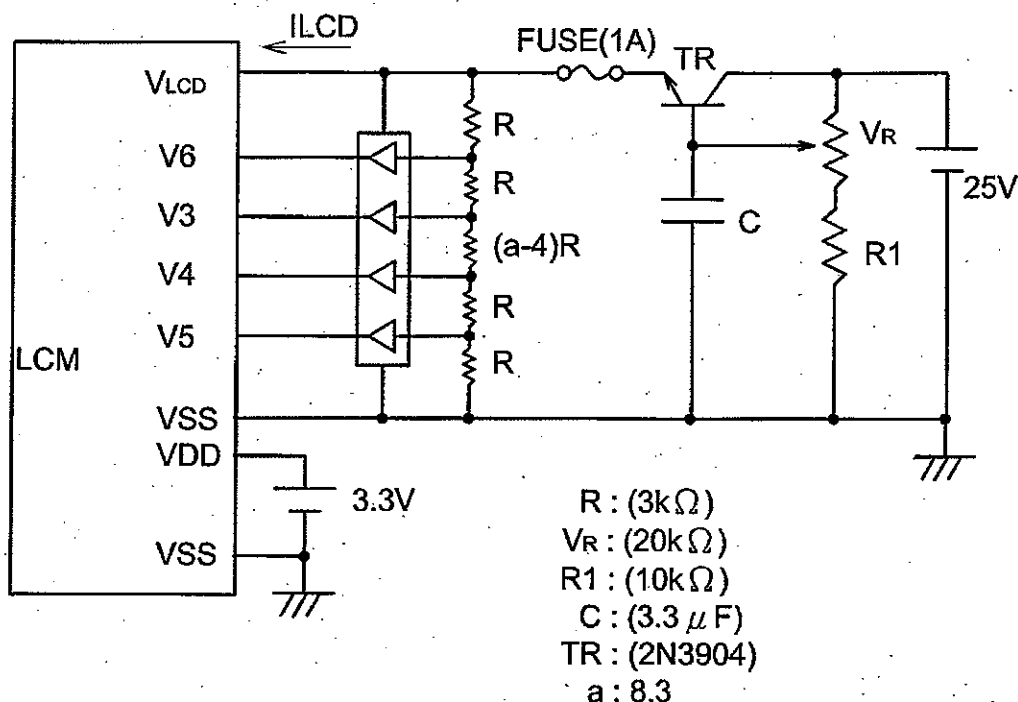
### 8.3 TIMING OF POWER SUPPLY AND INTERFACE SIGNAL



Note 1: DOFF function takes priority even if the input signal status becomes irregular immediately after VDD power-on.

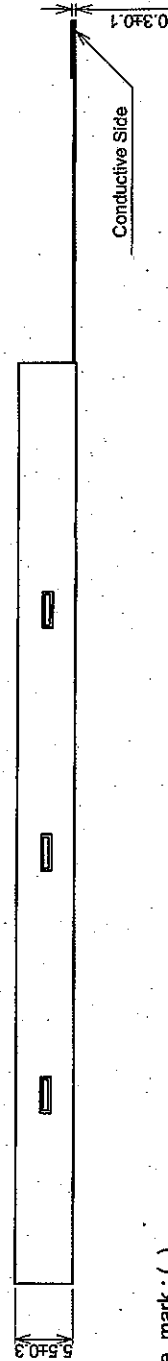
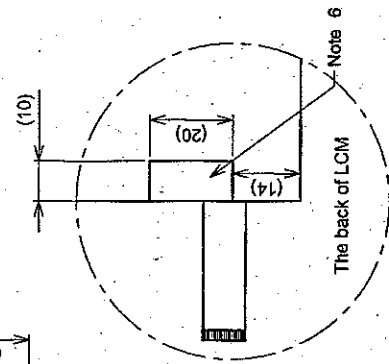
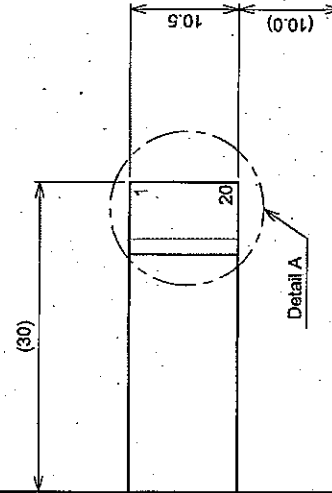
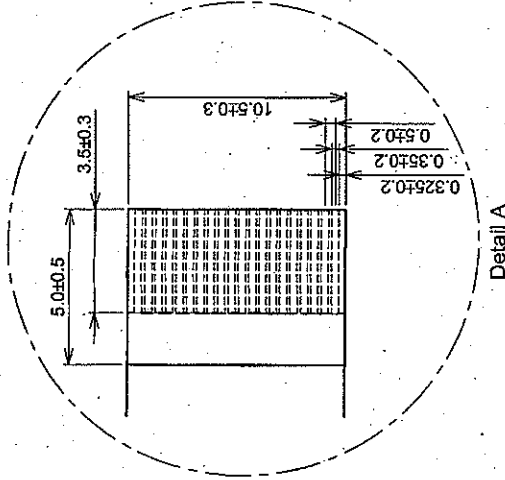
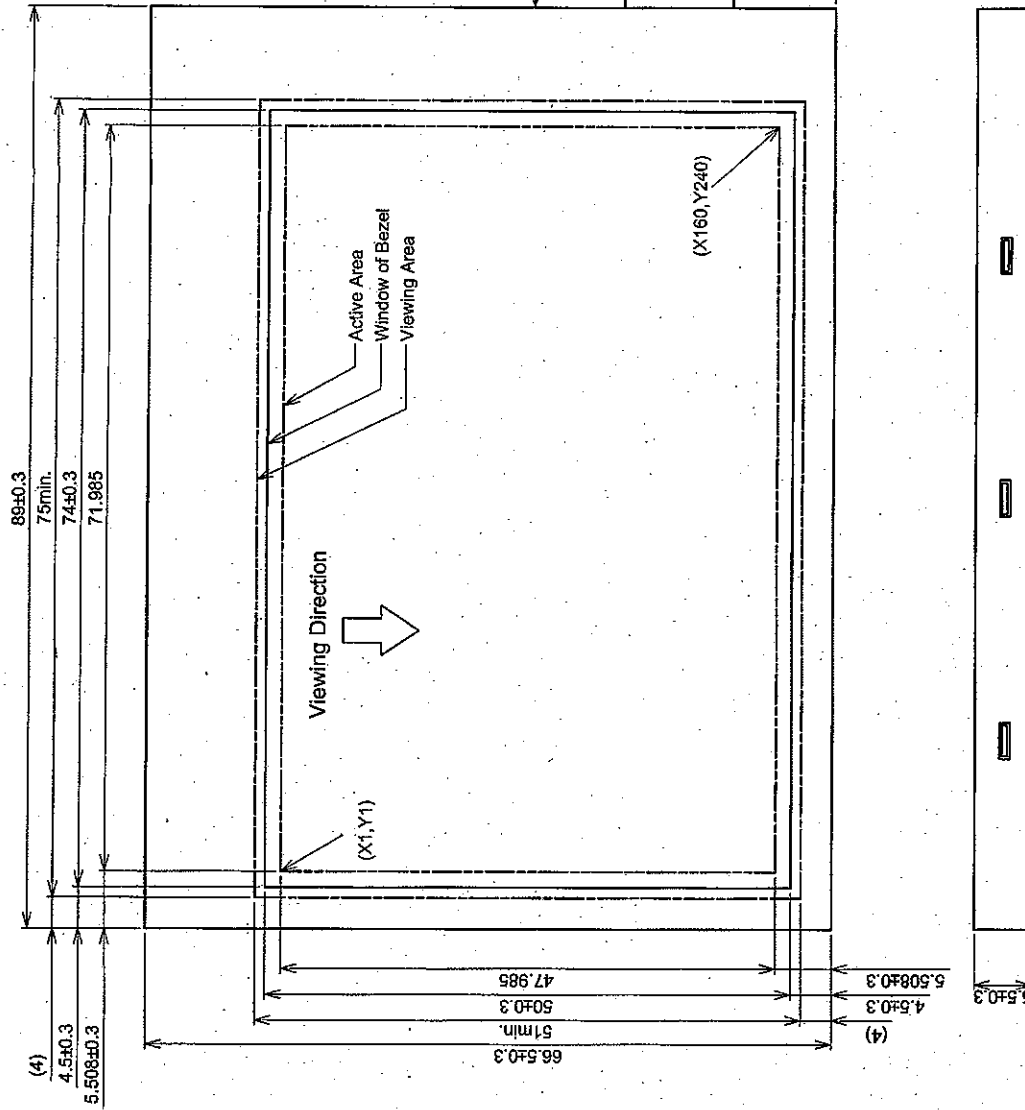
Note 2 : Please keep the specified sequence because wrong sequence may cause permanent damage to the LCM.

## 8.4 POWER SUPPLY FOR LCM



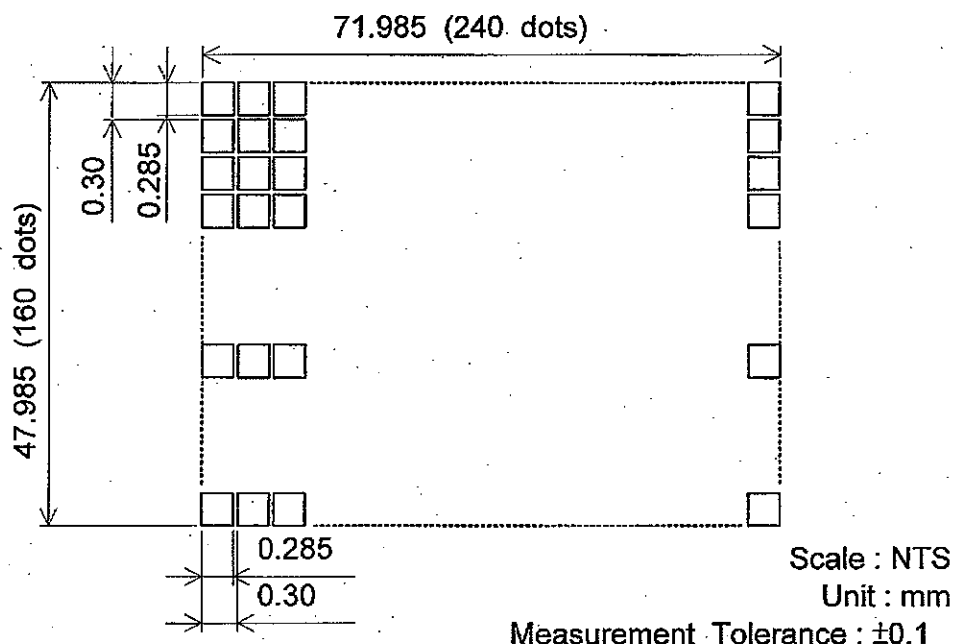
## 9. OUTLINE DIMENSIONS

### 9.1 OUTLINE DIMENSIONS



- Notes:
1. Reference mark : ( )
  2. Unit : mm
  3. Scale : NTS
  4. Unmarked Tolerance : ± 0.3mm
  5. Measurement when adding 9.8x10<sup>-4</sup> Pa at the measuring point
  6. We have 1mm high points of solder at VLED(+) and VLED(-)

## 9.2 DISPLAY PATTERN



## 9.3 INTERFACE PIN CONNECTION

### 9.3.1 CN1 : LCM I/F (0.5mm PITCH , 20PINS FPC)

| PIN No. | SYMBOL  | FUNCTION                                                               |
|---------|---------|------------------------------------------------------------------------|
| 1       | VLED(+) | Power supply for LED backlight                                         |
| 2       | VLED(-) | Power supply for LED backlight                                         |
| 3       | M       | Switch signal to convert LCD driver waveform into AC                   |
| 4       | DOFF    | Hi : Display on ; Low : Display off                                    |
| 5       | FLM     | Frame start signal data signal of the shift register of the Com driver |
| 6       | VLCD    | Power supply for LCD                                                   |
| 7       | V6      | Bias voltage for non-select (Com driver)                               |
| 8       | V3      | Bias voltage for non-select (Seg driver)                               |
| 9       | V4      | Bias voltage for non-select (Seg driver)                               |
| 10      | V5      | Bias voltage for non-select (Com driver)                               |
| 11      | D0      | Input data signal                                                      |
| 12      | D1      | Input data signal                                                      |
| 13      | D2      | Input data signal                                                      |
| 14      | D3      | Input data signal                                                      |
| 15      | VDD     | Power supply for logic                                                 |
| 16      | VSS     | Ground                                                                 |
| 17      | CL1     | 1) Latch pulse of display data<br>2) Shift clock for Com driver        |
| 18      | VSS     | Ground                                                                 |
| 19      | CL2     | Clock pulse for Seg shift                                              |
| 20      | VSS     | Ground                                                                 |

Suitable connector : Molex / 52745-2090 or 52746-2090