PLESSEY
Semiconductors

# SP1450B(B) & SP1455B(B)

## PCM SIGNAL MONITOR CIRCUITS

The SP1450 and SP1455 are bipolar integrated circuits designed to monitor errors in three-level digital signals modulated by a three-alphabet 4B3T code such as MS43. They can also indicate the failure of positive or negative pulses in the signal. The high frequency capability allows operation in PCM systems up to 34M bit/s (SP1450) and 140M bit/s (SP1455). Facilities are provided to adjust input thresholds independently on each polarity of input and the error output can be interfaced with low speed CMOS circuitry or high speed ECL.

The SP1450B(B) and SP1455B(B) are similar to the SP1450B and SP1455B but are screened to MIL-STD-883, Method 5004, Class B.

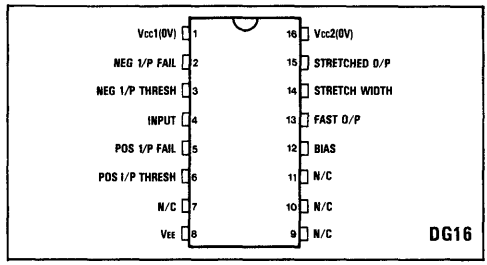


*Fig.1 Pin connections (top view)*

### FEATURES

- Suitable for 34, 120 and 140M bit/s PCM
- Positive and Negative Input Signal Fail Outputs
- High Speed Error Output
- Low Speed 'Stretched' Output
- Low Power Consumption

### APPLICATIONS

- PCM Telephone Transmission Terminal Equipment
- PCM Repeaters
- Error Checking Test Equipment

### QUICK REFERENCE DATA

- Supply Voltage -4.4V to -5.25V
- Operating Temperature Range -10°C to +70°C
- Power Consumption 100mW typ
- Input Voltage Range ±450mV to ±1100mV (SP1450)
  ±450mV to ±600mV (SP1455)
- Thermal Resistance θj-a 100°C/W

### ABSOLUTE MAXIMUM RATINGS

Supply voltage -8V
Reverse input current (pin 4) 5mA (continuous) 20mA (10us max)
Forward input current (pin 4) 20mA (10us max)
Storage temperature -55°C to +150°C
Operating temperature -10°C to +70°C
Junction temperature 150°C

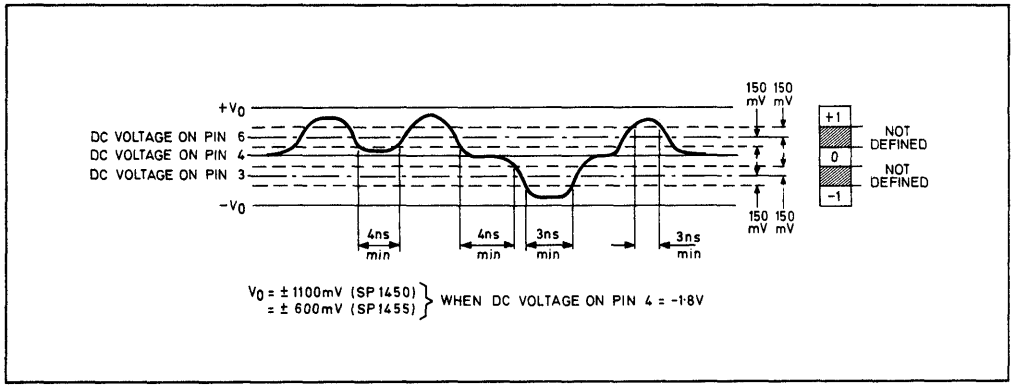


*Fig.2 Input pulse wave form*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$V_{CC}$ = Pins 1-16 = 0V
$V_{EE}$ = Pin 8 = -5.0V
$T_{amb}$ = +25°C
Input voltage range (pins 3,4,6) = -0.9V to -3.1V

### DC CHARACTERISTICS

| Characteristic | Pin | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output low, current | 2 | 0.9 | 1.2 | 1.9 | mA | Pin 2 = OV<br>Pin 3 = —1.7V<br>Pin 4 = —2.0V |
| Output low, current | 2 | 0.7 | — | — | mA | Pin 2 = OV<br>Pin 3 = —1.95V<br>Pin 4 = —2.0V |
| Output high, current | 2 | — | — | 1 | µA | Pin 2 = OV<br>Pin 3 = —2.3V<br>Pin 4 = —2.0V |
| Output high, current | 2 | — | — | 0.4 | mA | Pin 2 = OV<br>Pin 3 = —2.05V<br>Pin 4 = —2.0V |
| Output low, current | 5 | 0.9 | 1.2 | 1.9 | mA | Pin 4 = —2.0V<br>Pin 5 = OV<br>Pin 6 = —2.3V |
| Output low, current | 5 | 0.7 | — | — | mA | Pin 4 = —2.0V<br>Pin 5 = OV<br>Pin 6 = —2.05V |
| Output high, current | 5 | — | — | 1 | µA | Pin 5 = OV<br>Pin 4 = —2.0V<br>Pin 6 = —1.7V |
| Output high, current | 5 | — | — | 0.4 | mA | Pin 5 = OV<br>Pin 4 = —2.0V<br>Pin 6 = —1.95V |
| Output low, current | 13 | 6.0 | 7.0 | 9.0 | mA | Pin 13,15 = OV<br>Pin 3 = —1.7V<br>Pin 4 = —2.0V<br>Pin 6 = —2.3V<br>Pins 2,5 = OV<br>470 Ω pin 12 to —5V<br>27 kΩ pin 14 to —5V<br>Six pos. or neg. pulses on pin 4 |
| Output high, current | 15 | — | — | 1 | µA | |
| Output high, current | 13 | — | — | 1 | µA | Pin 13, 15 = OV<br>Pin 3 = —2.3V<br>Pin 4 = —2.0V<br>Pin 6 = —1.7V<br>Pins 2,5 = OV<br>470 Ω pin 12 to —5V<br>27 kΩ pin 14 to —5V |
| Output low, current | 15 | 0.5 | 0.75 | — | mA | |
| Current consumption | 1,16 | — | 20 | 25 | mA | (Pins 2,5,13,15 = OV<br>(Pins 3,6 = —2.3V<br>(Pin 4 = —2.0V<br>(27 kΩ resistor between<br>(Pin 14 and —5V<br>(Pin 12 open |
| Input bias current | 3 | — | — | 40 | µA | Pin 2 = OV<br>Pin 3 = —1.7V<br>Pin 4 = —2V |
| Input bias current | 6 | — | — | 40 | µA | Pin 4 = —2.0V<br>Pin 5 = OV<br>Pin 6 = —1.7V |
| Input bias current | 4 | — | — | 80 | µA | Pins 2,5 = OV<br>Pins 3,6 = —2.3V<br>Pin 4 = —2.0V |

**AC CHARACTERISTICS**

Circuit reference: Fig.3
Input signal: Fig.2
$T_{amb}$ = -10°C to +70°C
$V_{EE}$ = -4.4V to -5.25V

| Characteristic | Pin | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Max. Input Frequency | | | | | | |
| SP1450 | 13 | | — | 25.5 | M band/s | See note 1 below |
| SP1455 | 13 | | — | 105 | M band/s | See note 1 below |
| Stretched output pulse width | 15 | 0.5 | 0.7 | 2 | µS | $c_1$ = 390 pF $R_1$ = 27 kΩ using circuit of Fig. 7 (see note 2 below) |
| Error pulse width SP1455 | 13 | 4.25 | — | 5.25 | nS | Input freq. 105 M band/s |
| Error pulse amplitude | 13 | 300 | — | — | mV | At max input frequency |
| Spurious pulse amplitude | 13 | — | — | 50 | mV | At max. input frequency |

NOTE 1: These figures are the max.input symbol rates. For 4B3T codes, the effective bit rate is 4/3 x (input frequency).
NOTE 2: Resistor and capacitor values quoted are absolute values; temperature coefficients and tolerances have not been taken into account.

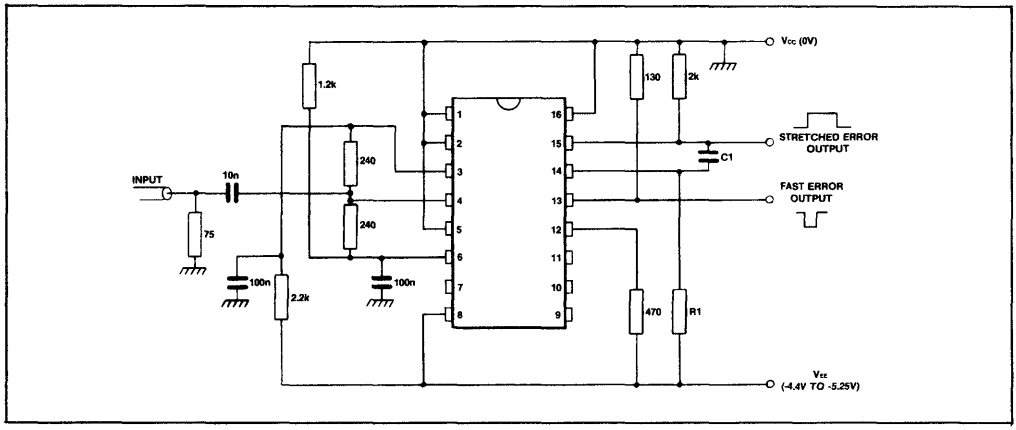


*Fig.3 Functional test circuit*

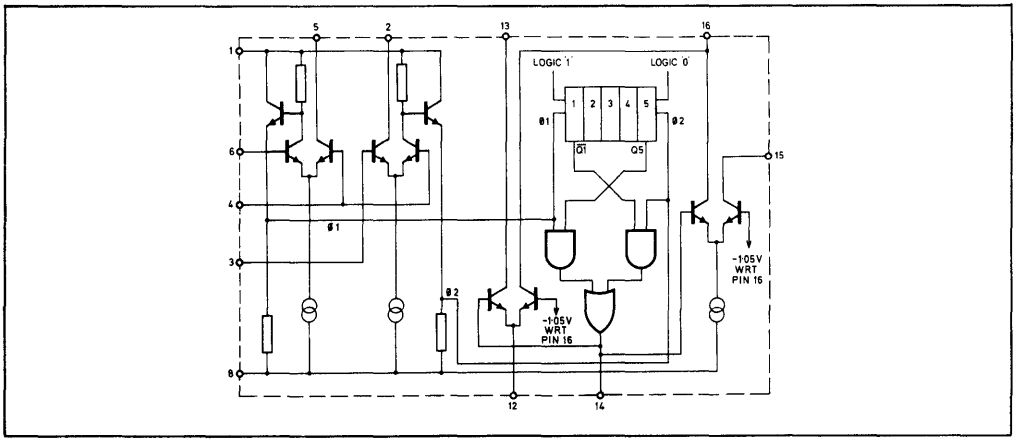


*Fig.4 Circuit diagram of SP1450/SP1455*

## APPLICATIONS

The circuit shown in Fig.3 is designed to accept a three level (ternary) input signal as shown in Fig.2. The input is applied to pin 4 whilst fixed bias levels are maintained on pins 3 and 6. When a positive input pulse is applied at a level more positive than the bias on pin 6 the positive comparator output o 1 goes from '0' ($V_{EE}$) to '1' ($V_{CC}$). The 1-0 edge of this pulse clocks the five bit shift register one place to the right. Repeated operation will cause a pattern of logic '1's to be propagated along the shift register. When bit 5 is at logic '1' and the input is also positive an 'error' will occur at pins 13 and 15.

A negative input pulse at a level more negative than the voltage on bias pin 3 causes the negative comparator output o 2 to clock the shift register one place to the left. Repeated operation causes a pattern of logic '0's to be propagated along the shift register. When bit 1 is at logic '0' and the input is also negative an 'error' output will again occur at pins 13 and 15.

During normal operation the shift register can assume one of only six possible states as shown in Fig.5.

| State | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|
| A | 0 | 0 | 0 | 0 | 0 |
| B | 1 | 0 | 0 | 0 | 0 |
| C | 1 | 1 | 0 | 0 | 0 |
| D | 1 | 1 | 1 | 0 | 0 |
| E | 1 | 1 | 1 | 1 | 0 |
| F | 1 | 1 | 1 | 1 | 1 |

*Fig.5 Shift register states*

When power is initially connected other states may occur.

Two 'error' outputs are available. The fast output at pin 13 is negative going; the peak current is defined by a resistor connected between pin 12 and $V_{EE}$ according to the formula:

$$I = \frac{3.3}{R} \text{ (e.g. 820 ohms; 4mA)}$$

A pullup resistor must then be connected between pin 13 and $V_{CC}$ to give a suitable voltage swing. A suitable ECL interface is shown in Fig.6.

If, as in a repeater application, a fast output is not required, pin 12 should be left open and pin 13 connected to $V_{CC}$ (pin 16).

A stretched output is available from pin 15 by connection of a capacitor between pins 14 and 15. A suitable circuit is shown in Fig.7.

Facilities are available at pins 2 and 5 to detect the absence of negative and positive going input signals. If these are not required pins 2 and 5 should be connected to $V_{CC}$ (pin 1). A CMOS interface circuit is shown in Fig.8.

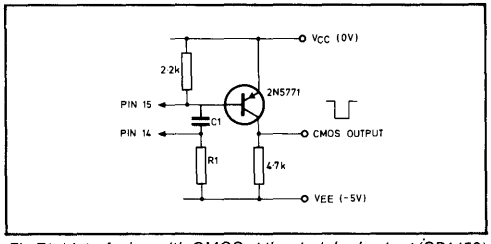


*Fig.7(a) Interfacing with CMOS at the stretched output (SP1450)*

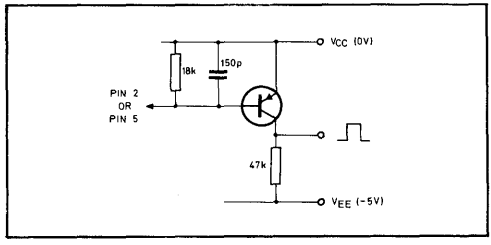


*Fig.8 Interfacing with pulse fail output with CMOS*

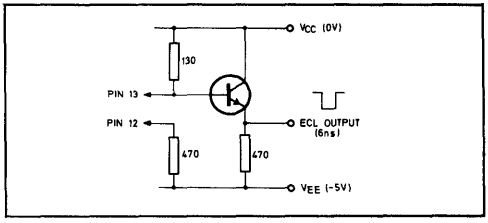


*Fig.6 Interfacing with ECL at the output*

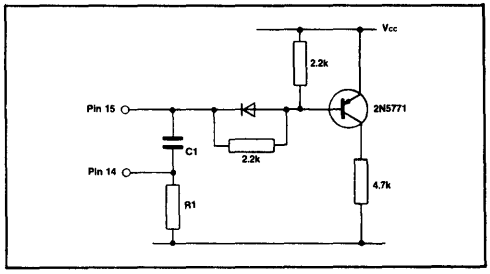


*Fig.7(b) Interfacing with CMOS at the stretched output (SP1455)*