

FEATURES

- ◆ Black on White Film STN Type
- ◆ Transmissive Mode

MECHANICAL DATA

Item	Value	Unit
Module Dimensions	167.0*109*8.5	mm
Viewing Area	120*89	mm
Resolution	320*240	dots
Dot Size	0.345*0.345	mm
Dot Pitch	0.36*0.36	mm
Weight	160	g

OPTICAL DATA

Item	Symbol	Condition	Min	Typ	Max	Unit
Contrast Ratio	K	Ø=10°, Q=0°, Note 1	-	20	-	-
Brightness	-	T=25°C, Note 7	-	80.0	-	cd/m ²
Viewing Direction		-	6			o'clock
Viewing Angle	Ø2 - Ø1	K=2, Note 1	-	40	-	degree
Response Time (Rise)	t _R	Ø=10°, Q=0°, Note 1	-	120	-	ms
Response Time (Fall)	t _F	Ø=10°, Q=0°, Note 1	-	150	-	ms

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Min	Max	Unit
Supply Voltage (Logic)	V _{DD} - V _{SS}	-	0	6	V
Supply Voltage (LC Drive)	V _{DD} - V _{EE}	-	0	27.5	V
Input Voltage	V _I	Note 2	-0.3	0.3+V _{DD}	V
Operating Temperature	T _{OP}	Note 5,6	0	50	°C
Storage Temperature	T _{ST}	Note 5,6	-20	60	°C

DATA INTERFACE PIN ASSIGNMENT

Pin No	Symbol	Level	Function
1-4	D0 - D3	H/L	Display data
5	Not DISP OFF	H/L	High for ON / Low for OFF
6	FRAME	H	First Line Marker
7	NC	-	Do not connect
8	LOAD	H->L	Data latch
9	CP	H->L	Data shift
10	VDD	-	Power supply for logic circuit
11	VSS	-	Ground
12	VEE	-	Power supply for LC drive circuit
13	V0	-	Operating voltage for LC driving
14	FGND	-	Front panel ground

CFL INTERFACE PIN ASSIGNMENT

Pin No	Symbol	Level	Function
1	VCFL	-	Power supply for CFL
2	NC	-	No connection
3	NC	-	No connection
4	VCFL	-	CFL Ground

- ◆ High Brightness CFL Backlight
- ◆ High Contrast LC Material

ELECTRICAL CHARACTERISTICS

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage (Logic)	V _{DD} - V _{SS}	-	4.75	5.0	5.25	V
Supply Voltage (LC Drive)	V _{EE} - V _{SS}	-	-20.9	-22.0	-23.1	V
Supply Current	I _{DD}	Note 3	-	6	-	mA
	I _{EE}	Note 3	-	5	-	mA
Input Voltage (High Level)	V _{IH}	High Level, Note 2	0.8* VDD	-	VDD	V
Input Voltage (Low Level)	V _{IL}	Low Level, Note 2	0	-	0.2* VDD	V
Frame Frequency	f _{FLM}	-	70	75	80	Hz
Duty Ratio		-	-	1/240	-	-
Recommended LC Drive Voltage	V _{DD} - V _O	Duty=1/240 T=0°, Ø=10°, Note 4	-	23.0	-	V
		Duty=1/240 T=25°C, Ø=10°, Note 4	-	22.0	-	V
		Duty=1/240 T=40°C, Ø=10°, Note 4	-	21.0	-	V
Backlight Lamp Voltage	V _{BL}	T=25°C	-	300	-	Vrms
Backlight Lamp Frequency	f _{BL}	T=25°C		70	85	kHz
Backlight Lamp Current	I _{BL}	T=25°C	4	5	6	mA _{rms}
Lamp Start Voltage	V _S	T=25°C	1000	-	-	V
Backlight Lamp Lifetime	T _L	T=25°C	15.000	20.000	-	hrs

TIMING CHARACTERISTICS

Item	Symbol	Min	Typ	Max	Unit
Clock frequency	f _{CP}	-	-	6.5	MHz
Clock pulse width	tw	63	-	-	ns
Rise, Fall time	t _r , t _f	-	-	20	ns
Data set up time	t _{DSU}	50	-	-	ns
Data hold time	t _{DHD}	50	-	-	ns
LOAD set up time	t _{LSU}	80	-	-	ns
LOAD -> Clock time	t _{LC}	80	-	-	ns
FRAME set up time	t _{setup}	100	-	-	ns
FRAME hold time	t _{hold}	100	-	-	ns
LOAD pulse width	twc	125	-	-	ns

INVERTER AND CONNECTORS

Recommended Inverter	Starter Kit
HITACHI INVC132, INVC196	START691x
Lamp Connector	Lamp Housing Connector
JAE IL-G-4S-S3C23	-

- Note1: Definition of optical data, see page 84
- Note 2: Applied to NotDISP.OFF, FRAME, LOAD, CP, D0-D3
- Note 3: FRAME=75Hz, D0-D3=0.1.0.1...VDD-VEE=23.7V, T=25°C
- Note 4: Recommended LC driving voltage may fluctuate about +/-1.0V by each module
- Note 5: Background colour of the LCD changes depending on temperature. Between 40-50°C optical characteristics of the LCD like contrast and viewing angle change but the display remains readable.
- Note 6: Storage at -20°C < 48 hr, at 60°C < 168 hr
- Note 7: Measurement after 10 minutes of CFL operating. Brightness control at 100 %

[illegible]

BLOCK DIAGRAM

The block diagram illustrates the LCD driver circuit for the TMS320C42. It features three main ICs: IC5 (TMS320C42), IC6 (TMS320C42), and IC7 (TMS320C42). IC5 is connected to the CPU (CP) and provides control signals (D0-D3, FRAME, LOAD, DISP OFF) to the other ICs. IC6 is connected to the CPU and provides control signals (D0-D3, FRAME, LOAD, DISP OFF) to the other ICs. IC7 is connected to the CPU and provides control signals (D0-D3, FRAME, LOAD, DISP OFF) to the other ICs. The circuit also includes a POWER SUPPLY block with inputs VDD, VSS, VEE, V0, and VCFL, and a CFL block with input VCFL. The LCD is a 320 x 240 pixel display. The diagram shows the interconnections between the ICs, the power supply, and the LCD, including the data bus (D0-D3) and control signals (FRAME, LOAD, DISP OFF, CP).

POWER SUPPLY / POWER TIMING DIAGRAM

LCM

VDD

VSS

V0

VEE

5V

VR

22.0V

NOTE 1: IT IS RECOMMENDED TO ADD FUS (1 A) TO VDD LINE

NOTE 2: VR = 10kW

4.75V

5V

4.75V

VDD

SIGNAL

VEE

0-50ms

0-50ms

0-50ms

20ms min

0 min

20ms min

0 min

DISP OFF

POWER ON

POWER OFF

INTERFACE TIMING DIAGRAM

The diagram illustrates the timing relationships between various signals in the system. The top section is for the condition $52.1\text{ms} < T < 59.5\text{ms}$, and the bottom section shows a minimum delay of 1.4ms between the LOAD and FRAME signals.

Top Section Timing Parameters:

- tw : Write time
- tf : Fall time
- tr : Rise time
- td_{SU} : Data setup time
- tD_{HD} : Data hold time
- tL_{SU} : Load setup time
- tL_C : Load clock time
- $tSETUP$: Setup time
- $tHOLD$: Hold time

Bottom Section Timing Parameters:

- 1.4ms min. : Minimum delay between LOAD and FRAME signals

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