SP201

Offline Current Mode PWM Controller with Built-in CC Regulation

FEATURES

- **General Primary Side Constant-Current (CC) Control Supports DCM and CCM Operation**
- **±5% CC Regulation, ±1% CV Regulation with Fast Dynamic Response**
- **CC Algorithm Compensates for Line Variation and Transformer Inductance Tolerance**
- **Less than 75mW Standby Power for sub 30W Application**
- **Current Mode Control**
- **Built-in Frequency Shuffling**
- **Fixed 65KHz Switching Frequency**
- **Green Mode and Burst Mode Control**
- **On-chip Thermal Shutdown**
- **Cycle-by-Cycle Current Limiting**
- **Built-in Leading Edge Blanking**
- **Built-in Slope Compensation**
- **Very Low Startup and Operation Current**
- **Available with SOT23-6 Package**

APPLICATIONS

- **Chargers and Adapter**
- **Motor Driver Power Supply**

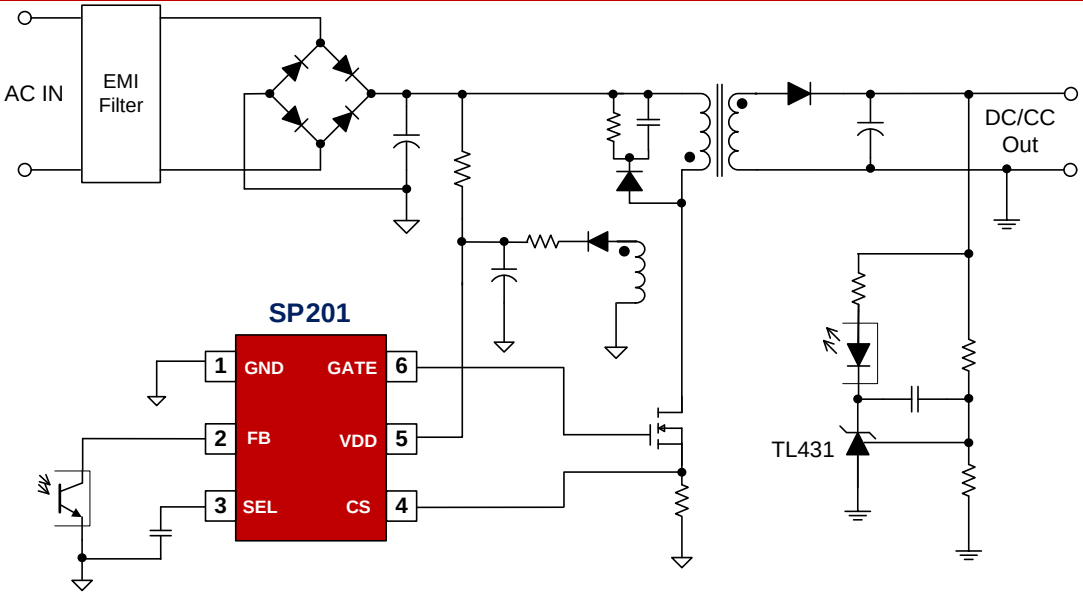
GENERAL DESCRIPTION

SP201 is a high performance current mode PWM controller for offline flyback converter applications. The IC has built-in General Primary Side CC control, which simplifies isolated power supply design that requires CC regulation of the output.

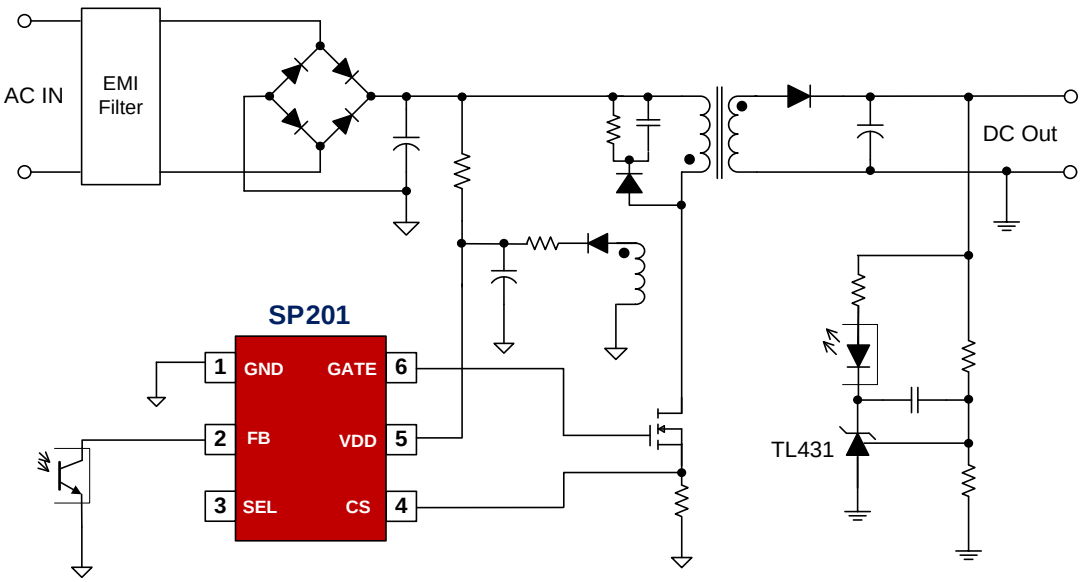
In SP201, PWM switching frequency with shuffling is fixed to 65KHz and is trimmed to tight range. The IC has built-in green and burst mode control for light and zero loadings, which can achieve less than 75mW standby power for sub 30W applications..

SP201 integrates functions and protections of Under Voltage Lockout (UVLO), VDD over Voltage Protection (VDD OVP), Cycle-by-cycle Current Limiting (OCP), Short Load Protection (SLP), Over Load Protection (OLP), On-Chip Thermal Shutdown (OTP), Soft Start, VDD Clamping, etc. .

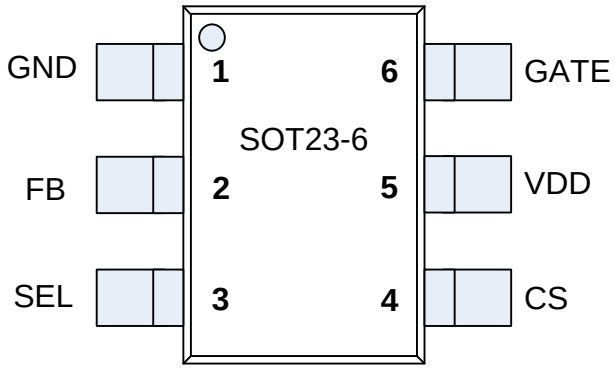
TYPICAL APPLICATION CIRCUIT (For Applications with CC/CV Control)



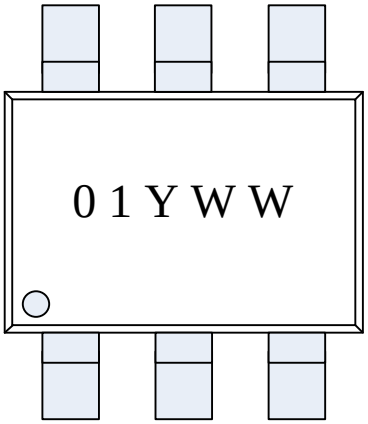
TYPICAL APPLICATION CIRCUIT (For Applications with Only CV Control)



Pin Configuration



Marking Information



Dot: Pin1 Mark
01: Part number KP201
YWW: Year&Week Code

Pin Description (KP201A)

Pin Number	Pin Name	I/O	Description
1	GND	P	The ground of the IC
2	FB	I	Feedback pin. The loop regulation is achieved by connecting a photo-coupler to this pin. PWM duty cycle is determined by this pin voltage and the current sense signal at Pin 4.
3	SEL	I	Connect a capacitor between SEL and GND, the IC will work in CC/CV mode. If SEL pin is floating, the IC will work in CV mode only.
4	CS	I	Current sense input pin.
5	VDD	P	IC power supply pin.
6	GATE	O	Totem-pole gate driver output to drive the external MOSFET.

Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
VDD DC Supply Voltage	35	V
VDD DC Clamp Current	10	mA
FB, CS, SEL voltage range	-0.3 to 7	V
GATE voltage range	20	V
Package Thermal Resistance (SOT23-6)	250	^{o}C/W
Maximum Junction Temperature	150	^{o}C
Operating Temperature Range	-40 to 85	^{o}C
Storage Temperature Range	-65 to 150	^{o}C
Lead Temperature (Soldering, 10sec.)	260	^{o}C
ESD Capability, HBM (Human Body Model)	3	kV
ESD Capability, MM (Machine Model)	250	V

Recommended Operation Conditions (Note 2)

Parameter	Value	Unit
Supply Voltage, VDD	10.5 to 28.5	V
Operating Ambient Temperature	-40 to 85	^{o}C

ELECTRICAL CHARACTERISTICS (T_A = 25^{o}C, VDD=22V, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage Section(VDD Pin)						
I_{VDD_st}	Start-up current into VDD pin			2	20	uA
I_{VDD_Op}	Operation Current	V_{FB}=3V,GATE=1nF		1.2	2	mA
$I_{VDD\_standby}$	Standby Current			0.6	1	mA
V_{DD_ON}	VDD Under Voltage Lockout Exit		19	21	23	V
V_{DD_OFF}	VDD Under Voltage Lockout Enter		8.2	9.3	10.2	V
V_{DD_OVP}	VDD OVP Threshold		29	31.5	33	V
V_{DD_Clamp}	VDD Zener Clamp Voltage	$I(V_{DD})$ = 7 mA	33.5	35.5	37.5	V
Feedback Input Section (FB Pin)						
V_{FB_Open}	FB Open Voltage		4.5	5.4	6	V

I_{FB_Short}	FB Short Circuit Current	Short FB Pin to GND, Measure Current		0.4		mA
Z_{FB_IN}	FB Input Impedance			25		Kohm
A_{CS}	PWM Gain	$\Delta V_{FB}/\Delta V_{CS}$		2.0		V/V
V_{skip}	FB Under Voltage GATE Clock is OFF			1.0		V
V_{TH_OLP}	Power Limiting FB Threshold Voltage			3.6		V
T_{D_OLP}	Power Limiting Debounce Time	SEL Pin is floating		75		ms
Current Sense Input Section (CS Pin)						
T_{LEB}	CS Input Leading Edge Blanking Time			250		ns
$V_{cs(max)}$	Current limiting threshold		0.97	1.0	1.03	V
T_{D_OC}	Over Current Detection and Control Delay	GATE=1nF		70		ns
Oscillator Section						
F_{OSC}	Normal Oscillation Frequency		60	65	70	KHz
$\Delta F(shuffle)/F_{OSC}$	Frequency Shuffling Range		-4		4	%
T(shuffle)	Frequency Shuffling Period			32		ms
D_{MAX}	Maximum Switching Duty Cycle			66.7		%
F_{Bust}	Burst Mode Base Frequency			22		KHz
CC Loop Regulation Section (SEL = Capacitor)						
V_{CC_Reg}	Internal Reference for CC Loop Regulation	SEL Pin=Capacitor	194	200	206	mV
$I_{CC\_SEL\_Source}$	Internal Source Current for CC Loop Regulation	SEL Pin=Capacitor		20		uA
$V_{CC\_SLP\_SEL}$	Short Load Protection (SLP) Threshold	SEL Pin=Capacitor		0.7		V
$T_{CC\_Short\_SEL}$	Short Load Protection (SLP) Debounce Time	SEL Pin=Capacitor		210		ms
On-Chip Thermal Shutdown						
T_{SD}	Thermal Shutdown	(Note 3)	---	165	--	° C

T_{RC}	Thermal Recovery	(Note 3)		140	--	˚C
GATE Driver Section (GATE Pin) (Note 3)						
V_{OL}	Output Low Level	Igate_sink=20mA			1	V
V_{OH}	Output High Level	Igate_source=20mA	7.5			V
V_{G_Clamp}	Output Clamp Voltage Level	VDD=24V		16		V
T_r	Output Rising Time	GATE=1nF		150		ns
T_f	Output Falling Time	GATE=1nF		60		ns

Note1. Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note2. The device is not guaranteed to function outside its operating conditions.

Note3. Guaranteed by the Design.