SamHop Microelectronics Corp.

SP2108

Ver 1.0

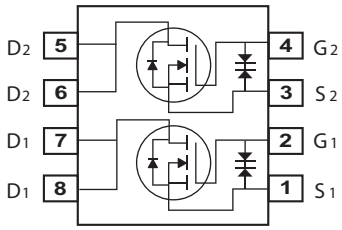
Dual N-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V_{DSS}	I_D	$R_{DS(ON)}$ (mΩ) Max
100V	1.2A	811 @ VGS=10V
		932 @ VGS=4.5V

FEATURES

- Super high dense cell design for low $R_{DS(ON)}$.
- Rugged and reliable.
- Suface Mount Package.
- ESD Protected.

PDFN 5x6



ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

Symbol	Parameter		Limit	Units
V_{DS}	Drain-Source Voltage		100	V
V_{GS}	Gate-Source Voltage		±20	V
I_D	Drain Current-Continuous [c]	T_A=25°C	1.2	A
		T_A=70°C	0.96	A
I_{DM}	-Pulsed [a c]		5	A
E_{AS}	Single Pulse Avalanche Energy [d]		4	mJ
P_D	Maximum Power Dissipation	T_A=25°C	2.5	W
		T_A=70°C	1.6	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range		-55 to 150	°C

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	50	°C/W

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	100			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=80V , V_{GS}=0V			1	uA
I_{GSS}	Gate-Body Leakage Current	V_{GS}= ±20V , V_{DS}=0V			±10	uA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} , I_D=250uA	1	1.9	3	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V , I_D=0.6A		649	811	m ohm
		V_{GS}=4.5V , I_D=0.5A		690	932	m ohm
g_{FS}	Forward Transconductance	V_{DS}=10V , I_D=0.6A		2.8		S
SWITCHING CHARACTERISTICS [b]						
$t_{D(ON)}$	Turn-On Delay Time	V_{DD}=50V I_D=0.6A V_{GS}=10V R_{GEN}= 6 ohm		54		ns
t_r	Rise Time			41		ns
$t_{D(OFF)}$	Turn-Off Delay Time			910		ns
t_f	Fall Time			149		ns
Q_g	Total Gate Charge	V_{DS}=50V,I_D=0.6A,V_{GS}=10V		3.4		nC
Q_{gs}	Gate-Source Charge	V_{DS}=50V,I_D=0.6A, V_{GS}=10V		0.85		nC
Q_{gd}	Gate-Drain Charge			1		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
V_{SD}	Diode Forward Voltage	V_{GS}=0V,I_S=1A		0.86	1.2	V

Notes

a.Pulse Test:Pulse Width ≤ 10us, Duty Cycle ≤ 1%.
b.Guaranteed by design, not subject to production testing.
c.Drain current limited by maximum junction temperature.
d.Starting T_J=25°C,L=0.5mH,V_{DD} = 50V.(See Figure12)
e.Mounted on FR4 Board of 1 $inch^2$, 2oz.

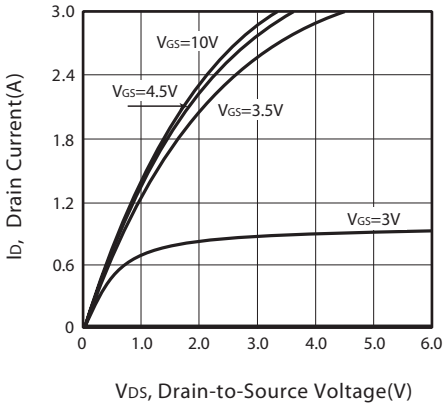


Figure 1. Output Characteristics

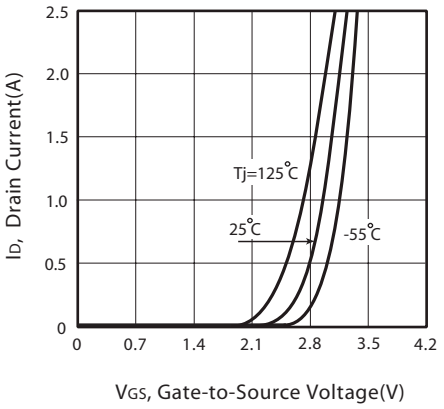


Figure 2. Transfer Characteristics

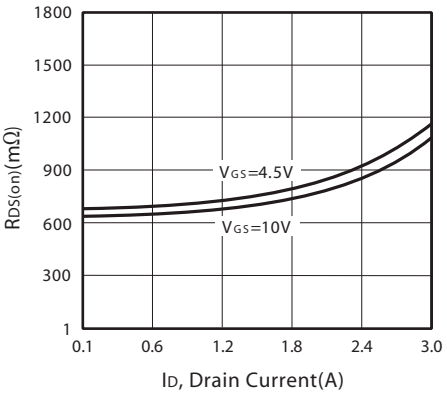


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

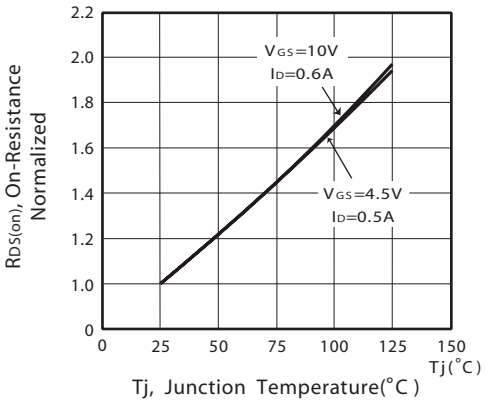


Figure 4. On-Resistance Variation with Drain Current and Temperature

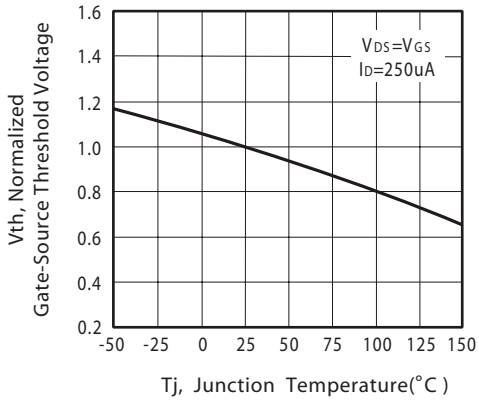


Figure 5. Gate Threshold Variation with Temperature

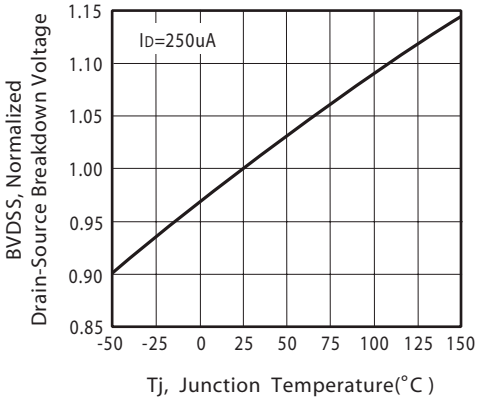


Figure 6. Breakdown Voltage Variation with Temperature

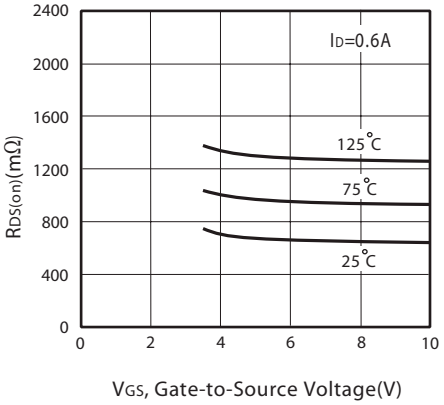


Figure 7. On-Resistance vs. Gate-Source Voltage

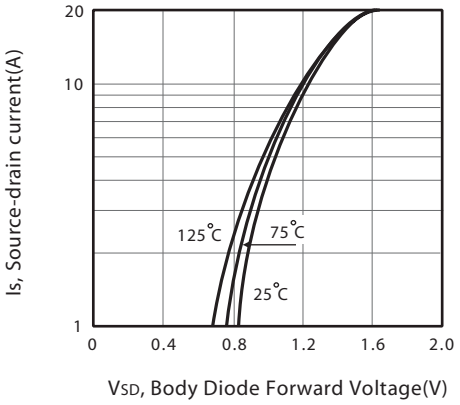


Figure 8. Body Diode Forward Voltage Variation with Source Current

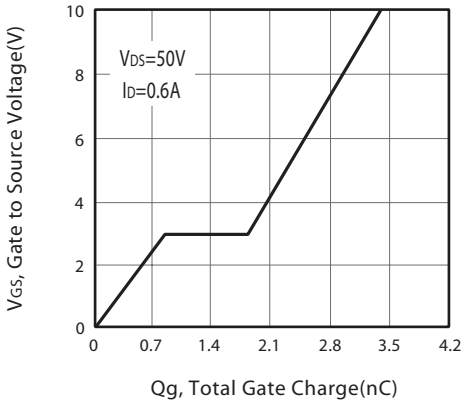


Figure 9. Gate Charge

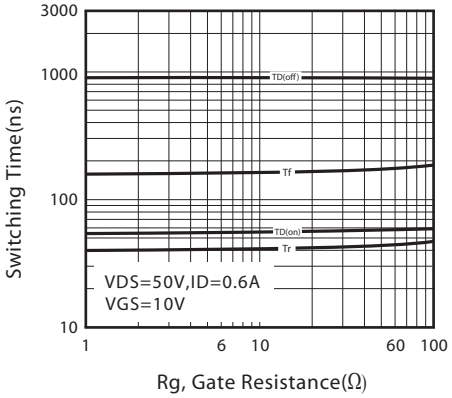


Figure 10. switching characteristics

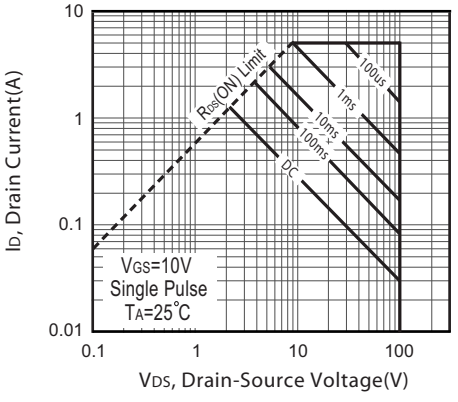
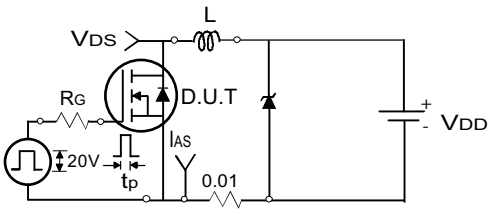
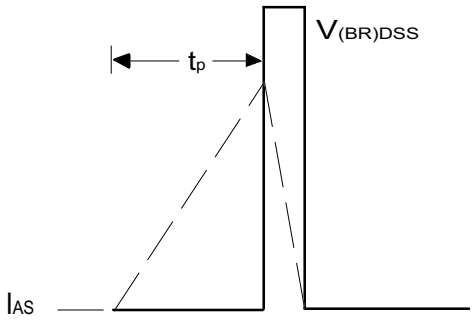


Figure 11. Maximum Safe Operating Area



Uncamped Inductive Test Circuit

Figure 12a.



Unclamped Inductive Waveforms

Figure 12b.

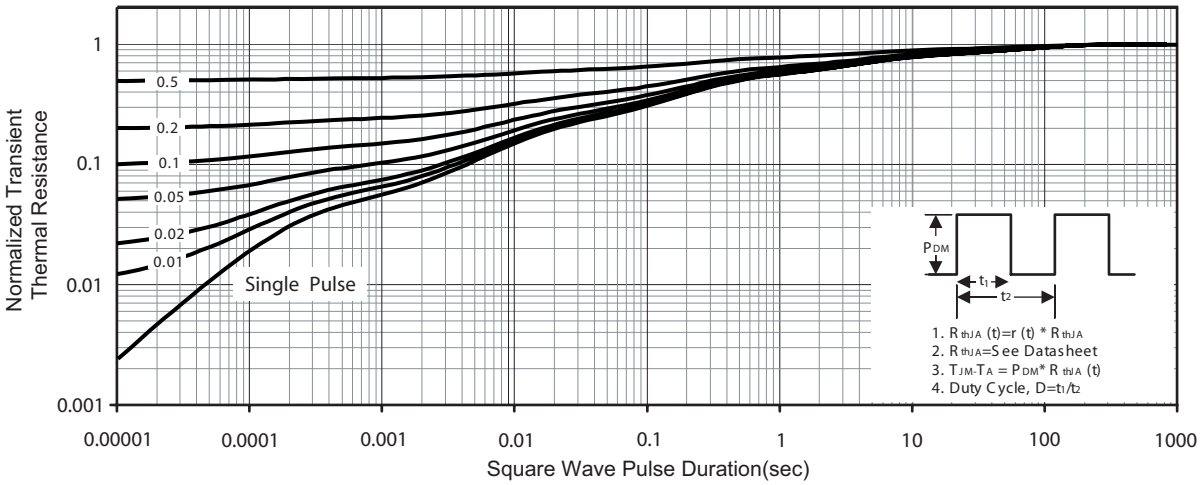
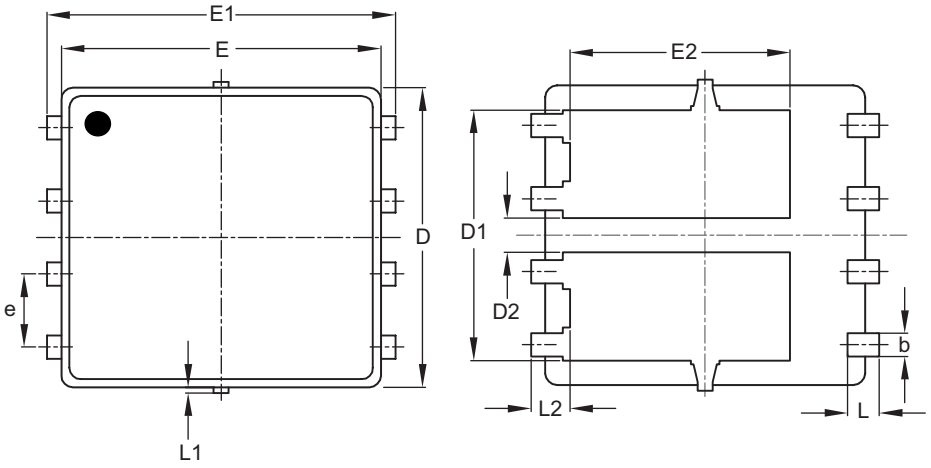


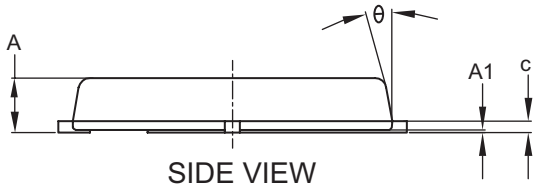
Figure 13. Normalized Thermal Transient Impedance Curve

PACKAGE OUTLINE DIMENSIONS

PDFN 5x6-8L



TOP VIEW BOTTOM VIEW



SIDE VIEW

SYMBOLS	MILLIMETERS		
	MIN	NOM	MAX
A	0.85	0.95	1.00
A1	0.00	—	0.05
b	0.30	0.40	0.50
c	0.15	0.20	0.25
D		5.20 BSC	
D1		4.35 BSC	
D2	0.50	0.60	0.75
E		5.55 BSC	
E1		6.05 BSC	
E2		3.82 BSC	
e		1.27 BSC	
L	0.45	0.55	0.65
L1	0.00	—	0.15
L2		0.68 REF	
θ	0°	—	10°

TOP MARKING DEFINITION

PDFN 5x6-8L