



SamHop Microelectronics Corp.



SP2112

Ver 1.0

## Dual N-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
VDSS	ID	RDS(ON) (mΩ) Max
100V	1.2A	390 @ VGS=10V
		430 @ VGS=4.5V

### FEATURES

- Super high dense cell design for low RDS(ON).
- Rugged and reliable.
- Surface Mount Package.



### ABSOLUTE MAXIMUM RATINGS ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		Limit	Units
$V_{DS}$	Drain-Source Voltage		100	V
$V_{GS}$	Gate-Source Voltage		$\pm 20$	V
$I_D$	Drain Current-Continuous <sup>a c</sup>	$T_A=25^\circ\text{C}$	1.2	A
		$T_A=70^\circ\text{C}$	1.0	A
$I_{DM}$	-Pulsed <sup>c</sup>		8	A
$E_{AS}$	Single Pulse Avalanche Energy <sup>d</sup>		0.64	mJ
$P_D$	Maximum Power Dissipation <sup>a</sup>	$T_A=25^\circ\text{C}$	1.47	W
		$T_A=70^\circ\text{C}$	0.94	W
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range		-55 to 150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	85	$^\circ\text{C/W}$
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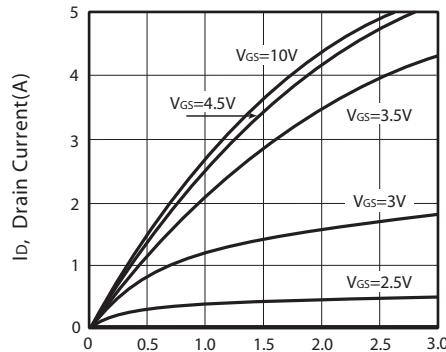
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## ELECTRICAL CHARACTERISTICS ( $T_A=25^\circ\text{C}$ unless otherwise noted)

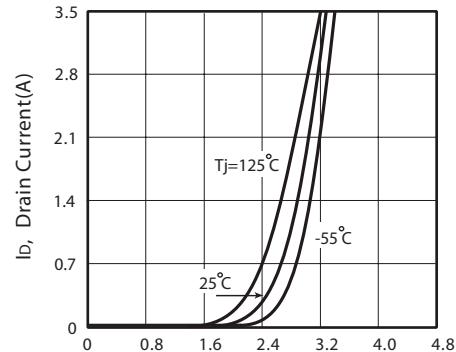
Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu\text{A}$	100			V
IDS <sub>S</sub>	Zero Gate Voltage Drain Current	$V_{DS}=80V, V_{GS}=0V$			1	$\mu\text{A}$
IGSS	Gate-Body Leakage Current	$V_{GS} = \pm 20V, V_{DS}=0V$			$\pm 100$	nA
<b>ON CHARACTERISTICS</b>						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1	1.7	3	V
R <sub>D<sub>S(ON)</sub></sub>	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=0.6A$		320	390	m ohm
		$V_{GS}=4.5V, I_D=0.55A$		350	430	m ohm
g <sub>FS</sub>	Forward Transconductance	$V_{DS}=5V, I_D=0.6A$		2		S
<b>DYNAMIC CHARACTERISTICS <sup>b</sup></b>						
C <sub>ISS</sub>	Input Capacitance	$V_{DS}=25V, V_{GS}=0V$ $f=1.0\text{MHz}$		248		pF
C <sub>OSS</sub>	Output Capacitance			21		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			14		pF
<b>SWITCHING CHARACTERISTICS <sup>b</sup></b>						
t <sub>D(ON)</sub>	Turn-On Delay Time	$V_{DD}=50V$ $I_D=0.6A$ $V_{GS}=10V$ R <sub>GEN</sub> = 6 ohm		8		ns
t <sub>r</sub>	Rise Time			10		ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time			16.5		ns
t <sub>f</sub>	Fall Time			4		ns
Q <sub>g</sub>	Total Gate Charge	$V_{DS}=50V, I_D=0.6A, V_{GS}=10V$		4.8		nC
		$V_{DS}=50V, I_D=0.6A, V_{GS}=4.5V$		2.7		nC
Q <sub>gs</sub>	Gate-Source Charge	$V_{DS}=50V, I_D=0.6A,$ $V_{GS}=10V$		0.8		nC
Q <sub>gd</sub>	Gate-Drain Charge			1.3		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
V <sub>SD</sub>	Diode Forward Voltage	$V_{GS}=0V, I_S=1A$		0.8	1.2	V
<b>Notes</b>						
a. Surface Mounted on FR4 Board of 1 inch <sup>2</sup> , 1oz.						
b. Guaranteed by design, not subject to production testing.						
c. Drain current limited by maximum junction temperature.						
d. Starting $T_J=25^\circ\text{C}$ , $L=0.5\text{mH}$ , $V_{DD}=50V$ . (See Figure13)						

May,07,2014



V<sub>DS</sub>, Drain-to-Source Voltage(V)

Figure 1. Output Characteristics



V<sub>Gs</sub>, Gate-to-Source Voltage(V)

Figure 2. Transfer Characteristics

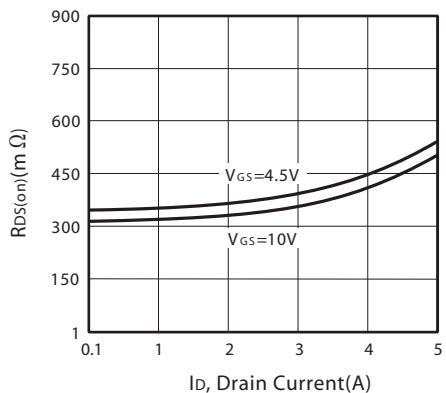


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

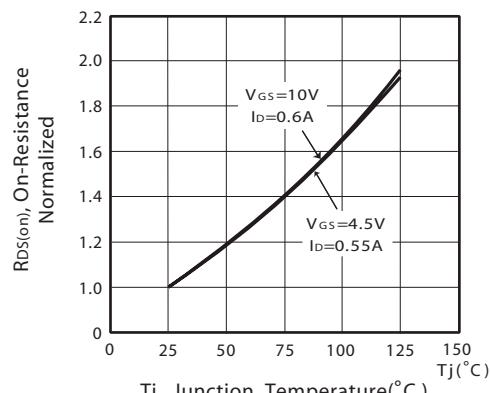


Figure 4. On-Resistance Variation with Drain Current and Temperature

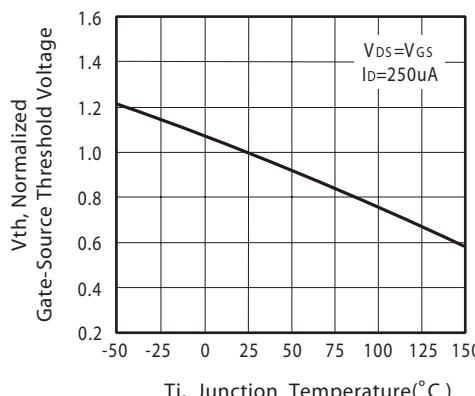


Figure 5. Gate Threshold Variation with Temperature

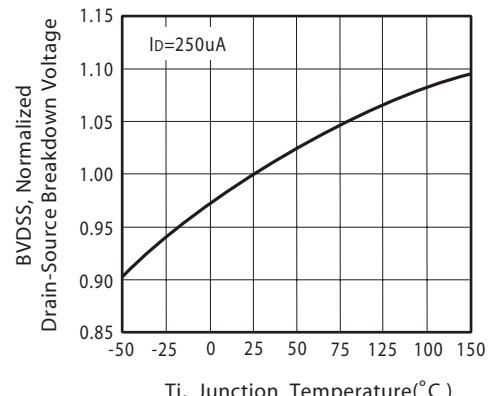
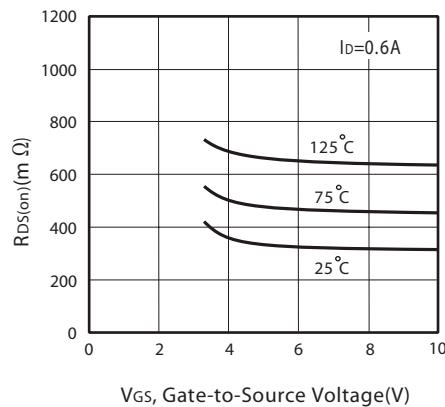
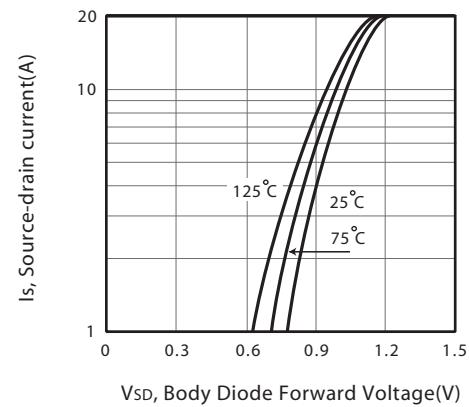


Figure 6. Breakdown Voltage Variation with Temperature



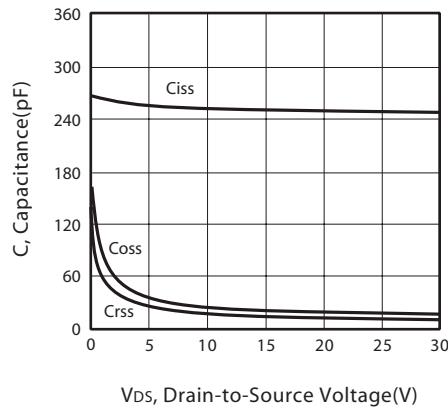
V<sub>GS</sub>, Gate-to-Source Voltage(V)

Figure 7. On-Resistance vs. Gate-Source Voltage



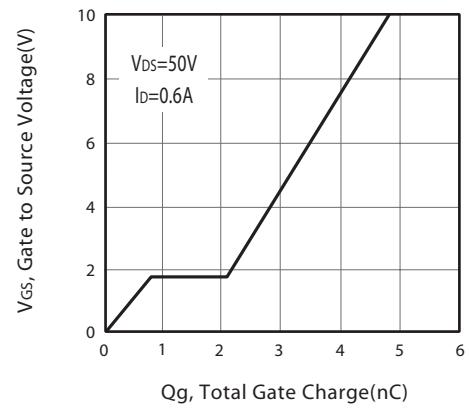
V<sub>SD</sub>, Body Diode Forward Voltage(V)

Figure 8. Body Diode Forward Voltage Variation with Source Current



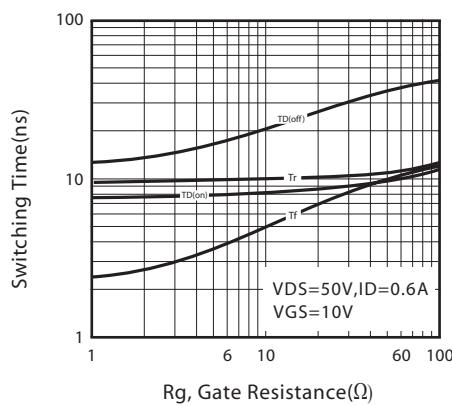
V<sub>DS</sub>, Drain-to-Source Voltage(V)

Figure 9. Capacitance



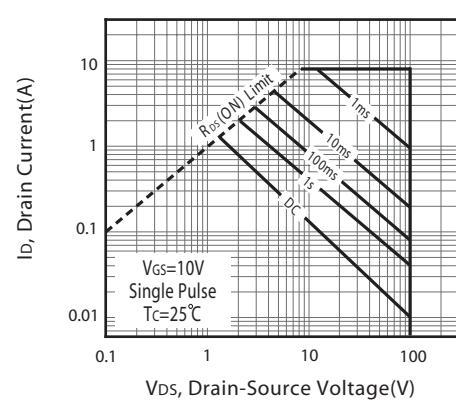
Q<sub>g</sub>, Total Gate Charge(nC)

Figure 10. Gate Charge



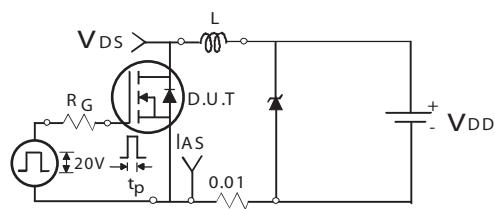
R<sub>g</sub>, Gate Resistance(Ω)

Figure 11. switching characteristics



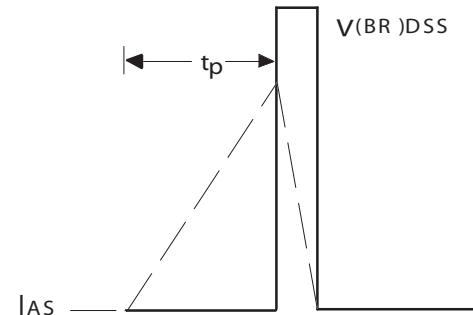
V<sub>DS</sub>, Drain-Source Voltage(V)

Figure 12. Maximum Safe Operating Area



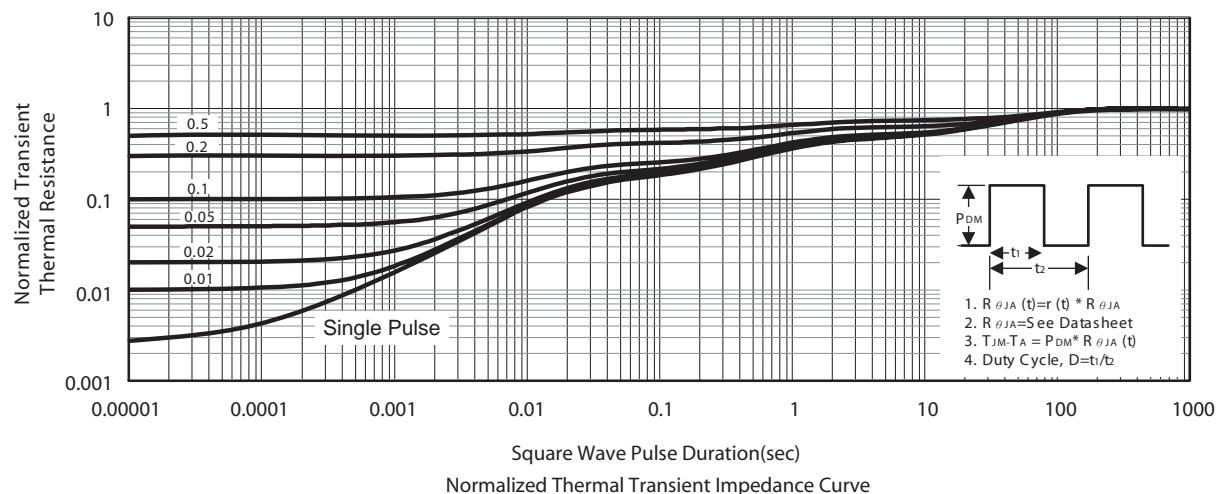
Unclamped Inductive Test Circuit

Figure 13a.



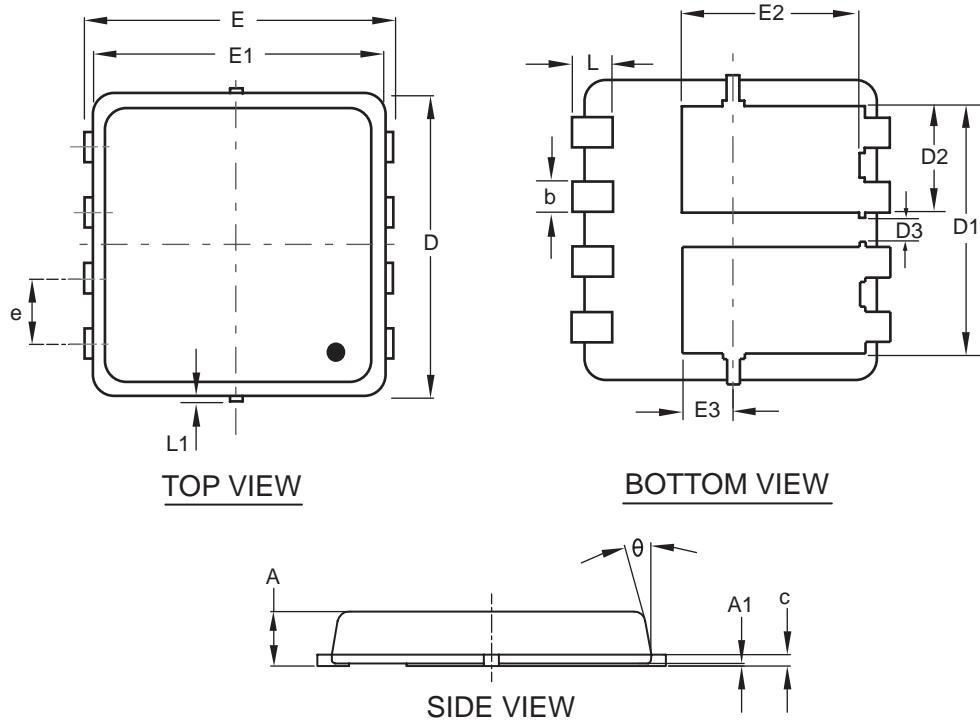
Unclamped Inductive Waveforms

Figure 13b.



## PACKAGE OUTLINE DIMENSIONS

**DFN 3x3-8L**



SYMBOLS	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.80	0.90
A1	0.00	—	0.05
b	0.24	0.30	0.35
c	0.10	0.152	0.25
D	3.00 BSC		
D1	2.475 BSC		
D2	1.063 BSC		
D3	0.225 BSC		
E	3.20 BSC		
E1	3.00 BSC		
E2	1.813 BSC		
E3	0.525 BSC		
e	0.65 BSC		
L	0.30	0.40	0.50
L1	0.00	—	0.100
θ	0°	10°	12°

## TOP MARKING DEFINITION

DFN 3x3

