Specifications

DVB-S2 NIM TUNER

SP2237AVb

Date : DEC. 2. 2008.

SERIT Co., Ltd.

#1001, Sunil Technopia, Sangdaewon-dong,
Jungwon-gu, Seongnam City, Gyeonggi-do,
Korea, 462-120

Tel. 86-755-26505315

Fax. 86-755-26504227

SERIT	DVB-S2 NIM	SP2237AVb	
		REV	A1

Description: The open DVB-S2 standard for advanced modulation [8PSK modulation With LDPC/BCH Forward Error Correction], as well as legacy DVB and DSS specification

1. General Specifications of RF Tuner (STB6110A).

1-1	Receiving Frequency Range	950~ 2150MHz
1-2	RF Input Impedance	75Ω
1-3	Channel Selection System	Built in PLL (I^2C Bus : Link IC)
1-4	RF input Connector	F Type (Female)
1-5	PLL Step Size	Depending on PLL Setting
1-6	Operating Voltage	LNB Power : (TYP) +3.3VL : 3.3V DC (± 5%) +3.3VT : 3.3V DC (± 5%) AGC Voltage : 0.5V ~ 2.5V DC
1-7	Current Consumption in Tuner Part	<table><tr><th></th><th>MIN</th><th>TYP</th><th>MAX</th></tr><tr><td>+3.3VL</td><td></td><td>15mA</td><td>20mA</td></tr><tr><td>+3.3VT</td><td></td><td>185mA</td><td>200mA</td></tr></table>
1-8	Temperature	Operating: 0℃ to 70℃ Storage: -40℃ to 125℃
1-9	Humidity	Operating: less than 85% Storage: less than 90%

2. Electrical Specifications of RF Tuner (STB6110A)

Optimal Test Condition :

1. Supply Voltage : 3.3V ± 0.3V DC
2. Ambient Temperature: 25℃ ± 5 %
3. Ambient Humidity: 65% ±1 0%

Table2.

No	Item	Specification				Condition
		Min	Typ	Max	Unit	
2-1	Input Level	-65		-25	dBm	
2-2	RF Input VSWR		2	3	dB	
2-3	Noise Figure		6	10	dB	
2-4	3'rd order Intermodulation Rejection Ratio	40	50		dB	Desired & Undesired input Level are -25dBm
2-5	Local Oscillation Signal leakage at RF Input Terminal		-80	-70	dBm	950 ~ 2150 MHz
2-6	Gain Deviation		8	10	dB	950 ~ 2150 MHz
2-7	Phase Noise 10KHz Offset Freq 100KHz 1MHz		-87 -90 -112		dBc/Hz	

3. Programming

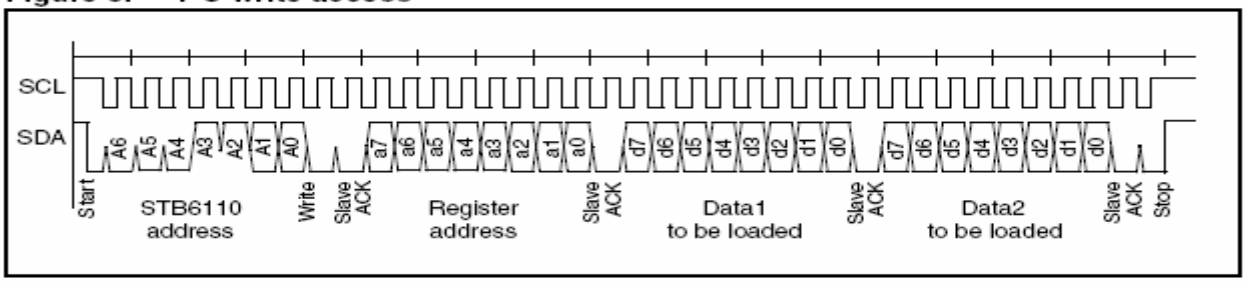
3.1 I2C Interface (STB6110A)

Write access

The byte sequence sent by the master is as follows:

1. The first byte gives the 7-bit device address plus the direction bit, RW = 0.
2. The second byte contains the internal address of the first register to be accessed.
3. The next byte is written in the internal register. Any following bytes are written in successive internal registers.
4. The transfer lasts until a stop bit is encountered.
5. The STB6110, as slave, acknowledges every byte transfer.

Figure 8. I^2C write access

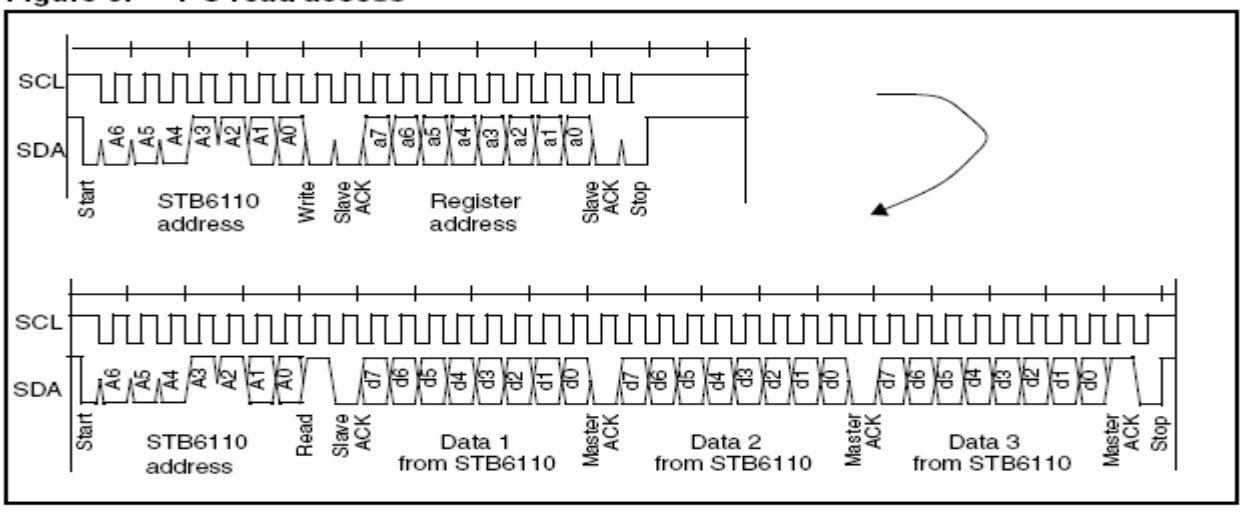


Read access

The byte sequence is as follows:

1. The master sends the first byte (7-bit device address and direction bit, RW = 0).
2. The second byte contains the internal address of the first register to be accessed.
3. This is terminated with a stop bit.
4. The master restarts the transmission with the device address and direction bit, RW = 1.
5. Now the STB6110 acknowledges and sends the register content. If the master acknowledge is low, the slave transmits another byte which is the contents of the next address register. This continues until the master acknowledge is high, then the transmission terminates with a stop bit.

Figure 9. I^2C read access



3.2 Register Map (STB6110A)

Register summary

Name	Addr	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CTRL1	0x0	0x5F	K[4:0]					LPT	RX	SYN
CTRL2	0x1	0x33	CO_DIV[1:0]S		Reserved	REFOUT SEL	BB_GAIN[3:0]			
TUNING0	0x2	0x30	N_DIV[7:0]							
TUNING1	0x3	0xC7	R_DIV[1:0]		PRESC 32ON	DIV4SEL	N_DIV[11:8]			
CTRL3	0x4	0x12	DCLOOP _OFF	Reserved	ICP	CF[4:0]				
STAT1	0x5	0x06	Reserved for test: set to 0					CALVCO _STRT	CALRC _STRT	LOCK
STAT2	0x6	0x00	Reserved for test: set to 0							
STAT3	0x7	0x00	Reserved for test: set to 0							

3.3 Register Description (STB6110A)

CTRL1 Calibration frequency and circuit configuration

K[4:0]					LPT	RX	SYN

Address: 0x00

Type: RW

Reset: 0x5F

Description:

7:3 K[4:0]: determines the divider value for setting the calibration frequency
The application requires a calibration frequency of 1 MHz.

2:0 LPT, RX, SYN: These three bits set the operating level. Only four combinations are allowed as given in the table below:

LPT	RX	SYN	Operating levels		
			Loop-through	Synthesizer (VCO, PFD, CP, Dividers)	LNA, Mixer, LPF, PGA and Buffers
0	0	0	Off	Off	Off
1	1	1	On	On	On
0	1	1	Off	On	On
1	0	0	On	Off	Off, except the LNA
All other combinations			Reserved: not to be used		

CTRL2 Output divider and BB gain setting

CO_DIV[1:0]		Reserved	REFOUTSEL	BB_GAIN[3:0]			

Address: 0x01

Type: RW

Reset: 0x33

Description:

7:6 CO_DIV[1:0]: sets the crystal oscillator divisor value, CO, for the output clock
00: divide by 1 (output frequency is f_{XTAL}) (default)
01: divide by 2
10: divide by 4
11: divide by 8

5 Reserved: set to 1

4 REFOUTSEL: sets the DC voltage on pins IP, IN, QP, QN:
0: VCC / 2
1: 1.25 V (default)

3:0 BB_GAIN[3:0]: sets the baseband amplifier gain
When the amplifier is on
the gain is increased as follows:
0x0: 0 dB
0x1: 2 dB
0x2: 4 dB
0x3: 6 dB (default)
0x4: 8 dB
0x5: 10 dB
0x6: 12 dB
0x7: 14 dB
0x8: 16 dB
0x9-0xF: not used.

TUNING1 N-integer divider LSBs

N-DIV[7:0]							

Address: 0x02

Type: RW

Reset: 0x30

Description:
7:0 N_DIV[7:0]: the LSBs of N_DIV[11:0], which sets the PLL divider value, N

TUNING2 Values for prescaler and dividers R, P and N

R_DIV[1:0]		PRESC32ON	DIV4SEL	N_DIV[11:8]			

Address: 0x03

Type: RW

Reset: 0xC7

Description:
Information on the usage of this register is also given in

7:6 R_DIV[1:0]: sets the divisor, R, for the reference divider:
00: 2
01: 4
10: 8
11: 16 (default)

5 PRESC32ON: selects the divisor for the pre-scaler divider:
0: 16 (default)
1: 32

4 DIV4SEL: selects the divisor, P, for the post divider:
0: 2 (default)
1: 4

3:0 N_DIV[11:8]: the MSBs of N_DIV[11:0], which sets the N-integer divider value N

CTRL3 Control 3 register

DCLOOP_OFF	Reserved	ICP	CF[4:0]				

Address: 0x04

Type: RW

Reset: 0x12

Description:

7 DCLOOP_OFF: selects the DC offset compensation loop:
0: compensation disabled (default)
1: compensation enabled

6 Reserved: set to 0

5 ICP: sets the value of the charge pump current:
0: 500 µA (default)
1: 1.0 mA

4:0 CF[4:0]: sets the baseband filter cut-off frequency:

0x00: 5 MHz	0x01: 6 MHz
0x02: 7 MHz	0x03: 8 MHz
0x04: 9 MHz	0x05: 10 MHz
0x06: 11 MHz	0x07: 12 MHz
0x08: 13 MHz	0x09: 14 MHz
0x0A: 15 MHz	0x0B: 16 MHz
0x0C: 17 MHz	0x0D: 18 MHz
0x0E: 19 MHz	0x0F: 20 MHz
0x10: 21 MHz	0x11: 22 MHz
0x12: 23 MHz (default)	0x13: 24 MHz
0x14: 25 MHz	0x15: 26 MHz
0x16: 27 MHz	0x17: 28 MHz
0x18: 29 MHz	0x19: 30 MHz
0x1A: 31 MHz	0x1B: 32MHz
0x1C: 33 MHz	0x1D: 34 MHz
0x1E: 35 MHz	0x1F: 36 MHz

STAT1 Status register 1

TEST1[4:0]					CALVCO_STRT	CALRC_STRT	LOCK

Address: 0x05

Type: RW

Reset: 0x06

Description:

7:3 TEST1[4:0]: set to 0x00

2 CALVCO_STRT: automatic calibration of VCO:
0: VCO calibration finished
1: start VCO calibration (default)

1 CALRC_STRT: automatic calibration of the low-pass filter:
0: filter calibration finished
1: start filter calibration (default)

0 LOCK: indicates when loop is locked:
0: not in lock
1: locked

STAT2 Status register 2

TEST2[7:0]							

Address: 0x06

Type: RW

Reset: 0x00

Description: A test setup register

7:0 TEST2[7:0]: reserved, set to 0x00

STAT3 Status register 3

TEST2[7:0]							

Address: 0x07

Type: RW

Reset: 0x00

Description: A test setup register

7:0 TEST3[7:0]: reserved, set to 0x00

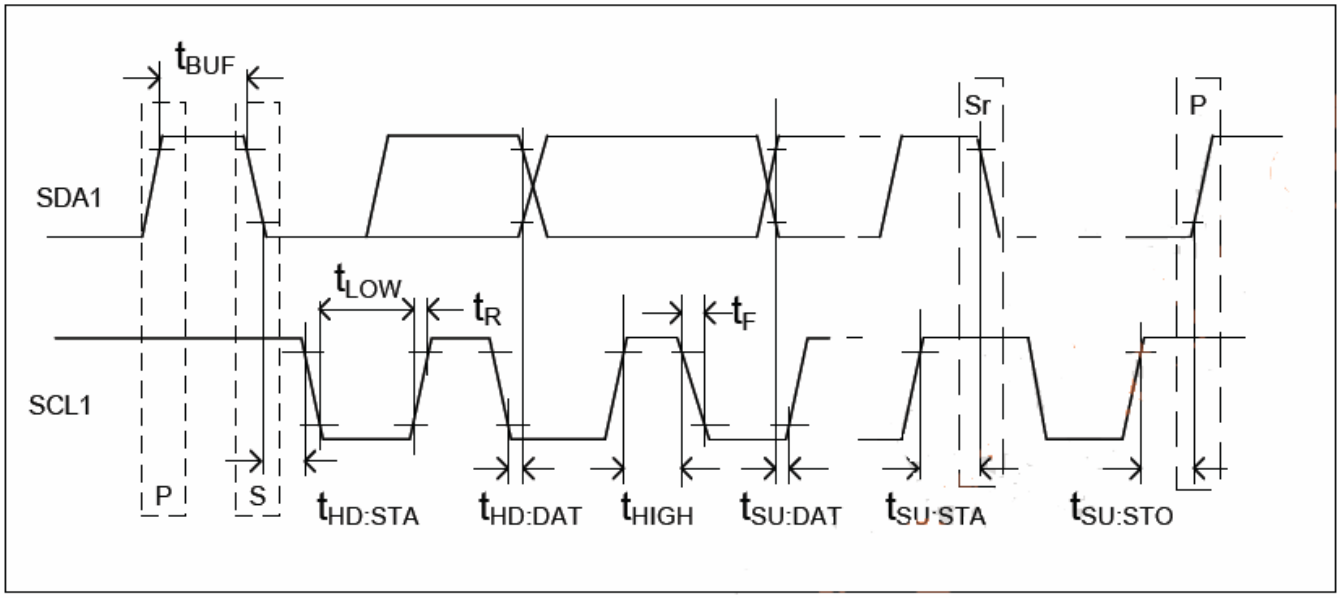
4. Environmental Specification of FEC IC

4-1	Temperature	- Operating: -10℃ to 70℃ - Storage: -40℃ to 150℃
4-2	Humidity	- Operating: less than 85% - Storage: less than 90%

5. General Specifications of The FEC IC.

<table>
<tr><th>No</th><th>Item</th><th>Specification</th></tr>
<tr><td>5-1</td><td>Symbol Rate</td><td>- QPSK/LDPC/BCH : 5MSps to 45MSps
- 8PSK/LDPC/BCH :10MSsps to 31MSps
- DVB QPSK : 2MSps to 65MSps</td></tr>
<tr><td>5-2</td><td>Code Rate</td><td>- QPSK : 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10
- 8PSK : 3/5, 2/3, 3/4, 5/6, 8/9, 9/10</td></tr>
<tr><td>5-3</td><td colspan="2">Automatic acquisition: ±10 acquisition range</td></tr>
<tr><td>5-4</td><td colspan="2">I2C bus interface</td></tr>
<tr><td>5-5</td><td>Link IC</td><td>AVL2108 (AVAILINK)</td></tr>
<tr><td>5-6</td><td>Data Output</td><td>Parallel or Serial(D7) Possible</td></tr>
<tr><td>5-7</td><td>Recommended Operating Voltage</td><td>
<table>
<tr><th>Symbol</th><th>Parameter</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>3.3VD</td><td>Supply Voltage</td><td>3.0</td><td>3.3</td><td>3.6</td><td>V</td></tr>
<tr><td>1.2VD</td><td>Supply Voltage</td><td>1.1</td><td>1.2</td><td>1.3</td><td>V</td></tr>
</table>
</td></tr>
<tr><td>5-8</td><td>Current Consumption</td><td>1. DVB-S and DTV Legacy
- 3.3VD: 20 mA(Typ.)
- 1.2VD: 360 mA(Typ.)
2. DVB-S2
- 3.3VD: 50 mA(Max.)
- 1.2VD: 1.03 A(MAX.)</td></tr>
</table>

6. I2C BUS Timing (I2C Seven Bit address is 0x0C)

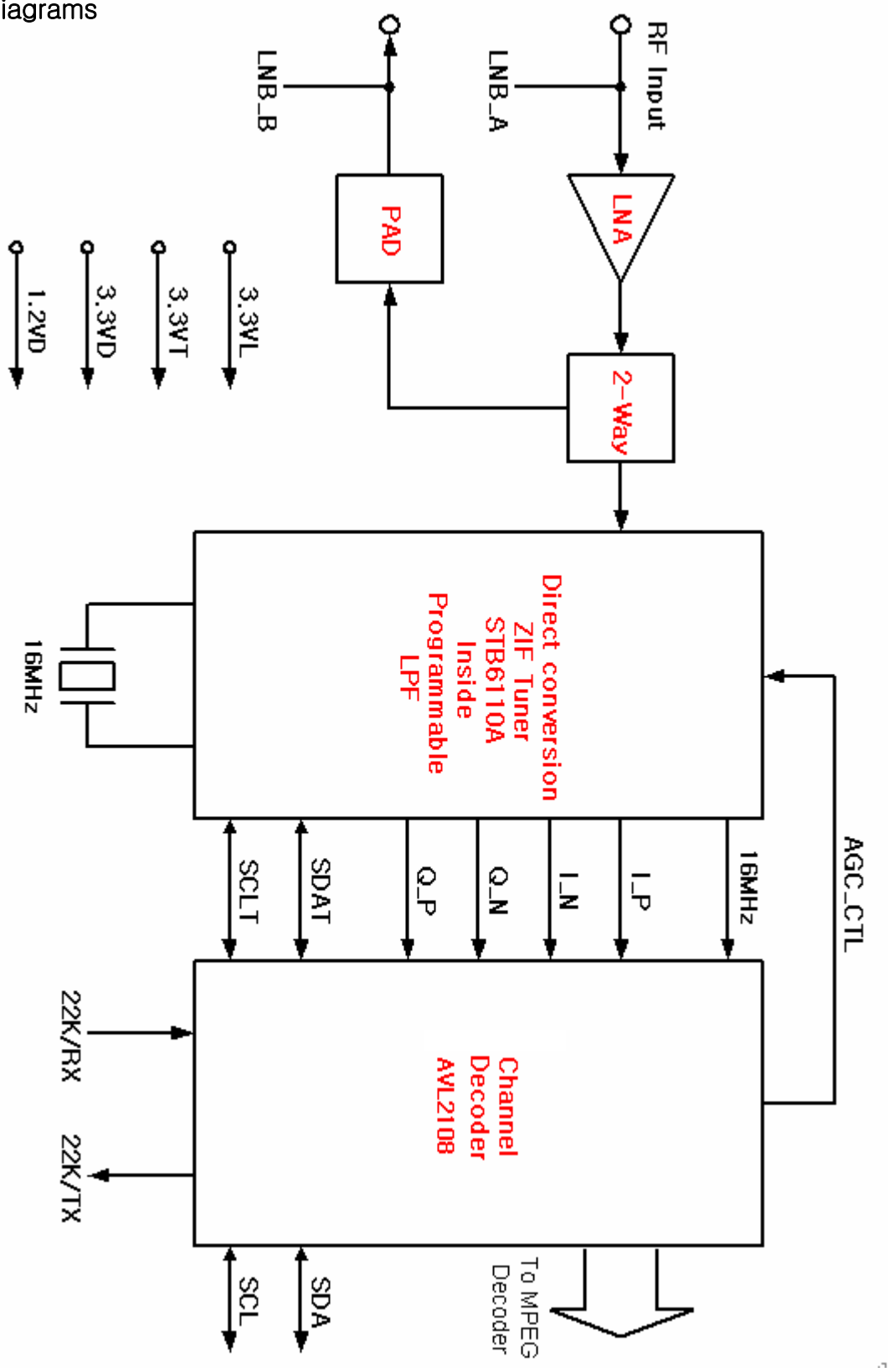


Where: S = Start
Sr = Restart, i.e., Start without stopping first.
P = Stop

Parameter	Symbol	Value		Unit
		Min	Max	
SCL1 Clock Frequency		0	400	KHz
Bus Free Time Between STOP and START		1300		ns
Hold time START condition		600		ns
LOW period of SCL1 Clock		1300		ns
HIGH period of SCL1 Clock		600		ns
SET-UP time for START condition		600		ns
DATA Hold time		0		ns
DATA set-up time		100		ns
Rise time of both SCL1,SDA1 signals		20	300[1]	ns
Fall time of both SCL1,SDA1 signals		20	300[1]	ns
SET-UP time for STOP condition		600		ns

1. The time depends on the external bus pull-up resistor and bus capacitance

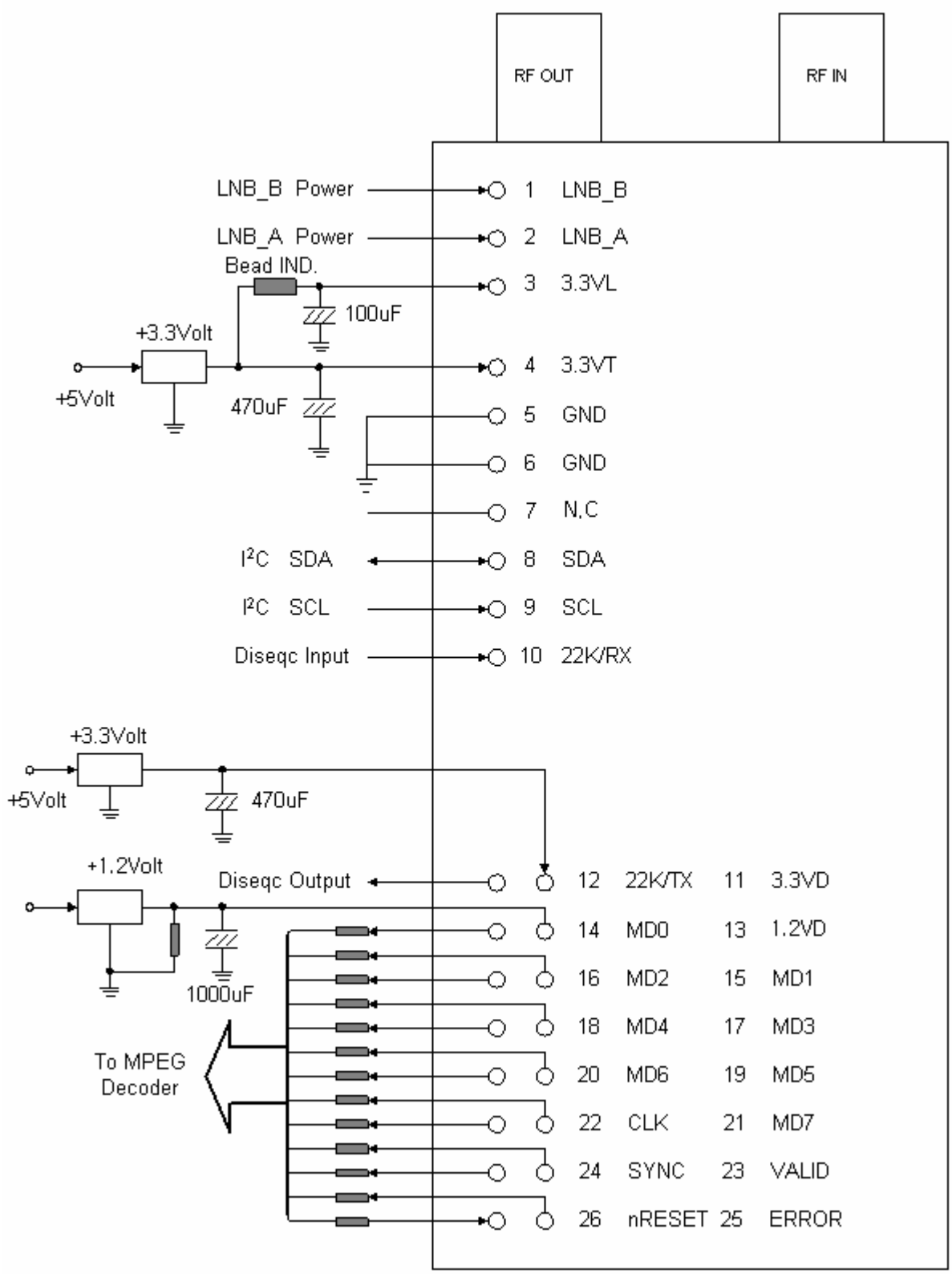
7. Block Diagrams



8. Pin Description

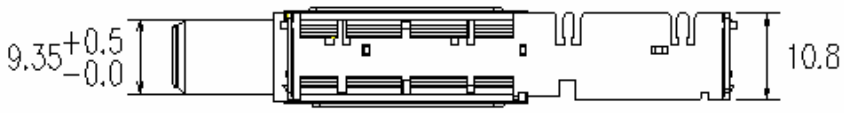
Pin No	Pin Name	Description
1	LNB_B	LNB B voltage supply
2	LNB_A	LNB A voltage supply
3	3.3VL	3.3Volt supply for RF-Amp (20 mA)
4	3.3VT	3.3Volt supply for ZIF IC
5	GND	Ground
6	GND	Ground
7	N.C	N.C
8	SDA	Serial programming interface data
9	SCL	Serial programming interface clock
10	22K/RX	LNB 22KHz Receive Signal
11	3.3VD	3.3Volt supply for LINK IC
12	22K/TX	LNB 22KHz Transmit Signal
13	1.2VD	1.2Volt supply for LINK IC
14~21	MD0~MD7	MPEG data interface data pins
22	CLK_OUT	MPEG data interface clock pin
23	VALID	MPEG data interface control pin_1(MOVAL)
24	SYNC	MPEG data interface control pin_2(MOSTART)
25	ERROR	ERROR OUT
26	nRESET	Chip reset

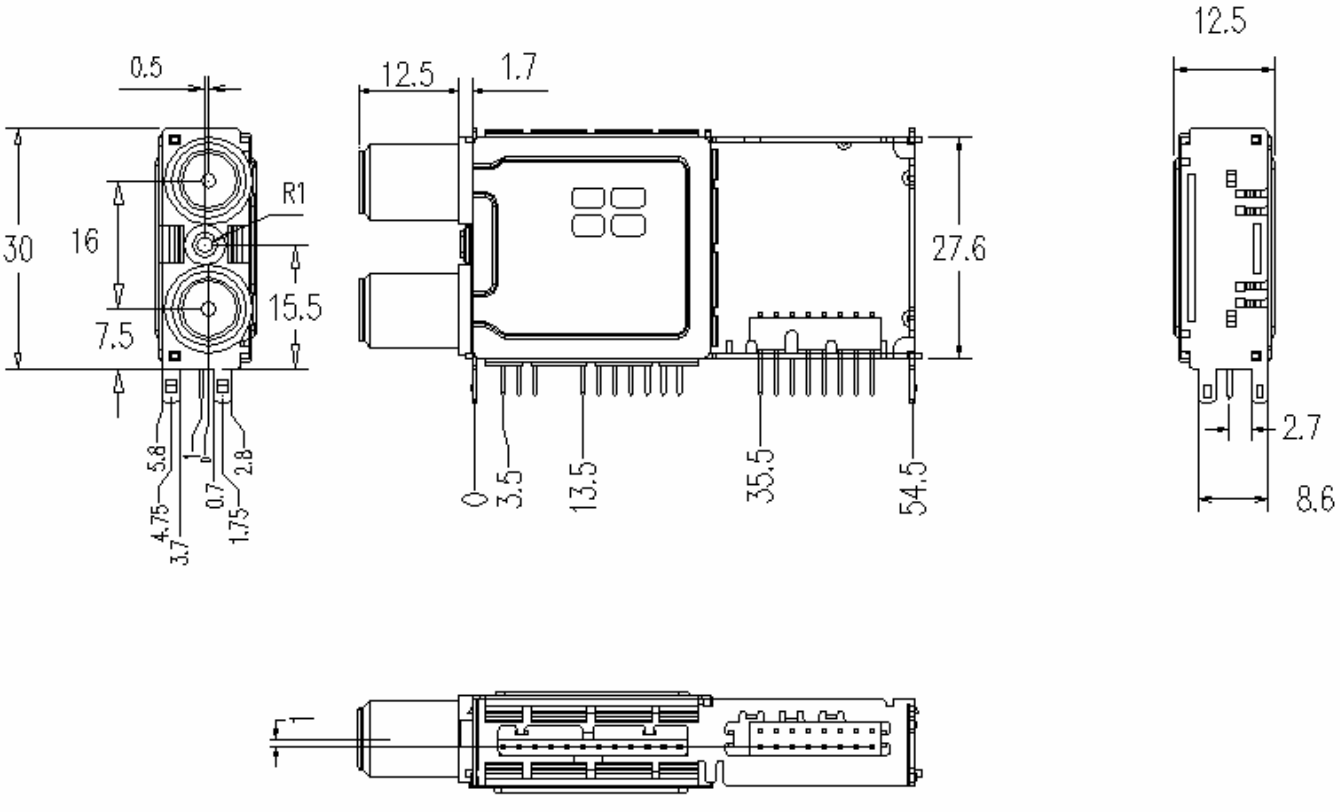
9. Application circuit



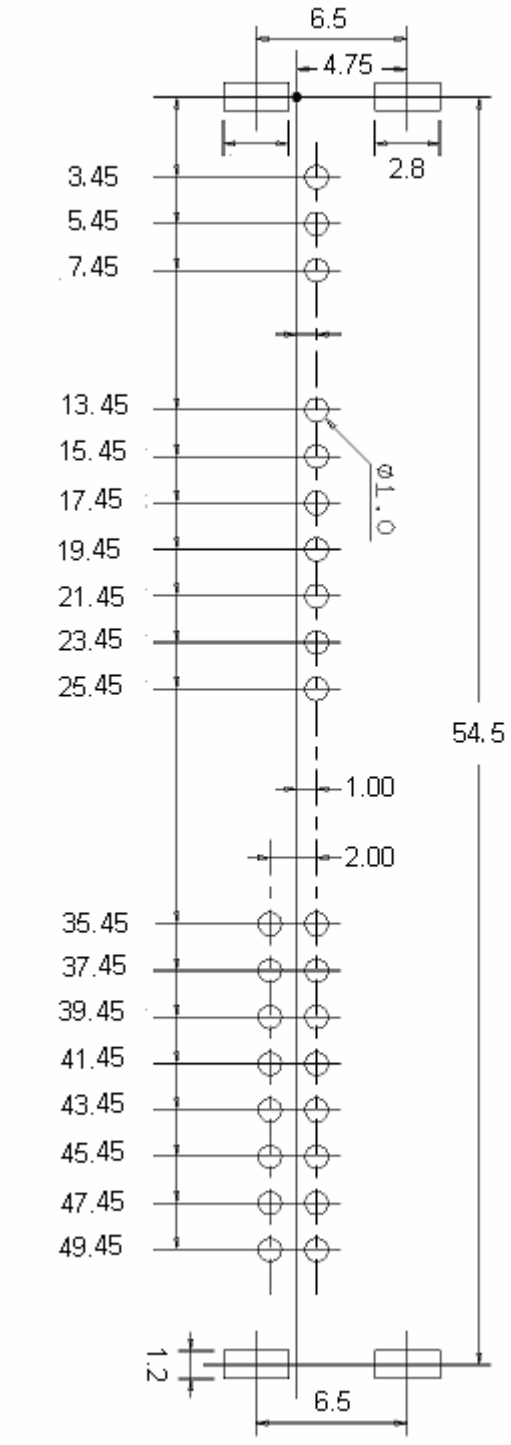
10. Outline Drawing

Vertical Chassis Type



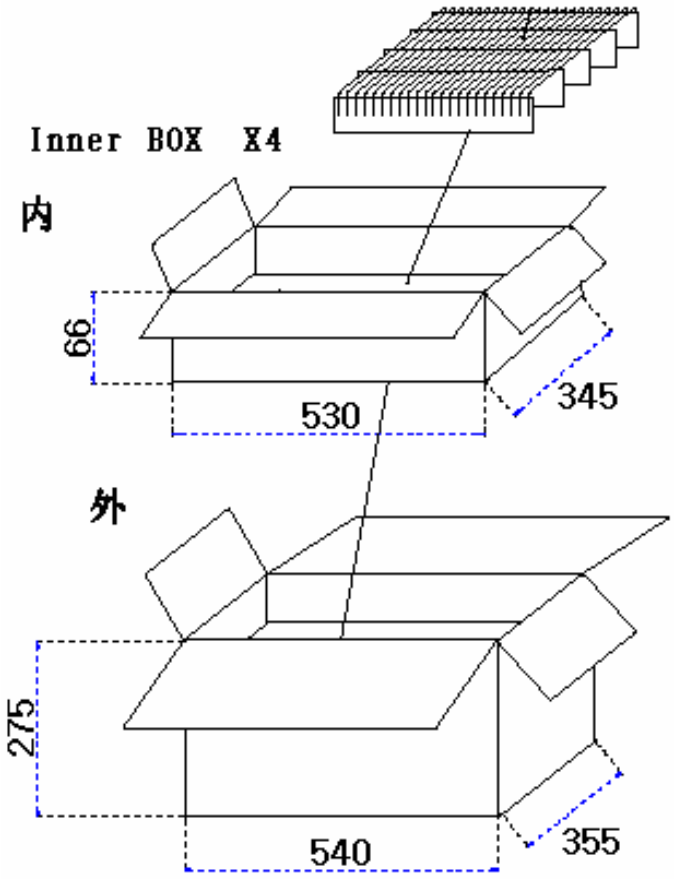


11. Mounting Drawing



12. Packing Details

Model	Weight	수량	Size	Carton weight
SP2237AVb	28g	400ea	540*355*275mm	14.36Kg



14. Electrostatic discharge

14.1 Test

Each front-end must be capable of normal performance after following tests:

ESD TEST

Test is performed with a voltage discharge From a 150 PF capacitor over a 330Ω series Resistor in the discharge path. There is a direct connect between the test probe head and the unit under test , using the test points and conditions detailed below:

- Test to pins 1 through 28

  4 successive ESD discharges of ±2KVDC between each pin and the front-end frame.

14.2 Handling

Anyone handling a front -end must wear a properly grounded anti -static Discharge bracelet to minimize ESD damage.

15. Heat load Test

- Measure the DUTs at room temperature
- Load the DUTs into chamber of the following conditions

  Temperature: 60℃

  Period: 160hrs

16. Cold Test

- Measure the DUTs at room temperature
- Load the DUTs into chamber of the following conditions

  Temperature: -20℃

  Period: 160hrs

17. Thermal shock

- Measure the DUTs at room temperature
- Load the DUTs into chamber of the following conditions

  Temperature: -40℃ for 60 min

  ↑ ↓

  110℃ for 60 min

  Period: 24 Cycle

18. Humidity load test

- Measure the DUTs at room temperature
- Load the DUTs into chamber of the following conditions

  Temperature: 40℃

  Humidity: 90%

  Period: 96hrs