SP3721A

6X DVD analog
Front End Chip

Confidential

Opto-Electronics & Systems Laboratories

Version 1.00 (June 2000)

SP3721A : 6x DVD Analog Front End Chip

Section 1 : INTRODUCTION

1.1 Features

- Supports AGC and an equalizer/filter for CD 3x to 32x and DVD 1x to 6x (with RX=8.2kohm)
- Low Power operation (350mW typical @5V)
- Bi-directional serial port register access
- Register programmed power management (Sleep mode <5mW)
- Power supply range (4.4 to 5.5 V)
- Small footprint 64-lead TQFP Package

Servo System

- Programmable equalizer for the Differential Phase tracking error Detection Circuit (DPD)
- 70 KHz bandwidth for the focus and PI circuits
- Input programmable gain control amplifier
- Servo algebra signals used for optical alignment, seeking, focusing and track following :
  - Pull-in Signal output
  - Mirror Signal output
  - Defect signal output/BCA (Burst Cutting Area) code output
  - Tracking Error Signal output
    Top Hold Push-Pull/3-beam tracking error detection
  - Differential Phase tracking error Detection
    Focusing Error Signal Output
    Center Error Signal Output

Channel

- 40 MHz bandwidth
- Supports individual RF inputs for DVD (differential or single-ended) and CD (Single-ended)
- Supports internal summing mode for RF signal for DVD and CD respectively
- Programmable attenuator (min:-24dB, 4-bit resolution)
- Fast attack/ decay mode for rapid AGC recovery
- Low drift AGC hold circuitry
- Temperature compensated, exponential control AGC
- Supports external and internal AGC hold control function
- Supports two ranges of Programmable cutoff frequency : 8 to 24MHz and 1 to 8MHz
- Programmable boost/equalization of 0 to 12dB
- Single-ended normal outputs for pulse qualification
- Differential normal signal outputs
- ? 20% Fc accuracy (Fc = 2 to 4 MHz)
- ? 15% Fc accuracy (Fc = 4 to 10 MHz, 8 to 24 MHz)
- Less than 2 % total harmonic distortion
- No external filter components required

Auto LASER Power Control

- Supports power mode selection
- Provides dual APC circuits for twin laser

VC Reference Voltage

- Provides a reference voltage output (VC) for external circuits
- Provides reference voltage input (VCI) for internal servo output reference voltage
- Provides reference voltage input (VCI2) for internal servo input reference voltage

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The SP3721A is a high performance BiCMOS single chip analog front-end IC that contains the servo functions, RF attenuator, AGC and programmable equalizer/filter for a DVD drive system and a dual auto laser power control circuit to support the twin pickups or twin lasers system. The programmable functions of the SP3721A are controlled through a bi-directional serial port and banks of internal registers.

This chip is packed in a 64-pin TQFP package.

1.2 Block Diagram

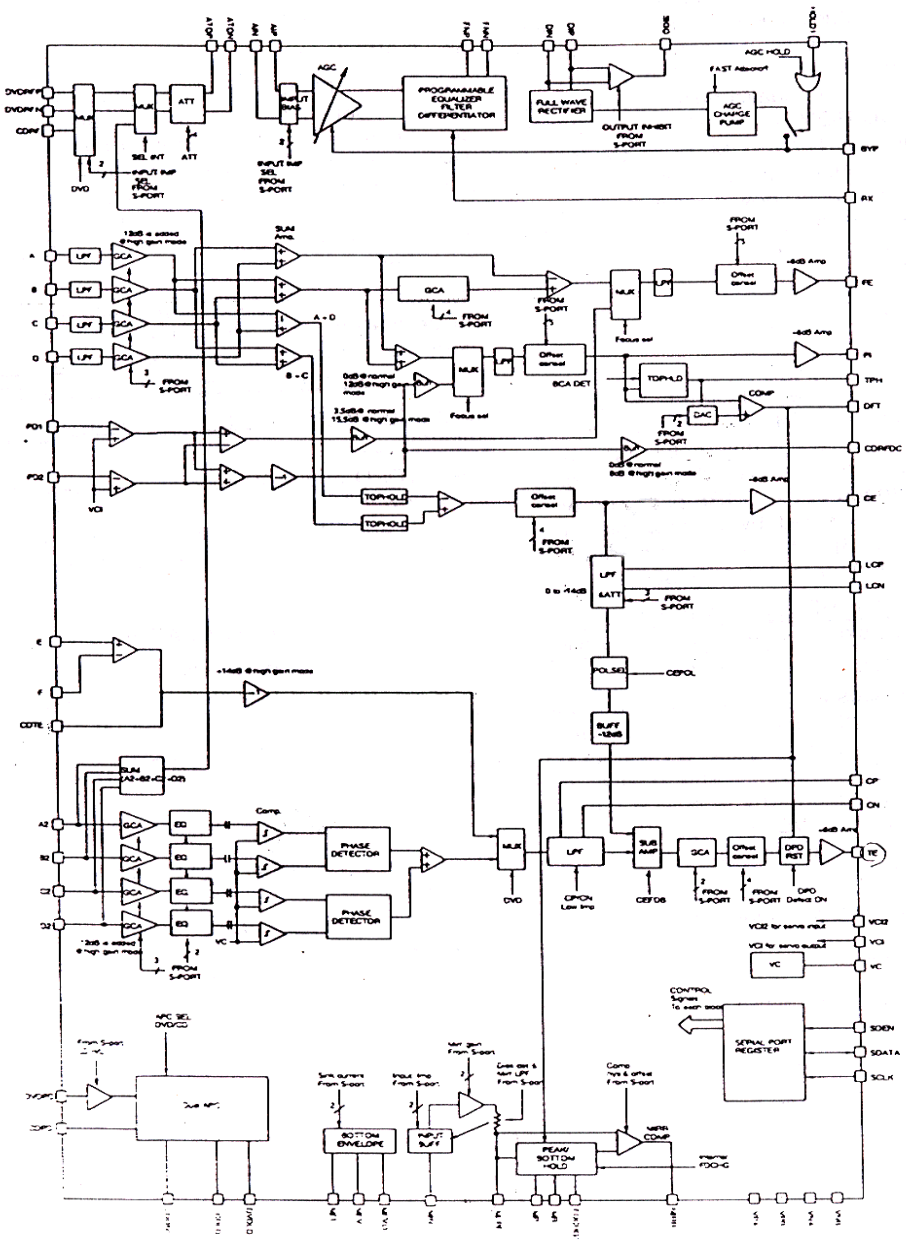

FIGURE 1 : Block Diagram

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Section 2: Pin Description

2.1 Pin Diagram

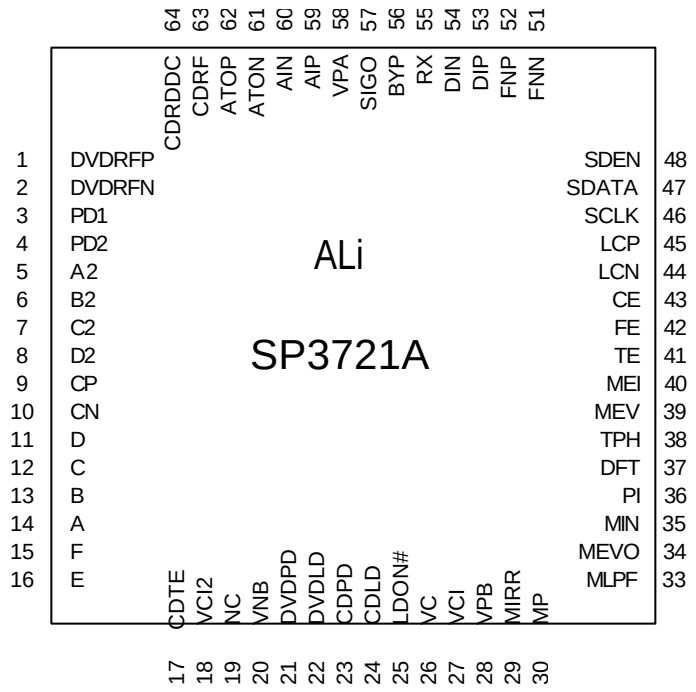

Figure 2-1 Pinout Diagram

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2.2 Pin Description Table:

Name	Number	Type	Description
Input Pins:			
DVDRFP, DVDRFN	1,2	I	**RF Signal Inputs**. Differential RF signal attenuator input pins.
CDRF	63	I	**RF Signal Input**. Single-ended RF signal attenuator input pin.
AIP, AIN	59,60	I	**AGC Amplifier Inputs**. Differential AGC amplifier input pins.
DIP, DIN	53,54	I	**Analog inputs for RF Single Buffer**. Differential analog inputs to the RF single-ended output buffer and full wave rectifier.
FDCHG#	32	I	**Low Impedance Enable**. A TTL compatible input pin that activates the FDCHG switches. A low level activates the switches and the falling edge of the internal FDCHG triggers the fast decay for the MIRR bottom hold circuit. (open high)
HOLD1	49	I	**Hold Control**. A TTL compatible control pin which, when pulled high, disables the RF AGC charge pump and holds the RF AGC amplifier gain at its present value. (open high)
A,B,C,D	14-11	I	**Photo Detector Interface Inputs**. Inputs from the main beam Photo detector matrix outputs.
A2,B2,C2,D2	8-5	I	**Photo Detector Interface Inputs**. AC coupled inputs for the DPD from the main beam Photo detector matrix outputs.
E,F	16-15	I	**CD tracking Error Inputs**. Inputs from the CD photo detector error outputs.
PD1,PD2	3-4	I	**CD Photodetector Interface Inputs**. Inputs from the CD photo detector error outputs.
MEI	40	I	**Mirror Envelope Input**. The SIGO envelope input pin.
MIN	35	I	**RF signal Input for Mirror**. AC coupled inputs for the mirror detection circuit from the pull-in signal output. (PI)
DVDPD	21	I	**APC Input**. DVD APC input pin from the monitor photo diode.
CDPD	23	I	**APC Input**. CD APC input pin from the monitor photo diode.
LDON#	25	I	**APC Output On/Off**. APC output control pin. A low level activates the LD output. (open high)
Output Pins:			
ATOP/ATON	62,61	O	**Differential Attenuator Output**. Attenuator outputs.
FNP, FNN	52,51	O	**Differential Normal Output**. Filter normal outputs.
SIGO	57	O	**Single Ended Normal Output**. Single-ended RF output.
CDRFDC	64	O	**CD RF Signal Output**. Single ended CD RF summing output.
FE	42	O	**Focusing Error Signal Output**. Focus error output reference to VCI.
TE	41	O	**Tracking Error Signal Output**. Tracking error output reference to VCI.
CE	43	O	**Center Error Signal Output**. Center error output reference to VCI.
MEVO	34	O	**SIGO Bottom Envelope Output**. Bottom envelope for Mirror detection.
DFT	37	O	**Defect Output**. Pseudo CMOS output. When a defect is detected, the DFT output goes high. Also the servo AGC output can be monitored at this pin, when CAR bits 7-4 are '0011'.
MIRR	29	O	**Mirror Detect Output**. Mirror Detect comparator output. Pseudo CMOS output.
PI	36	O	**Pull-in Signal Output**. The summing signal output of A,B,C,D or PD1, PD2 for mirror detection. Reference to VCI.
DVDLD	22	O	**APC output**. DVD APC output pin to control the laser power.
CDLD	24	O	**APC output**. CD APC output pin to control the laser power.

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Pin Description Table (continued) :

Name	Number	Type	Description
Analog Pins:			
BYP	56	I/O	The RF AGC integration capacitor CBYP, is connected between BYP and VPA.
CP	9	I/O	**Differential Phase tracking LPF pin**. An external capacitance is connected between this pin and the CN pin.
CN	10	I/O	**Differential Phase tracking LPF pin**. An external capacitance is connected between this pin and the CP pin.
LCP	45	-	**Center Error LPF pin**. An external capacitance is connected between this pin and the LCN pin.
LCN	44	-	**Center Error LPF pin**. An external capacitance is connected between this pin and the LCP pin.
MP	30	-	**MIRR signal Peak hold pin**. An external capacitance is connected to between this pin and VPB.
MB	31	-	**MIRR signal Bottom hold pin**. An external capacitance is connected between this pin and VPB.
MEV	39	-	**Sigo Bottom Envelope pin**. An external capacitance is connected between this pin and VPB.
CDTE	17	-	**CD Tracking**. E-F Opamp output for feedback.
TPH	38	-	**PI Top Hold pin**. An external capacitance is connected between this pin and VPB.
VC	26	-	**Reference Voltage output**. This pin provides the internal DC bias reference voltage (+2.5V fix). Output impedance is less than 50ohms.
VCI	27	-	**Reference Voltage Input**. DC bias voltage input for the servo input reference.
VCI2	18	-	**Reference Voltage Input**. DC bias voltage input for the servo input reference.
RX	55	-	**Reference Resistor Input**. An external 8.2 kohm, 1% resistor is connected from this pin to ground to establish a precise PTAT (proportional to absolute temperature) reference current for the filter.
MLPF	33	-	**MIRR signal LPF pin**. An external capacitance is connected between this pin and VPB.
NC	19	-	No Connect.
Serial Port Pins:			
SDEN	48	I	**Serial Data Enable**. Serial Enable CMOS input. A high level input enables the serial port. (Not to be left open).
SDATA	47	I/O	**Serial Data**. Serial data bi-directional CMOS pin. NRZ programming data for the internal registers is applied to this input. (Not to be left open).
SCLK	46	I	**Serial Clock**. Serial Clock CMOS input. The clock applied to this pin is synchronized with the data applied to SDATA. (Not to be left open).

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Pin Description Table (continued)

Name	Number	Type	Description
Power Pins:			
VPA	58		**Power.** Power supply pin for the RF block and serial port.
VPB	28		**Power.** Power supply pin for the servo block.
VNA	50		**Ground.** Ground pin for the RF block and serial port.
VNB	20		**Ground.** Ground pin for the servo block.

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2.3 Numerical Pin List

Pin No.	Pin Name	Type
1	DVDRFP	I
2	DVDRFN	I
3	PD1	I
4	PD2	I
5	A2	I
6	B2	I
7	C2	I
8	D2	I
9	CP	-
10	CN	-
11	D	I
12	C	I
13	B	I
14	A	I
15	F	I
16	E	I
17	CDTE	-
18	VCI2	-
19	NC	-
20	VNB	-
21	DVDPD	I
22	DVDLD	O
23	CDPD	I
24	CDLD	O
25	LDON#	I
26	VC	-
27	VCI	-
28	VPB	-
29	MIRR	O
30	MP	-
31	MB	-
32	FDCHG#	I
33	MLPF	-
34	MEVO	O
35	MIN	I
36	PI	O
37	DFT	O
38	TPH	-
39	MEV	-
40	MEI	I
41	TE	O
42	FE	O
43	CE	O
44	LCN	-
45	LCP	-

Pin No.	Pin Name	Type
46	SCLK	I
47	SDATA	I/O
48	SDEN	I
49	HOLD1	I
50	VNA	-
51	FNN	O
52	FNP	O
53	DIP	I
54	DIN	I
55	RX	-
56	BYP	-
57	SIGO	O
58	VPA	-
59	AIP	I
60	AIN	I
61	ATON	O
62	ATOP	O
63	CDRF	I
64	CDRFDC	O

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2.4 Alphabetical Pin List:

Pin No.	Pin Name	Type
14	A	I
5	A2	I
60	AIN	I
59	AIP	I
61	ATON	O
62	ATOP	O
13	B	I
6	B2	I
56	BYP	-
12	C	I
7	C2	I
24	CDLD	O
23	CDPD	I
63	CDRF	I
64	CDRFDC	O
17	CDTE	-
43	CE	O
10	CN	-
9	CP	-
11	D	I
8	D2	I
37	DFT	O
54	DIN	I
53	DIP	I
22	DVDLD	O
21	DVDPD	I
2	DVDRFN	I
1	DVDRFP	I
16	E	I
15	F	I
32	FDCHG#	I
42	FE	O
51	FNN	O
52	FNP	O
49	HOLD1	I
44	LCN	-
45	LCP	-
25	LDON#	I
31	MB	-
40	MEI	I
39	MEV	-
34	MEVO	O
35	MIN	I
29	MIRR	O
33	MLPF	-

Pin No.	Pin Name	Type
30	MP	-
19	NC	-
3	PD1	I
4	PD2	I
36	PI	O
55	RX	-
46	SCLK	I
47	SDATA	I/O
48	SDEN	I
57	SIGO	O
41	TE	O
38	TPH	-
26	VC	-
27	VCI	-
18	VCI2	-
50	VNA	-
20	VNB	-
58	VPA	-
28	VPB	-

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Section 3 : Function Description

The SP3721A implements a high performance analog front-end, including RF summing amplifier, input attenuator, AGC, programmable active equalizer/filter, and a servo block. The attenuator, AGC and programmable equalizer/ filter support a wide bandwidth from CD-ROM 1x to 32x (RX=8.2kohm) speed signal rate and DVD ROM 1x to 32x (RX=8.2 kohm) speed signal rates and DVD-ROM 1x to 6x speeds. The servo block includes mirror detection, defect detection, dual auto laser power control, tracking zero crossing, focus error, center error and tracking error detection circuits. (Fig. 1)

3.1 Input Interface

3.1.1 RF Interface

The SP3721A provides the RF interface for both DVD and CD signals. DVD signals can be AC coupled into the device through the differential input pins DVDRFP and DVDRFN, while the CD signal interface is single-ended through the CDRF pin. The type of interface can be selected by programming the CD/DVD bit (PDCR bit 3). This bit should be set to 1 for the DVD interface, and 0 for the CD interface.

Input impedance of the RF signal is programmable from 10kohm to 40 kohm, single-ended and is controlled by the RF input IMP bits (RFCR bits 7,6).

This device also provides an internal summing mode for the RF signal. In this mode, an RF signal is internally generated by summing the DVD tracking servo inputs (A2, B2, C2, D2). The device will process this signal and ignore any signals at the RF interface pins (DVDRFP, DVDRFN, CDRF). This mode can be enabled by setting the Internal RF SEL bit (SIGR bit 3) to 1.

The following table outlines the control bits for the RF signal.

Internal RF SEL (SIGR bit 3)	**CD/DVD (PDCR bit3)**	**RF signal**
0	0	CDRF
0	1	DVDRFP-DVDRFN
1	x	A2+B2+C2+D2

Signal equalization is provided by a programmable filter, a wide bandwidth full wave rectifier, and a dual rate charge pump.

3.1.2 Servo Interface

The SP3721A also provides the voltage-input interface for photo detector signals used in the servo block to detect center errors, focusing errors and tracking errors. These signals include the output from the quad cell photo detectors. (A, B, C, D) and CD photo detectors (E, F, PD1, PD2) which are directly connected from the pick-up and require external IV or (OEIC) converters.
The A2, B2, C2, D2 inputs are provided for the Differential Phase tracking error detection (DPD) used in the DVD mode (see Tracking Error Detection). These signals are the AC coupled version of the, B, C, D signals. All of these servo inputs have a 10 kohm input impedance.
The DVDPD and CDPD inputs are provided for the Auto Power Laser Control circuits used to monitor the DVD and CD laser, respectively (see Auto Laser Power Control). These inputs are high impedance pins.

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3.2 Programmable Attenuator

The RF signal is differentially fed into an input attenuator, which is provided for the input signal swing variations of the RF signal dependent on the layer and media. The maximum input range is 1.1 Vpp and the programmable range is 1 to 1/16 by 1/16 step. (min. 24dB)

ATT Gain = (16-ATT)/16 [V/V]

where, ATT is the higher 4-bit word in the Attenuator Gain Register (ATGR)

The differential output of the attenuator, as seen at the ATOP, ATON pins, should be AC coupled to the inputs of the AGC at the AIP, AIN pins.

3.3 AGC Circuit

The input stage to the AGC includes a programmable input impedance. This impedance can be programmed to be from 7.5 kohms to 20 kohms, single-ended by the AGC input bits (RFCR bits 5,4).
The gain of the AGC amplifier is controlled by the voltage (Vbyp) stored on the BYP hold capacitor (Cbyp). A dual rate charge pump drives Cbyp with currents that depend on the instantaneous differential voltage at the amplifier gain, while the decay currents increase Vbyp which increase the amplifier gain.

The AGC gain is 20 db from AIP/AIN to FNP/FNN, when the Vbyp is set to the VRC voltage, where VRC=VPA-2.35V (internal bandgap reference voltage).
When the signal at DIP/DIN is greater than 100% of the AGC level (typical : 1.0 Vppd), the nominal attack current of 0.18 mA is used to reduce the amplifier gain.

If RFCR bit 3 is set to 1, a fast attack mode is entered when the signal at DIP/DIN is greater than 125% of the AGC level. In this mode, a fast attack current of 8 times the nominal attack current (0.18 mA) is used to reduce the amplifier gain rapidly. This dual rate approach allows the AGC gain to be quickly decreased when it is too high/low yet minimizes distortion when the proper AGC level has been acquired.

A constant decay current of 4 uA acts to increases the amplifier gain when the signal at DIP/DIN is less than the AGC level. The large ratio (0.18 mA:4uA) of the nominal attack and nominal decay currents allow the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value.

3.3.1 AGC Mode Control

When the RF block is powered down, Vbyp will be held constant subject to leakage currents only.
External control for enabling the dual rate charge pump is provided. Driving the Hold function high, forces the dual rate charge pump output current to zero. In this mode, Vbyp will be held constant subject to leakage currents only. The Hold function is asserted when the Hold1 pin is high.

In addition, the AGC can also be placed in a Hold mode when the RF AGC Hold bit (CER bit7) is set to 1.

3.4 Programmable Filter Circuit Description

The SP3721A programmable filter consists of an electronically controlled seven-pole, low pass filter output. Programmable bandwidth and boost/equalization is provided by the internal 7-bit control DACs. Differentiation pulse slimming equalization is accomplished by a two-pole, low pass filter with a two-pole, high pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations. The single-ended normal signal output buffer (SIGO) is added for external signal qualification. This SIGO output is disabled when the SIGO Off bit (FBCR bit 7) is set to 1. The filter implements a 0.05 degree equi-ripple linear phase response.
The normalized transfer functions (i.e., Wc=2 ?fc =1) are:
Vnorm/Vi =[(-Ks2+1.31703)(13.65205)/D(s)]xAN
where :
(s) = $(S^2+1.68495s+1.31703)(S^2+1.54203s+2.95139)^D$

$(S^2+1.14558s+5.37034)(s+0.86133)$,
AN is adjusted for a gain of 10 at fs =(2/3)fc.

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3.4.1 Filter Operation

The outputs of the AGC are internally coupled to inputs of the filter. The programmable bandwidth and boost/equalization features are controlled by internal DACs and the registers are programmed through the serial port. The current reference for both DACs is set using a single 8.2 kohm external resistor connected from the RX pin to ground. The voltage at the RX pin is proportional to the absolute temperature (PTAT), hence the current for the DACs is a PTAT referenced current.

3.4.2 Bandwidth Control

The programmable bandwidth and cutoff range are set by the filter cutoff DAC. This DAC value is controlled by FCCR register. The DAC value can be programmed as follows:

fc = (-0.00052 xFCDACxFCDAC) + (0.28707xFCDAC) +0.535 (MHz) at Fc range 8MHz? fc? 24MHz

fc = (-0.00016xFCDACxFCDAC) + (0.12020xFCDAC) +0.165 (MHz) at Fc range 2MHz? fc? 10MHz

where FCDAC = FCCR register value

The Filter Cutoff control register (FCCR) is used to determine the filter's –3dB cutoff frequency. The SP3721A provides a filter maximum range control register bit. When the FC range bit (FCCR bit 7) is set high, the maximum cutoff frequency is 10 MHz. When this bit is low, the maximum cutoff frequency is 24MHz. The filter cutoff set by the internal DAC is the unboosted –3db frequency. When boost/equalization is added, the actual –3 dB point will move out. Table 1 provides information on boost versus –3dB frequency.

Table 3-1. 3 dB cutoff frequency v. boost magnitude.

Boost	Fc 10MHz mode	Fc 24MHz mode
(dB)	Fc (-3dB)	Fc(-3dB)
0	1.00	1.00
1	1.28	1.28
2	1.52	1.53
3	1.73	1.75
4	1.93	1.96
5	2.11	2.14
6	2.28	2.31
7	2.43	2.46
8	2.56	2.59
9	2.68	2.71
10	2.77	2.80
11	2.85	2.87
12	2.92	2.93

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3.4.3 Boost/Equalization Control

The programmable equalization is also controlled by an internal DAC. The 7-bit Filter Boost Control Register (FBCR) determines the amount of equalization that will be added to the –3db cutoff frequency, as follows:
Boost = 20 log[(N1xFBDAC) +(N2xFBDACxFCDAC)+(N3xFBDACxFBDAC)+1](dB)
N1=0.0341, N2=9.3e-5 , N3=1.8e-5 at Fc range 8MHz?fc?24MHz
N1=0.0333, N2=-5.11e-5, N3=2.08e-5 at Fc range 2MHz?fc?10MHz

Where FBDAC =FBCR bits 6-0 value, FCDAC=FCCR bits 6-0 value.

3.5 Servo Block Modes and Control

The SP3721A servo block includes focusing error detection, tracking error detection, center error detection, defect detection, tracking zero crossing output, mirror detection and dual auto laser power control circuits.

The servo interface has been designed to accommodate both single laser and twin-laser pickups. In the single-laser pickup mode, [selected by setting the Focus One-Beam Sel bit (CAR bit3) to 1], it is assumed that the signals from the quad cell photo detectors (A,B,C,D) are used for the generation of all the servo signals in both the CD and DVD modes (except for the tracking error signal in CD mode).
In the twin-laser pickup mode, (selected when Focus One-Beam Sel is 0), it is assumed that the quad cell photo detectors are still used to generate servo signals in the DVD mode, but the CD mode utilizes signals from a separate set of inputs, PD1 and PD2, to generate most of the servo signals. In this mode, the center error signal (CE) is determined from the CEIN input.

Table 3-2 below summarizes the controlling bits and the corresponding input signals used to generate the servo signals.

The device also offers a high gain mode to support rewritable disk reading. This mode is asserted when the High Gain bit (CBR bit6) is set high.

3.5.1 Focusing Error Detection

The SP3721A provides two sets of circuits for focus error detection to support both the single laser and twin laser pickups. In the single laser pickup mode, [selected by setting the Focus One Beam Sel bit (CAR bit3) to 1], the device provides a focus error detection circuit for a cylindrical lens using astigmatism. The equation for this scheme is:
1.4[Kf(A+C)-(B+D)]
The focusing error asymmetry balance can be controlled by Kf. The gain dynamic range of Kf is ?4dB with 4-bit resolution (FTGR bits 7-4, see table 7)
In twin laser pickup mode, the focusing error detection circuit equation is:
Kfcd(PD1-PD2)

The gain, KfCD, is a fixed value at 9.5dB. In the high gain mode, [selected when the High gain bit (CBRbit6) is set to 1], this gain is increased to 21.5dB.

The focusing error signal can be seen on the FE pin. The output signal swing is VC?1.0V (max)

This device also provides a programmable focusing DC offset cancelling circuit. Up to ?690 mV of offset can be added to the signal by programming the FEOFFSET bits (CCR bits4-0)(see table20)

Table 3-2. Mode Control

Mode	CD/DVD (PDCR bit3)	Focus One-Beam (CARbit3)	Focus Error (FE)	Tracking Error (TE)	Center Error (CE)
DVD	1	1	A,B,C,D	A2,B2,C2,D2	A,B,C,D
CD (single laser)	0	1	A,B,C,D	E,F	A,B,C,D
CD(double laser)	0	0	PD1,PD2	E,F	A,B,C,D

3.5.2 Tracking Error Detection

The SP3721A provides two sets of tracking error detection logic, one for DVD tracking, the other for CD tracking. In the DVD mode, the tracking error signal is implemented through a differential phase detection circuit. Equalizers are provided at each of the DPD inputs (A2,B2,C2,D2). The outputs of these equalizers are AC coupled into comparators through an internal 100KHz network. The phase differentiation signals between the A2 and B2, C2 and D2 are summed to generate the tracking error signal.

In the CD mode, the tracking error signal is detected from the F-E function. The gain from the CDTE1 to TE is +6dB. In high gain mode (CBR bit6=1), an additional 14dB is added to the signal.

The tracking error signals for both DVD and CD are fed into a multiplexer. The output of this multiplexer is selected by the CD/DVD bit (PDCR bit3). This bit should be set to 1 for DVD tracking or 0 for CD tracking. The selected signal then goes through a low pass filter whose cutoff frequency is determined by a programmable impedance, programmed by the CD/DVD (PDCR bit3) and CP/CN (CDR bit5) bits and an external capacitor connected between the CP and CN pins. An output gain control amplifier is provided to increase the signal by up to 6.8dB. This gain is programmable by the TRGAIN bits (FTGR bits1,0)(see Table7). A programmable tracking DC offset cancelling circuit with ?350mV range is also provided. The offset is controlled by the TROFFSET bits (TRCR bits 3-0).
The tracking error circuit also includes provisions for offset compensation due to lens shift. This is implemented by subtracting an appropriate integrated and attenuated center error (CE) component from the TE signal in DPD mode. This provision is available when the CE FDB bit (CBR bit 4) is set to 1. The polarity and attenuation of the CE component is controlled by the CE POL bit (CBR bit3) and CE ATT bits (CBR bits2-0), respectively.

An additional function has been provided to prevent false tracking error signals during a defect. This function forces the TE signal to the VCI voltage during a defect, (defined by a high level on the DFT pin) and is enabled by setting the DFT mask TE bit (CBR bit3) to 1.

The tracking error signal can be observed at the TE pin.

CP/CN Impedance Selection

CP/CN CDR bit5	CD/DVD (PDCR bit3)	Impedance (Kohm)
0	0	30
0	1	20
1	X	10

3.5.3 Center Error Detection

The SP3721A provides a center error detection circuit to support single or twin laser pickups. In the single laser pickup mode, the center error is generated by taking the subtracting output from the top hold signals of A+D and B+C and adding 6dB.

This device also provides ?840mV center error DC offset cancelling circuit controlled by the CEOFFSET bits (TRCR bits 7-4).

3.5.4 Mirror Detection

The Mirror Detection circuit accepts one of two inputs, the bottom envelope of the SIGO signal (single-ended output of the RF filter) or the PI signal.

SIGO can be directly coupled to the MEI pin to bottom envelope the signal. The sink current of this envelope can be programmed from 20uA to 200 uA and is controlled by the MRENV CURNT bits (CAR bits1-0). The enveloped signal is output from the MEVO pin and should be AC coupled into MIN for mirror detection.

PI can also be used as an input to the Mirror circuit. The signal should be AC coupled into the MIN pin.

The input stage at MIN includes a programmable input impedance control circuit and gain amplifier. The input impedance is programmable from 5 to 45 kohms selected by the MIRR Input_Z sel bits (MRCR bits1-0, see table 11). The gain amplifier can be programmed from 3 to 12 dB by the MIRR GAIN bits (FTGR bits 3-2).

The amplifier output is fed into a 1st order low pass filter which consists of an internal impedance and an external capacitor connected between the MLPF pin and the VPB supply. The impedance can be programmed using the MLPF bits (MRCR bits 3-2) to set the cutoff frequency of the LPF network. With an external capacitor of 160 pf, the cutoff frequency can be adjusted from 50KHz to 400KHz.

The low pass filter output is fed into the hysteresis comparator and peak/bottom hold circuits. The time constant of the peak/bottom hold is determined by sink currents and external capacitors connected between the MP and MB pins and the VPB supply. Both peak and bottom sink currents are set to 14.5 uA in the normal mode.

When the FDCHG pin is low, the bottom sink current is set to 5mA. This Fast Discharge mode is provided for fast recovery from defect. In addition, an internal fast discharge mode is also provided and is enabled when FDCHG is high and MRCR bit4 =1.

The comparator reference level can be selected by the MRCOMP OFFSET bits (MRCR bits6-5). The MRCOMP HYS-LOW bit (MRCR bit 7) controls the amount of hysteresis in the comparator. When this bit is 0, the hysteresis is ?100mV. When this bit is set to 1 the hysteresis is ?50mV. The comparator output is a pseudo CMOS output and can be observed at the MIRR pin.

The SP3721A also provides a disk discrimination function for the CD or DVD using the mirror circuit. This function is available when the DISK DET bit (CCR bit7) is set to 1. This function makes use of difference in distance between the disk surface to signal layer of the media. The circuit measures the time difference between the signal from the reflectivity of the surface of the media, which is relatively small, and the actual data signal. The signal layer depth from the surface of the media is 1.2 mm for a CD and 0.6mm for a DVD. Therefore the corresponding time difference between the surface layer signal and data signal should be longer for a CD than a DVD.

In this mode, the mirror input impedance is changed to 300 kohms, the peak detector gain is changed to 18 dB or 8dB, selected by the DISK DET HIGH GAIN bit (CCR bit 6), the MP/MB sink currents are changed to 3.5uA, and the impedance for the MLPF is changed to 100 kohms.

3.5.5 Defect Detection

The defect output pin (DFT) is provided for defect detection and BCA (Burst Cutting Area) code detection.

Defect detection is implemented by holding the peak value of the Pull-in (PI) signal and comparing it to a programmed level. An external capacitor connected between the TPH pin and ground and a 5 uA sink current are used to hold the peak value of the PI signal. The reference level can be programmed as a percentage of the peak of the PI signal referenced to VCI. The reference level can be set by programming the Defect bits (CDR bits7-6). The DFT comparator has +100mV hysteresis. This means that the PI signal level has to be 100mV above the slice level in order for the DFT output to remain low.

When the BCA DET bit (CBR bit 7) is set to 1, the Burst Cutting Area (BCA) code detection is asserted. In this mode, the peak hold sink current is changed to 50uA. The polarity logic of the DFT output is also reversed when the signal falls below the programmed level the DFT. In this case, the DFT output will go low when the PI signal is below the programmed level.

3.5.6 Auto Laser Power Control

The SP3721A provides dual APC circuits for a DVD laser and a CD laser. The DVD APC circuit has a selectable high or low power mode of operation. In high power mode, also denoted as low gain mode, the gain of the APC circuit is set at 21.4 V/V. In this mode, a 150mV PD input voltage is centered resulting in a 3V output at the LD output. In low power mode, or high gain mode, the gain is 36.4 V/V. In this mode, a 250mV PD input voltage is centered resulting in a 3V output at the LD output. The CD APC circuit is fixed at low power or high gain mode, resulting in a gain of 36.4 V/V.

Only one APC circuit can be operating at any given time. When either or both of the APC circuits is off, the output will be fixed to the supply voltage. Operations of the APC circuits are controlled by the control bits APC select (CCR bit5), LDH/L (CER bit 5), and the LDON pin as defined in the following table:

APC selection

APC select	LDH/L	LDON	DVD APC Gain (V/V)	CD APC Gain (V/V)
X	x	1	Off	Off
0	0	0	36.4	Off
0	1	0	21.4	Off
1	X	0	Off	36.4

The LDON pin must be high for either of the APC circuits to be operating. The APC select bit selects which of the APC circuit will be operating while the LDH/L bit selects the gain the APC only if the DVD mode is selected.

3.6 Operating modes and Control

The SP3721A has several operating modes that support CD/VCD signal equalization, focus and tracking errror detection, and power management functions.

3.6.1 Test Mode Control

The SP3721A provides a test mode for measuring some circuit parameters. When the TMS3 to TMS0 (CAR bit 7,6,5,4) are set low, the test mode is disabled (see table 17). When one of each of these bits is set high, the device is in the test mode. When TMS3, TMS2, TMS1 and TMS0 are set to '0001', the device is in the bypass AGC mode. The bypass AGC mode is provided for the programmable equalizer/filter testing. When these bits are set to '0010', the device is in the bypass filter mode. The bypass filter mode is provided for the AGC testing. When these bits are set to '01xx', the DPD equalizer output can be observed at the ATOP/ATON pins. When these bits are set to '100x', one of the DPD phase detectors can be disabled. When these bits are set to '101x', the A+D or B+C signals for CE can be observed at ATOP/ATON pins.

3.6.2 Power Down Control

For power management, the PowerDown Control register (PDCR) can be used to set the operating mode of the device. The PDCR provides a control bit for each of the functional blocks. The contents of the PDCR determine which blocks will be active. Register mapping for the PDCR is shown in Table 3-2. Even though all blocks are disabled, register information is retained during the Sleep mode so it is not necessary to reprogram the serial port registers after returning to an active mode. The reference voltage (VC) is set to Hi-Z when the servo, mirror and RF blocks are disabled.

3.7 Serial Interface Operation

The serial interface is a CMOS bi-directional port for reading and writing programming data from/to the internal registers of the SP3721A. The serial port data transfer format is shown in Fig.3-2. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin. After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a read (1) or a write (0). The remaining 7 bits determine the internal register to be accessed. Table 3-3 provides register mapping information. The second byte contains the programming data. In Read mode(R/W=1) the SP3721A will output the register contents of the selected address. In Write mode, the device will load the selected register with data presented on the SDATA pin. At initial power-up, the contents of the internal registers will be set to '0' except the PDCR registers (PDCR will be set to '11011111' as a power down mode) and must be programmed prior to operation. During power down modes, the serial port remains active and the register programming data is retained. Detailed timing information is provided in Fig. 3.

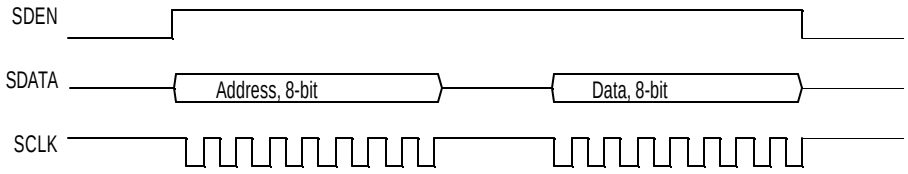

Figure 3-3. Serial Port Data Transfer Format

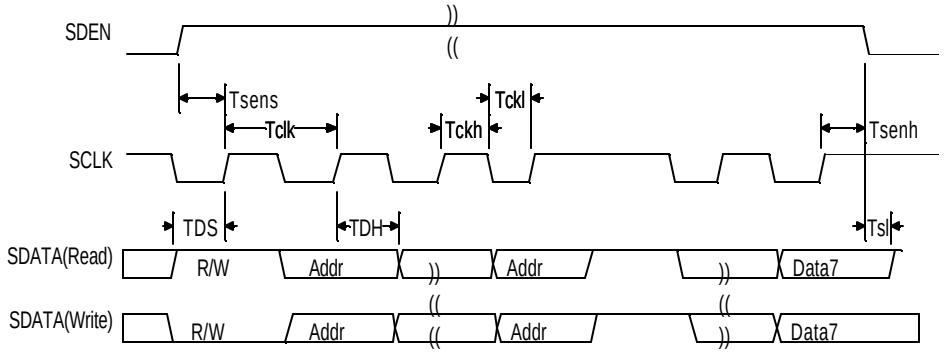

Figure 3-4. Serial Port Timing Information

Section 4 : Register Description

4.1 Configuration Registers

Eleven internal registers are used to configure the SP3721A. Each register definition is as follows:

Register Name : **PowerDown Control** (PDCR)
Address : 000 0010 =02h =02d

Bit	Description
7-5	**ID register** bits. Contains the device ID (000). Readback only
4	**Servo PowerDown**. When set to 1, powers down all circuitry in the servo section.
3	**Mode Selection**. Selects either DVD or CD mode. 0 : CD mode 1 : DVD mode
2	**Mirror Powerdown**. When set to 1, powers down all circuitry in the Mirror section.
1	**APC Powerdown**. When set to 1, powers down all circuitry in the APC section.
0	**RF Block Powerdown**. When set to 1, powers down all circuitry in the RF section including the AGC and filter.

Register Name : **Filter Cutoff** (FCCR)
Address : 0000 0011 =03h =03d

Bit	Description
7	**Fc Range**. Cutoff Frequency Range Select: 1= 2MHz ?fc ?10MHz 0= 8MHz ?fc ?24MHz
6-0	**FcDAC**. 7-bit DAC used to program the cutoff frequency of the filter.

Register Name : **Filter Boost** (FBCR)
Address : 0000 1011=0Bh =11d

Bit	Description
7	**SIGO Off**. SIGO Enable bit 0 = SIGO output pin enabled. 1 = SIGO output pin disabled (Hi-Z)
6-0	**FbDAC**. 7-bit DAC used to program the amount of boost added to the filter response at the –3dB point.

Register Name : **Servo Input Gain** (SIGR)
Address : 0000 1010 =0Ah =10d

Bit	Description
7-4	**ATT**. Attenuator Gain. Programs the gain of the RF attenuator. ATT Gain = (16-ATT)/16 [V/V] Where ATT is the decimal value of this 4bit word.
3	**Internal RF** selection 0 =RF signal externally supplied at the DVDRFP/DVDRFN pins. 1 =RF signal internally generated by summing up (A2,B2,C2,D2).
2-0	**ABCD**. Servo Input Gain Selection. Programs the gain of the input GCA for the A,B,C,D inputs (see table 4-6).

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Register Name : **RF Input Control** (RFCR)
Address : 0001 1010 =1Ah =26d

Bit	Description
7-6	**RF input Imp**. RF input impedance selection. Programs the input impedance at the RF inputs –DVDRFP/N and CDRF pins (see table 4-15)
5-4	**AGC Input Imp**. AGC Input impedance selection. Programs the input impedance at the input of the AGC-AIP/AIN pins (see table 4-16)
3	**AGC Fast Attack On**. AGC Fast Attack Current Enable. Enables the fast attack current in the AGC circuit when the signal at DIP/DIN is greater than 125% of the AGC level.
2-0	**A2B2C2D2**. Servo Input Gain Selection. Programs the gain of the input GCA for the A2,B2,C2 & D2 inputs (see table 4-6).

Register Name : **Focus/Tracking Gain** (FTGR)
Address : 0001 0010 =12h =18d

Bits	Description
7-4	**FSGAIN**. Focusing Gain Selection. Programs the gain of the focusing error signal (see table 4-8)
3-2	**MIRR GAIN**. Mirror Gain Selection. Programs the gain of the mirror circuit (see table 4-14)
1-0	**TRGAIN**. Tracking Gain Selection. Programs the gain of the tracking error signal (see table 4-7).

Register Name : **Tracking Offset** (TRCR)
Address : 0010 0010 =22h =34d

Bits	Description
7-4	**CE offset**. Center Error Offset Cancel. Programs the offset of the center error signal (see table 4-19)
3-0	**TR Offset**. Tracking Error Offset Cancel. Programs the offset of the tracking error signal (see table 4-18).

Register Name : **Mirror Control** (MRCR)
Address : 0010 1010 =2Ah =42d

Bits	Description
7	**MRCOMP HYS low**. MIRR Comparator Hysteresis Level Selection. 0 = 100mV 1 = 50mV
6-5	**MRCOMP.** MIRR Comparator Offset Level Selection. Programs the offset of the MIRR comparator. (see Table 4-10)
4	**MIRR Internal FDCHG ON**. Internal Fast Discharge. Used in conjunction with the FDCHG pin to initiate internal fast discharge in the mirror circuit.
3-2	**MLPF.** MIRR LPF Cutoff Selection. Programs the internal impedance of the Mirror circuit which, with the external capacitor connected between MLPF and VPB, sets the cutoff frequency of the low pass filter in the Mirror circuit. (see table 4-13).
1-0	**MIRR Input_Z Selection**. MIRR Input Impedance Selection. Selects the input impedance at the MIN pin. (see table 4-11)

Register Name : **Control A** (CAR)
Address : 0011 1010 =3Ah =58d

Bits	Description
7-4	**TMS bits**. Test mode selection. Programs the device to be in certain test modes. (See table 4-17).
3	**Focus one-beam sel**. Focus One Beam Select. Selects either single laser or twin laser pickup mode (see table 3-2). 0 : twin laser 1 : single laser
2	**MIR COMP low signal inhibit enable**. Mirror Comparator Low Signal Inhibit Enable. 0 : test mode 1 : Normal Mirror circuit function.
1-0	**MRENV Current**. MIRR Envelope Sink Current. Programs the sink current for the bottom envelope of the signal at MEI. (see table 4-12)

Register Name : **Control B (CBR)**
Address : 0011 0010=32h=50d

Bits	Description
7	**BCA Det**. BCA Code Detection Enable 0 : disable 1 : enable
6	**High Gain**. High Gain Mode Bit Select. 0 : Normal mode 1 : high gain mode
5	**DFT Mask TE On**. Defect Mask TE On. 0 : Normal Operation 1 :Fixes TE to VCI level when DFT is high.
4	**CE FDB**. Center Error Feedback Bit. When this bit is set to1, the center error value is fed back for the TE value.
3	**CE POL.** Center Error Polarity Bit. Programs the polarity of the CE component to be fed back into the TE signal.
2-0	**CE ATT**. Center Error Attenuator. Programs the attenuation of the center error signal to be fed back to the TE signal (see table 4-21)

Register Name : **Control C (CCR)**
Address : 010 0100 =24h =36d

Bits	Description
7	**DiSK Det**. Disk Discrimination Function 0 : disable 1 : enable
6	**DISK Det High Gain.** Disk Discrimination High Gain Bit. Selects the peak detector gain from MLPF, when the disk discrimination function is enabled. 0 = 8dB 1 = 18 dB
5	**APC Select**. Activates either the DVD or CD APC Circuitry. 0 = CD 1 = DVD
4-0	**FE Offset.** Focusing Error Offset Cancel. Programs the offset to be added to the focusing error signal. (see table 4-20)

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Register Name: **Control D (CDR)**
Address: 0001 1100 =1Ch =28d

Bits	Description
7-6	**DEFECT**. Defect Slice Level Offset Selection. Selects the slice level of the defect circuit as a percentage of the peak held value at PI. (see table9)
5	**CP/CN Low-Imp.** CP/CN Impedance Selection. 0 : 30 Kohm for CD mode, 20Kohm for DVD mode. 1 : 10 Kohm
4-3	**DPDLP**. DPD Equalizer LPF Filter cutoff selection. (See table 4-5)
2-0	**DPDEQ.** DPD Equalizer Unity Gain/Boost range selection (see Table 4-4)

Register Name: **Control E (CER)**
Address: 0010 1100 =2Ch =44d

Bits	Description
7	**RFAGC Hold**. RF AGC Hold Function. 0 : Normal Operation 1 : AGC is in a hold mode (Constant Gain)
6	Not Used.
5	**LDH/L.** APC Gain Selection. Programs the gain of the APC Circuit.
4-0	**Ploffset**. PI Offset Cancel Selection. Programs the offset to be added to the PI signal. (see table 4-20)

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Control Registers

Table 4-3. Serial Port Register Mapping

Register Name	Address (A6..A0,R/W)								D7	D6	D5	D4	D3	D2	D1	D0
PowerDown Control(PDCR)	0	0	0	0	0	1	0	0	ID 2 '0'	ID 1 '0'	ID 0 '0'	Servo 1=Disable 0=Enable	CD/DVD 1=DVD 0=CD	MIRR 1=Disable 0=Enable	Apc 1=Disable 0=Enable	RF 1=Disable 0=Enable
Filter Cutoff (FCCR)	0	0	0	0	0	1	1	0	FcRange 1=max 10M	FcDAC Bit6	FcDAC Bit5	FcDAC Bit 4	FcDAC Bit 3	FcDAC Bit 2	FcDAC Bit 1	FcDAC Bit 0
Filter Boost (FBCR)	0	0	0	1	0	1	1	0	SIGO Off	FaDAC Bit 6	FaDAC Bit 5	FaDAC Bit 4	FaDAC Bit 3	FaDAC Bit 2	FaDAC Bit 1	FaDAC Bit 0
Servo Input Gain (SIGR)	0	0	0	1	0	1	0	0	ATT Bit3	ATT Bit2	ATT Bit1	ATT Bit 0	Internal RF Sel	ABCD Bit 2	ABCD Bit 1	ABCD Bit 0
RF Input Control (RFCR)	0	0	1	1	0	1	0	0	RF Input IMP Bit1	RF Input IMP Bit0	AGC Input Bit1	AGC Input Bit 0	AGC Fast Attack On	A2B2C2D2 Bit 2	A2B2C2D2 Bit 1	A2B2C2D2 Bit 0
Focus/Tracking Gain (FTGR)	0	0	1	0	0	1	0	0	FSGAIN Bit 3	FSGAIN Bit 0	FSGAIN Bit1	FSGAIN Bit 0	MIRR Gain Bit 1	MIRRGAIN Bit 0	TRGAIN Bit 1	TRGAIN Bit 0
Tracking Offset (TRCR)	0	1	0	0	0	1	0	0	CE Offset Bit 3	CE Offset Bit 2	CE Offset Bit1	CE Offset Bit0	TROffset 2 Bit 3	Troffset2 Bit 2	Troffset2 Bit 1	Troffset2 Bit 0
Mirror Control (MRCR)	0	1	0	1	0	1	0	0	MRCOMP HYS-Low	MRCOMP Offset	MRCOMP Offset bit0	MIRR Internal FDCHG On	MLPF Bit 1	MLPF Bit 0	MIRR Input_Z sel Bit 1	MIRR Input_Z sel Bit 0
Control A (CAR)	0	1	1	1	0	1	0	0	TMS3	TMS2	TMS1	TMS0	Focus One-Beam sel	MIR COMP Low sig Inhibit En	MRENV CURNT Bit1	MRENV CURNTBit 0
Control B (CBR)	0	1	1	0	0	1	0	0	BCA DET	High Gain	DFT Mask TE On	CEFDB 1=on 0=off	CE POL 1=hlnv 0=lnv	CE ATT Bit 2	CE ATT Bit 1	CE ATT Bit 0
Control C (CCR)	0	0	1	1	1	0	0	0	Disk Det	Disk Det High Gain	APC Sel 1=DVD, 0=Cd	Feoffset Bit4	FE offset Bit 3	FE offset Bit 2	FE offset Bit 1	FE offset Bit 0
Control D (CDR)	0	1	0	0	1	0	0	0	Defect Bit 1	Defect Bit0	CP/CN Low-imp	DPDLP Bit1	DPDLP Bit 0	DPDEQ Bit 2	DPDEQ Bit 1	DPDEQ Bit 0
Control E (CER)	0	1	0	1	1	0	0	0	RFAGC Hold		LDH/L	Ploffset Bit 4	Ploffset Bit 3	Ploffset Bit 2	Ploffset Bit 1	Ploffset Bit 0

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Table 4-4. DPD Equalizer unity gain range Selection (CDR bits 2-0)

DPDEQ Bit 2	DPDEQ Bit1	DPDEQ Bit0	Unity Gain Range (typ)	
			Z1 (MHz)	P1 (MHz)
0	0	0	0.4	1
0	0	1	1.6	4
0	1	0	3.2	8
0	1	1	6.4	16
1	X	X	none	none

Table 4-5. DPD Equalizer LPF Cutoff Selection (CDR Bits 4-3)

DPDLPF Bit 1	DPDLPF Bit0	LPF Fc P2 (MHz)
0	0	10
0	1	20
1	0	30
1	1	40

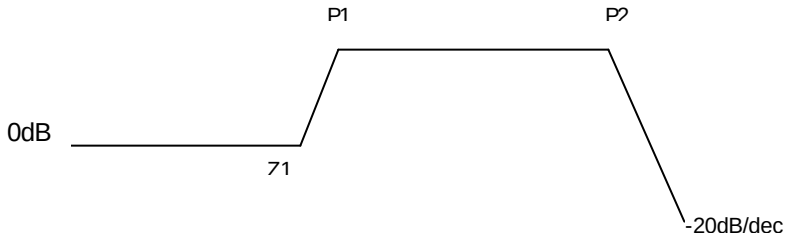

Fig. 4-4 : DPD Equalizer Characteristics

Table 4-6. Servo Input Gain Selection (SIGR bits 2-0, RFCR bits 2-0)

ABCD/ A2B2C2D2 bit 2	ABCD/ A2B2C2D2 bit 1	ABCD/ A2B2C2D2 bit 0	Input GCA Gain For A,B,C,D (V/V)	Input GCA Gain For A2,B2,C2,D2 (V/V)
0	0	0	1.2	3.6
0	0	1	1.4	4.2
0	1	0	1.7	5.1
0	1	1	2.1	6.3
1	0	0	2.5	7.5
1	0	1	3.0	9.0
1	1	0	3.6	10.8
1	1	1	4.3	12.9

Table 4-7. Tracking Gain Selection (FTGR bits 1-0)

TRGAIN bit 1	TRGAIN bit 0	Gain Control Amp Gain (V/V)
0	0	1.0
0	1	1.3
1	0	1.69
1	1	2.2

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Table 4-8. Focusing Gain Selection (FTGR bits 7-4)

FSGAIN bit 3	FSGAIN bit 2	FSGAIN bit 1	FSGAIN bit 0	Gain Control Amp Gain (V/V)
0	0	0	0	0.63 (-4dB)
0	0	0	1	0.69
0	0	1	0	0.76
0	0	1	1	0.82
0	1	0	0	0.88
0	1	0	1	0.95
0	1	1	0	1.00
0	1	1	1	1.07
1	0	0	0	1.14
1	0	0	1	1.20
1	0	1	0	1.26
1	0	1	1	1.33
1	1	0	0	1.39
1	1	0	1	1.45
1	1	1	0	1.52
1	1	1	1	1.58(4dB)

Table 4-9 : DFECT Slice Level Offset Selection (CDR bits 7-6)

Referenced to peak held PI value

Defect bit 1	Defect bit 0	Defect Detect level (%)
0	0	50
0	1	40
1	0	30
1	1	20

Table 4-10 : MIRR Comparator offset Selection (MRCR Bits 6-5)

MRCOMP bit1	MRCOMP bit0	Comparator Offset (mV)
0	0	0
0	1	50
1	0	100
1	1	150

Table 4-11 : MIN Input Impedance Selection (MRCR bits 1-0)

MIRR Input_Z bit 1	MIRR Input_Z bit 0	Input Impedance (kohm)
0	0	5
0	1	15
1	0	30
1	1	45

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Table 4-12 : MIRR Bottom Envelope Sink Current Selection (CAR bits 1-0)
A 1000 pF capacitor is connected to VPB from MEV pin

MRENV bit 1	MRENV bit 0	Bottom Envelope Current (uA)
0	0	20 (50us/V)
0	1	50 (20us/V)
1	0	100 (10us/V)
1	1	200 (5us/V)

Table 4-13 : MIRR LPF Fc Selection (MRCR bits 3-2)
A 160 pF capacitor is connected between VPB and the MLPF pin.

MLPF bit 1	MLPF bit 0	Output impedance for LPF (kohm)
0	0	2.5 (400 KHz)
0	1	5 (200 KHz)
1	0	10 (100 KHz)
1	1	20 (50 KHz)

Table 4-14 : MIRR Gain Selection (FTGR Bits 3-2)

MIRR Gain bit 1	MIRR GAIN bit 0	MIRR GAIN (db)
0	0	3
0	1	6
1	0	9
1	1	12

Table 4-15 : RF input impedance Selection (RFCR bits 7-6)

RF input bit 1	RF input bit 0	CDRF Input Impedance single-ended (kohm)	DVDRFP/N Input Impedance single-ended (kOhm)
0	0	10	10
0	1	20	20
1	0	30	30
1	1	40	40

Table 4-16 : AGC Input Impedance Selection (RFCR bits 5-4)

AGC Input Bit 1	AGC Input Bit 0	AGC Input Impedance single-ended (kohm)
0	0	7.5
0	1	12.5
1	0	17.5
1	1	20.0

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Table 4-17 : Test Modes Selection (CAR bits 7-4)

TMS3	TMS2	TMS1	TMS0	Test Modes
0	0	0	0	Test Mode disable
0	0	0	1	Bypass AGC
0	0	1	0	Bypass Filter
0	0	1	1	Not used
0	1	0	0	DPD EQ (A2) output from ATOP/ATON
0	1	0	1	DPD EQ (B2) output from ATOP/ATON
0	1	1	0	DPD EQ (C2) output from ATOP/ATON
0	1	1	1	DPD EQ (D2) output from ATOP/ATON
1	0	0	0	DPD Phase det. disable (A2/B2)
1	0	0	1	DPD Phase det. disable (C2/D2)
1	0	1	0	A+D output from ATOP/ATON
1	0	1	1	B+C output from ATOP/ATON
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	Mirror MLPF clamp ON

Table 4-18 : Tracking Error (TE) Offset Cancel (TRCR bits 3-0)

TROffset2 bit3	TROffset2 bit2	TROffset2 bit1	TROffset2 bit 0	Absolute Offset Value (mV)
0	0	0	0	0
0	0	0	1	-50
0	0	1	0	-100
0	0	1	1	-150
0	1	0	0	-200
0	1	0	1	-250
0	1	1	0	-300
0	1	1	1	-350
1	0	0	0	0
1	0	0	1	50
1	0	1	0	100
1	0	1	1	150
1	1	0	0	200
1	1	0	1	250
1	1	1	0	300
1	1	1	1	350

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Table 4-19 : Center Error (CE) Offset Cancel (TRCR bits 7-4)

CEOffset bit3	CEOffset bit2	CEOffset bit1	CEOffset bit0	Absolute Offset Value (mV)
0	0	0	0	0
0	0	0	1	-120
0	0	1	0	-240
0	0	1	1	-360
0	1	0	0	-480
0	1	0	1	-600
0	1	1	0	-720
0	1	1	1	-840
1	0	0	0	0
1	0	0	1	120
1	0	1	0	240
1	0	1	1	360
1	1	0	0	480
1	1	0	1	600
1	1	1	0	720
1	1	1	1	840

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Table 4-20: Focusing Error (FE) Offset Cancel (CCR bits 4-0), PI Offset Cancel (CER bits 4-0)

FE/PI Offset bit4	FE/PI Offset bit 3	FE/PI Offset bit 2	FE/PI Offset bit 1	FE/PI Offset bit 0	Absolute Offset Value (mV)
0	0	0	0	0	0
0	0	0	0	1	-46
0	0	0	1	0	-92
0	0	0	1	1	-138
0	0	1	0	0	-184
0	0	1	0	1	-230
0	0	1	1	0	-276
0	0	1	1	1	-322
0	1	0	0	0	-368
0	1	0	0	1	-414
0	1	0	1	0	-460
0	1	0	1	1	-506
0	1	1	0	0	-552
0	1	1	0	1	-598
0	1	1	1	0	-644
0	1	1	1	1	-690
1	0	0	0	0	0
1	0	0	0	1	46
1	0	0	1	0	92
1	0	0	1	1	138
1	0	1	0	0	184
1	0	1	0	1	230
1	0	1	1	0	276
1	0	1	1	1	322
1	1	0	0	0	368
1	1	0	0	1	414
1	1	0	1	0	460
1	1	0	1	1	506
1	1	1	0	0	552
1	1	1	0	1	598
1	1	1	1	0	644
1	1	1	1	1	690

Table 4-21 : Center Error (CE) Feedback Gain Selection (CBR bits 2-0)

CE-ATT Bit 2	CE-ATT Bit 2	CE-ATT Bit 2	CE Attenua-tion (dB)
0	0	0	-12
0	0	1	-14
0	1	0	-16
0	1	1	-18
1	0	0	-20
1	0	1	-22
1	1	0	-24
1	1	1	-26

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Section 5 : Electrical Characteristics

Electrical Specifications:

Unless otherwise specified, the recommended operating conditions are as follows: 4.5V<Positive Supply Voltage<5.5V, 0deg.C<T(ambient)<70deg.C. Currents flowing into the chip are positive. Current maximum are currents with the highest absolute value.

5.1 Absolute Maximum Ratings

Operation above maximum ratings may damage the device.

Parameter	Rating
Storage Temp.	-65 to 150deg.C
Junction Operating Temperature	+135deg.C
Positive Supply Voltage (Vp)	-0.5 to 7V
Voltage Applied to Logic Inputs	-0.5V toVp+0.5V
All other pins	-0.5V to Vp+0.5V

Power Supply Current and Power Dissipation

Parameter	Conditions	Min	Nom.	Max	Unit
ICC (VPA,B)	Outputs open		70		mA
Pwr	Outputs open		350		mW
Sleep mode Power	PDCR bit4,2,1,0=all'1'			5	mW

5.2 Digital Inputs and Outputs

TTL Compatible Inputs

Symbol	Parameter	Conditions	Min	Nom.	Max	Unit
VIL	Input low voltage		-0.3		0.8	V
VIH	Input high voltage		2.0		VPA+0.3	V
IIL	Input low current	VIL = 0.4V	-400		+100	uA
IIH	Input high current	VIH = 2.4V			50	uA

CMOS Compatible Inputs

Schmitt trigger type (not to be left open) Nominal 1.0V hysteresis around VPA/2.

Parameter	Conditions	Min	Nom.	Max	Unit
Input low voltage		-0.3		1.5	V
Input high voltage		3.5		VPA+0.3	V

CMOS Outputs

Parameter	Conditions	Min	Nom.	Max	Unit
Output low voltage	IOL =4mA			0.5	V
Output high voltage	IOH =-400uA	VPA-0.7			V
Rise time	10% to 90%, CL=15pF			8	ns
Fall time	90% to 10%, CL=15pF			8	ns

PSEUDO CMOS Outputs (MIRR, DFT, TZC)

Parameter	Conditions	Min	Nom	Max	Unit
Output low voltage	VOL IOL =4mA			0.5	V
Output high voltage	VOH IOH =400uA	VPBx-1.7			V

Serial Port

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
Tclk	SCLK period		100			ns
Tckl	SCLK low time		40			ns
Tckh	SCLK high time		40			ns
Tsens	Enable to SCLK		35			ns
Tsenh	SCLK to disable		100			ns
Tds	Data set-up time		15			ns
Tdh	Data hold time		15			ns
Tdskew	SCLK fall to valid data	CL?15pF	0		50	ns
Tsendl	SDATA tri-state delay				50	ns
Ttrn	SDATA turnaround time		70			ns
Tsl	SDEN low time		200			ns

5.3 RF Block Characteristics

Attenuator:
Input signals are AC coupled to DVDRFP/DVDRFN and CDRF. Unless otherwise specified, outputs are measured differently at ATOP/ATON, input frequency=16MHz@DVDRFP/DVDRFN and CDRF.

Parameter	Conditions	Min	Nom	Max	Unit
Input range DVDRFP/DVDRFN				1100	mVppd
Input range CDRF				1100	mVpp
Attenuator Gain Range	ATT gain=(16-ATT)/16	1/16		1	V/V
Attenuator Gain Accuracy	DVDRFP/DVDRFN=1Vppd, CDRF=1Vpp	-15		15	%
Differential Input impedance	DVDRFP/DVDRFN (see table 15)		2Rdvd		kohm
Single-ended input impedance	DVDRFP/DVDRFN (see table 15)		Rdvd		kohm
	CDRF (see table 15)		Rcd		kohm
Single-ended output impedance	ATOP/ATON to GND			120	ohm
Bandwidth	RF inputs to ATOP/ATON	40			MHz
RF summing amp input range	A2,B2,C2,D2 each			250	MV
RF summing amp gain			1		V/V
ATOP/ATON dynamic range	THD=1%	250			mVppd

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AGC Amplifier for RF signal

Input signals are AC coupled to AIP/AIN, and FNP/FNN are AC coupled to DIP/DIN. 0.1uF capacitor is connected from BYP to VPA (Cbyp). Unless otherwise specified, outputs are measured differentially at FNP/FNN, AIP/AIN=16MHz, and filter boost =0dB

Parameter	Conditions	Min	Nom	Max	Unit
Input range	Filter boost 0 to 12dB	20		200	mVppd
DIP-DIN voltage	AIP/AIN =0.1 Vppd	0.90	1.00	1.10	Vppd
DIP-DIN voltage variation	20mVppd<AIP/AIN<200mVppd			8.0	%
Gain range	Minimum gain			3	V/V
	Maximum gain	64			V/V
Gain sensitivity	BYP voltage change		38		dB/V
AGC dynamic range	THD=1%at FNP/FNN	1.2			Vppd
Differential input impedance ®	AIP/Ain (see table16)		2Ragc		kohm
Output offset variation	Gain=3to64			120	mV
Input noise voltage	Gain=24dB, FNP/FNN=0V			20	NV/√Hz
Bandwidth	Gain=24dB, CL?15pF	40			MHz
CMRR	Gain=24dB, @20MHz	40			dB
PSRR	Gain=24dB, @20MHz	40			dB
Gain decay time	AIP/AIN=200to 100mVppd FNP/FNN<0.9 Final Value, Cbyp=1000pF		36		us
Gain attack time Value	AIP/AIN=100to 200mVppd FNP/FNN<1.1 Final Value, Cbyp=1000pF		0.65		us

AGC Control

The input signals are AC coupled into DIP/DIN, Cbyp=0.1uF to VPA

Parameter	Conditions	Min	Nom	Max	Unit
DIP/DIN input range	Test only		1.0	1.5	Vppd
DIP/DIN input impedance		28	40	52	Kohm
Decay current	Normal decay Id		-4.0		uA
Attack current	Normal attack Ich		0.18		mA
	Fast attack mode Ichf (RFCR bit 3=0)		8x1ch		mA
BYP leakage current	HOLD1=high	-50		50	nA

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Programmable Filter Characteristics

Parameter	Conditions	Min	Nom	Max	Unit
Filter cutoff range	Fc@-3dB point Fc=(-0.00052x FCDACx FCDAC)+(0.28707xFCDAC) +0.535(MHz) Boost=0dB, FCCR D7=0 34?FCDAC?127	8		24	MHz
	Fc@-3dB point Fc=(-0.00016x FCDACx FCDAC)+(0.12020xFCDAC) +0.165(MHz) Boost=0dB, FCCR D7=1 12?FCDAC?127	2		10	MHz
Filter Cutoff Accuracy	6.7MHz@100MHz mode	-10		10	%
	8MHz?Fc?24MHz	-15		15	%
	4MHz?Fc?10MHz	-15		15	%
	2MHz?Fc?4MHz	-20		20	%
FNP,FNNdifferential gain(An)	@100kHz, boost=0dB	8	11	13	V/V
	@6dB setting	-1.0		+1.0	dB
	@9dB setting	-1.25		+1.25	dB
	@12dB setting	-1.5		+1.5	dB
Group delay @Fc FNP,FNN	Fc=2MHz		250		nS
	Fc=4MHz		110		nS
	Fc=8MHz		65		nS
	Fc=12MHz		40		nS
	Fc=24MHz		20		nS
Group delay variation FNP,FNN	Fc=2to4MHz F=0.2FctoFc,Boost=0&3dB		?5		%
	Fc=2to4MHz F=0.2FctoFc,Boost=0&3dB	-4		4	%
	Fc=2to4MHz F=0.2FctoFc,Boost=0&3dB		?7		%
	Fc=2to4MHz F=0.2FctoFc,Boost=0&3dB	-4		4	%
Filter output THD@1Vppd	FNP/FNN, F=0.67Fc,Fc=2to24MHz			2	%
	SIGO, F=0.67Fc,Fc=2to24MHz			2	%
Output noise voltage normal output	BW=100MHz,Rs=50? Fc=12MHz,boost=0dB		2.4		mVRms
	Fc=12MHz,boost=12dB		3.5		mVRms
Filter output sink current		1.5			mA
Filter output source current		4.0			mA
Filter output offset voltage	Fc=12MHz			200	mV
Filter output resistance	Single ended			200	ohm
SIGO sink current		1.8			mA
SIGO source current		3.0			mA
SIGO output swing	*reference		1.5	2.0	Vpp
Rx pin voltage	Ta=27deg.C		600		mV
	Ta=70deg.C		800		mV
Rx resistance	1%fixed value		8.2		kohm

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Servo Amplifier Outputs

Focusing, Tracking Error Detection Characteristics

The input signal is a sum of the photo detector outputs (ABCD). The feedback resistance of 100k? is connected from CDTE to F and another 100k? from E to VC. 100k? resistances are connected to the E & F inputs.

Parameter	Conditions	Min	Nom	Max	Unit
ABCD input Range	Referenced to VCI2			+250	mV
A+B+C+D input range	Referenced to VCI2 @GCA=1.2V/V	0		+1000	mV
PD1,PD2 Input range	Referenced to VCI2			+400	mV
PD1?PD2 input rangefor PI	Referenced to VCI2	0		+600	mV
PD1?PD2Input range for CDRFDC	Referenced to VCI2	0		+600	mV
EF Input range	Referenced to VCI2			?0.5	V
A,B,C,D Input impedance			10		kohm
PD1,PD2 Input impedance			20		kohm
Gain Control Amplifier	@CBR bit6=0 (1.2 to 4.3V/V) mode		11		dB
Dynamic Range	@CBR bit6=1 (4.8 to 17.2V/V) mode		11		dB
Resolution			3		bit
Bandwidth	For Focus&PI		500		KHz
Bandwidth	For CenterError	20			MHz
PD1PD2Input Amplifier bandwidth	@CDRFDC	40			MHz
CDRFDC Gain from PD1,PD2	@CBR bit6=0		1.0		V/V
	@CBR bit6=1(high gain)		2.5		V/V
CDRFDC Output swing	@PD1,PD2>VCI2			750	mVpp
Focus Error(FE) output swing				VC?1.0	Vpp
FE output offset from ABCD	CARbit3=1,GCA=1.2 to 4.3V/V Vcc=5V, focusGCA=4 to4dB CBRbit6=0			?200	mV
	CBRbit6=1(high gain mode)			?500	mV
FE output offset from PD1,PD2	CARbit3=0,Vcc=5V CBR bit6=0			?200	mV
	CBRbit6=1(High gain mode)			?500	mV
FE gain fromABCD((A+C)-(B+D))	Without imput GCA gain		1.4		V/V
FE gain fromPD1,PD2(PD2-PD1)	CBRbit6=0		3		V/V
	CBRbit6=1		12		V/V
FE output voltage		0.5			V
TE output voltage		0.5			V
FE,PI bandwidth			70		KHz
Tracking Error(TE)output swing				VCI?10	Vpp
TE gain from CDTE	@TE GCA=1.0V/V,CBRbit6=0		2		V/V
	CBR bit6=1		10		V/V
CP/CN differential impedance	CDR bit5=1		10		Kohm
	CDRbit5=0,PDCRbit3=0		30		Kohm
	CDRbit5=0,PDCRbit3=1		20		Kohm
TE output offset (TPPmode(F-E))	TE GCA=1.0to2.0V/V Vcc=5V, CBRbit6=0			?150	mV
	CBRbit6=1(High gain mode)			?350	mV
PI output offset from ABCD	CARbit3=1,Vcc=5V GCA=1.2to4.3V/V,CBRbit6=0			?200	mV
	CBRbit6=1(High gain mode)			?500	mV

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(continued)

PI output offset from PD1,PD2	CARbit3=0, Vcc=5V, CBRbit6=0			?200	mV
	CBRbit6=1 (high gain mode)			?500	mV
PI output gain from ABCD	CARbit3=1, does not include input GCA gain		1		V/V
PI output gain from PD1,PD2	CARbit3=0, CBRbit6=0		2		V/V
	CBR bit6=1		8		V/V
PI output range	@VCI=1.65V			VCI+1.6	V
Gain control Amplifier for FE	Dynamic Range		?4		dB
	Resolution		4		bit
Gain control Amplifier for TE	Dynamic range(1.0to2.2V/V)		6.8		dB
	Resolution		2		bit
FE,PI,TE,CE output sink current		350			uA
FE,PI,TE,CE output source current		4			mA

Differential Phase Tracking Error Detection

The input signals are AC coupled (2200pF) into A2,B2,C2,D2

Parameter	**Conditions**	**Min**	**Nom**	**Max**	**Unit**
Input impedance			10		k?
A2B2C2D2 Input Range				250	mVpp
Gain Control Amplifier	@CBR bit6=0 (3.6 to 12.9V/V) mode		11		dB
Dynamic Range	@CBR bit6=1 (14.4 to 51.6V/V) mode		11		dB
Resolution			3		bit
Equalizer Characteristics					
TE output offset in DPD mode	Input same phase signals (4MHz,100mVpp sine wave) @Vcc=5V, RFCR bits2-0=000, CDR bit4-0=00000, FTGRbit1-0=11 (TEGCA=6.8dB)			?350	mV
CE feedback attenuator Gain	See table 21		FBG		DB

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Mirror Detection
The SIGO signal is connected to MEI pin. The external capacitor (250pF) is connected to VPB. The MEVO signal is AC coupled (0.1uF) into MIN from SIGO.

Parameter	Conditions	Min	Nom	Max	Unit
MIN input impedance	See table 11		Rmirr		Kohm
	@CCR bit7=1		300		Kohm
MEI input swing	From SIGO		1.5	2.0	Vpp
MEI input impedance	PNP transistor base				
MLPF output swing	CCR bit7=0	300		1000	mVpp
MLPF output impedance	See table 13		Rmlpf		Kohm
	@CCRbit7=1		100		Kohm
MLPF output gain (from MIN)	See table 14		Gmlpf		dB
Peak detector gain (from MLPF)	@CCR bit7=0		0		dB
	@CCRbit7,6=11		8		dB
	@CCRbit7,6=10		18		dB
BOTTOM envelope sink current	See table 12		BME		uA
BOTTOM hold sink current	@CCRbit7=0		14.5		uA
	@CCRbit7=1		3.5		uA
Top hold sink current	@CCRbit7=0		14.5		uA
	@CCRbit7=1		3.5		uA
Bottom hold fast discharge current	FDCHG=low, for bottom hold		5		mA
MIRR comparator offset	See table 10		MOF		mV
MIRR comparator hysteresis	MRCR bit 7=1		?50		mV
	MRCR bit 7=0		?100		mV
MIRR comparator disable level	@CAR bit 2=0		70		mV
MIRR output duty cycle	MLPF>400mVpp. MRCRbit6,5=00	45		55	%

Defect Detection
The PI peak hold capacitance is connected from TPH to VNB

Parameter	Conditions	Min	Nom	Max	Unit
TPH sink current	@CBR bit7=0		5		uA
	@CBR bit7=1		50		uA
DFT comparator hysteresis	Low to high only		+100		mV
DFT slice level	Refer to TPH see table 9		DS		%

Center Error Detection

The feedback resistance of 100kohms is connected from CDTE to F and another 100kohms from E to VCI2. 39kohms resistances are connected to the E & F inputs.

Parameter	Conditions	Min	Nom	Max	Unit
CDTE Gain			2.5		V/V
CDTE output range				VC?0.5	V
CE output swing				VC?1.0	V
DVD CE top hold time constant			10000		dV/dT
CE output Gain	@DVD mode(CER bit 3=1) after top hold		2		V/V
CE output offset	CAR bit3=1,Vcc=5V,CBR bit6=0 GCA=1.2to 4.3V/V			?200	mV
(DVD mode)	CBR bit6=1(High gain mode)			?600	mV

Auto Laser Power Control

Parameter	Conditions	Min	Nom	Max	Unit
Gain high power mode (DVD)	@250mV PD input,CDR bit5=1		21.4		V/V
Low power mode (CD/DVD)	@150mV PD input, CDR bit5=0		36.4		V/V
LD source current			100		uA
LD output voltage	@Vcc=5V @Highpowermode,PD=250mV	2.4		3.6	V
	@low powermode,PD=150mV	2.2		3.8	V

VC Reference Circuit

Parameter	Conditions	Min	Nom	Max	Unit
VC output impedance				50	Ohm
VC output voltage	No-load		2.5		V
VC output voltage	5mA load	2.25			V
VCI input range		1.6		2.75	V
VCI2 input range		2.25		2.75	V

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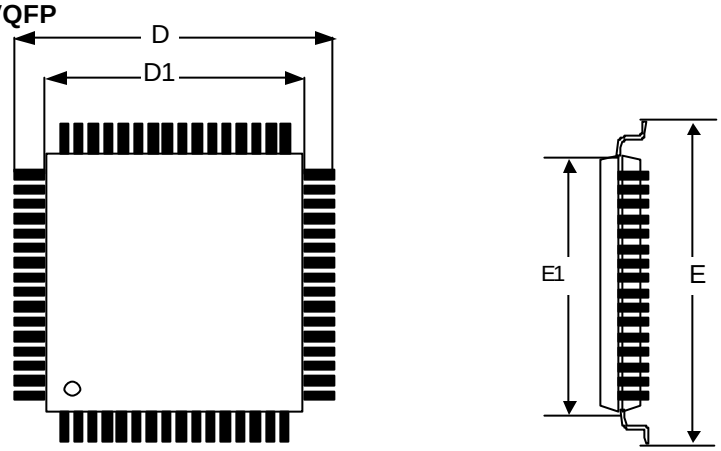
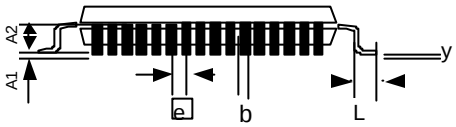
Section 6 : Packaging Information

64-pin VQFP





Symbol	Dimension (millimeters)		
	Min.	Nom.	Max.
A		1.50	
A_1		0.10	
A_2	1.30	1.40	1.50
b	0.10	0.20	0.30
D	11.70	12.00	12.30
D_1	10.20	10.00	9.80
E	11.70	12.00	12.30
E_1	10.20	10.00	9.80
e		0.50	
L	-	0.50	-
y	-	-	0.10

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Section 7 : Revision History

May 2000 v.0.90 - Date started

June 16, 2000 v.1.00

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