## Features

1. The protection IC and The Dual-Nch MOSFET to use common Drain are integrated into One-packaging IC.
2. Reduced Pin-Count by fully connecting internally.
3. Application Part

1) Protection IC

① Uses high withstand voltage CMOS process.
- The charger section can be connected up to absolute maximum rating 28V.

② Detection voltage precision
- Overcharge detection voltage

±35㎷ (Ta=25℃), ±50㎷ (Ta=-30~76℃)

- Overdischarge detection voltage

±58㎷ (Ta=25℃), +63, -76㎷ (Ta=-30~76℃)

- Discharge overcurrent detection voltage

±10㎷ (Ta=25℃), ±15㎷ (Ta=-30~76℃)

- Charging overcurrent detection voltage

±15㎷ (Ta=25℃), ±25㎷ (Ta=-30~76℃)

③ Built-in detection delay times (timer circuit)
- Overcharge detection delay time

5.0±1.5s (Ta=25℃), 5.0[+3.45, −2.0]s (Ta=-30~76℃)

- Overdischarge detection delay time

20.0±6.0㎳ (Ta=25℃), 20.0[+13.6, −8.0]㎳ (Ta=-30~76℃)

- Discharge overcurrent detection delay time

12.0±4.0㎳ (Ta=25℃), 12.0[+8.7, −4.8]㎳ (Ta=-30~76℃)

- Charging overcurrent detection delay time

16.0±5.0㎳ (Ta=25℃), 16.0[+17.1, −6.4]㎳ (Ta=-30~76℃)

- Short detection delay time

400[+160, −170]㎲ (Ta=25℃), 400[+400, −200]㎲ (Ta=-30~76℃)

④ 0V charge function is allowed

⑤ Auto Wake-up function is not allowed

2) FET

① Using advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltage as low as 2.5V while retaining a 12V $V_{GS(MAX)}$.

② ESD protected

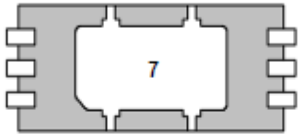
③ Common drain configuration

④ General characteristics
- $V_{DS}$ (V) = 24V
- $I_D$ (A) = 8A
- $R_{SS(ON)}$ < 25mΩ ($V_{GS}$ = 3.9V, $I_D$ = 1A)
- ESD Rating : 2000V HBM

## Pin Assignment

[ Package: TEP-6L ]


< TOP VIEW >




< BOTTOM VIEW >

| | |
|---|---|
| 1 | Source 1 (Same as Vss) |
| 2 | Source 1 (Same as Vss) |
| 3 | $V_{DD}$ |
| 4 | V-(VM) |
| 5 | Source 2 |
| 6 | Source 2 |
| 7 | Drain |

## Block Diagram