

### Features

- Complete 1-3 GHz Single Chip System for Digital Terrestrial Television Applications
- Selectable Reference Division Ratio, Compatible with DTT Requirements
- Optimised for Low Phase Noise, with Comparison Frequencies up to 4 MHz
- No RF Prescaler
- Selectable Reference/Comparison Frequency Output
- Four Selectable I<sup>2</sup>C Addresses
- I<sup>2</sup>C Fast Mode Compliant with 3.3V and 5V Logic Levels
- Four Switching Ports
- Functional Replacement for SP5659 (except ADC)
- Pin Compatible with SP5655
- Power Consumption 120mW with V<sub>CC</sub> = 5-5V, all Ports off
- ESD Protection 2kV min., MIL-STD-883B Method 3015 Cat.1 (Normal ESD handling procedures should be observed)

### Applications

- Digital Satellite, Cable and Terrestrial Tuning Systems
- Communications Systems

### Description

The SP5730 is a single chip frequency synthesiser designed for tuning systems up to 1-3GHz and is optimised for digital terrestrial applications. The RF preamplifier interfaces direct with the RF programmable divider, which is of MN1A construction so giving a step size equal to the loop comparison frequency and no

### Ordering Information

|                 |              |             |
|-----------------|--------------|-------------|
| SP5730A/KG/QP1T | 16 Pin QSOP  | Tape & Reel |
| SP5730A/KG/QP1S | 16 Pin QSOP  | Tubes       |
| SP5730A/KG/MP1S | 16 Pin SOIC  | Tubes       |
| SP5730A/KG/MP2S | 16 Pin SOIC* | Tubes       |
| SP5730A/KG/QP2T | 16 Pin QSOP* | Tape & Reel |
| SP5730A/KG/MP1T | 16 Pin SOIC  | Tape & Reel |
| SP5730A/KG/MP2T | 16 Pin SOIC* | Tape & Reel |
| SP5730A/KG/QP2S | 16 Pin QSOP* | Tubes       |

\*Pb Free Matte Tin

prescaler phase noise degradation over the full RF operating range. The comparison frequency is obtained either from an on-chip crystal controlled oscillator, or from an external source. The oscillator frequency,  $f_{REF}$ , or phase comparator frequency,  $f_{COMP}$ , can be switched to the REF/COMP output providing a reference for a second frequency synthesiser. The synthesiser is controlled via an I<sup>2</sup>C bus and is fast mode compliant. It can be hard wired to respond to one of four addresses to enable two or more synthesisers to be used on a common bus. The device contains four switching ports P0 - P3.

### Absolute Maximum Ratings

All voltages are referred to V<sub>EE</sub> = 0V

|                                 |                               |
|---------------------------------|-------------------------------|
| Supply voltage, V <sub>CC</sub> | -0.3V to +7V                  |
| RF differential input voltage   | 2.5Vp-p                       |
| All I/O port DC offsets         | -0.3 to V <sub>CC</sub> +0.3V |
| SDA and SCL DC offset           | -0.3 to 6V                    |
| Storage temperature             | -55°C to +150°C               |
| Junction temperature            | +150°C                        |
| QP16 thermal resistance         |                               |
| Chip to ambient, $\theta_{JA}$  | 80°C/W                        |
| Chip to case, $\theta_{JC}$     | 20°C/W                        |

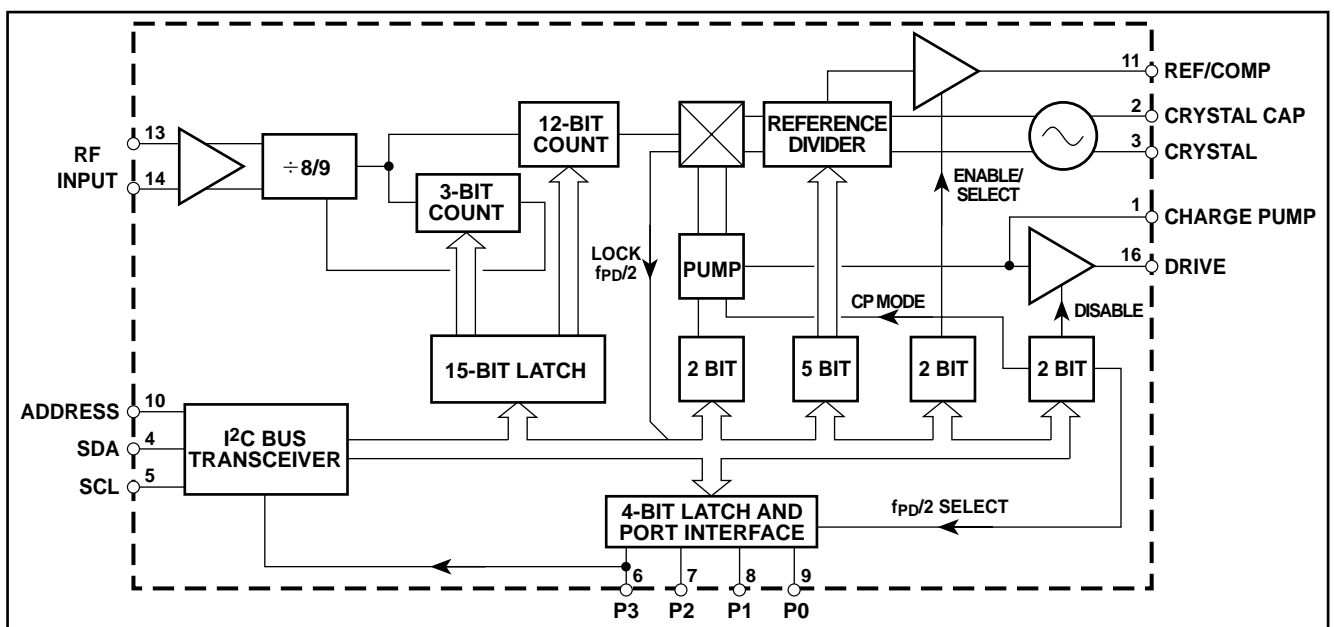


Figure 1 - SP5730 block diagram

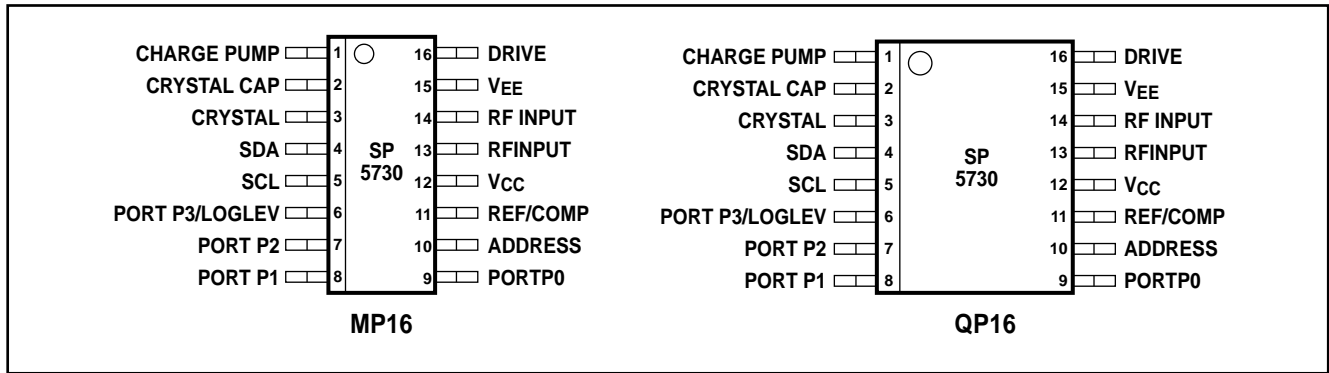


Figure 2 - Pin connections - top view

**Table 1 - Electrical Characteristics**

Test Conditions:  $T_{AMB} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 4.5\text{V}$  to  $5.5\text{V}$ . These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

| Characteristic                           | Pin   | Value |      |       | Units  | Conditions  |
|--|-------|-------|------|-------|--------|---|
|  |       | Min.  | Typ. | Max.  |        |   |
| Supply current                           | 12    |       | 16   | 22    | mA     |   |
| <b>RF input</b>                          | 13,14 |       |      |       |        |   |
| Input voltage                            |       | 12.5  |      | 300   | mVrms  | 100MHz to 1.3GHz, see Figure 3  |
| Input impedance                          |       | 40    |      | 300   | mVrms  | 50MHz to 100MHz, see Figure 3<br>See Figure 4   |
| <b>SDA, SCL</b>                          | 4,5   |       |      |       |        |   |
| Input high voltage                       |       | 3     |      | 5.5   | V      | 5V I <sup>2</sup> C logic selected  |
| Input low voltage                        |       | 2.3   |      | 3.5   | V      | 3.3V I <sup>2</sup> C logic selected  |
| Input high current                       |       | 0     |      | 1.5   | V      | 5V I <sup>2</sup> C logic selected  |
| Input low current                        |       | 0     |      | 1     | V      | 3.3V I <sup>2</sup> C logic selected  |
| Leakage current                          |       |       |      | 10    | μA     | Input voltage = $V_{CC}$  |
| Input hysteresis                         |       |       |      | -10   | μA     | Input voltage = $V_{EE}$  |
| SDA output voltage                       | 4     | 0.4   |      | 10    | μA     | $V_{CC} = V_{EE}$   |
| SCL clock rate                           | 5     |       |      | 0.4   | V      | $I_{SINK} = 3\text{mA}$   |
| <b>Charge pump</b>                       |       |       |      |       |        |   |
| Output current                           | 1     |       |      | 0.6   | V      | $I_{SINK} = 6\text{mA}$   |
| Output leakage                           | 1     |       |      |       |        |   |
| Drive output current                     | 16    | 0.5   | ±3   | ±10   | nA     | See Table 7, $V_{PIN1} = 2\text{V}$<br>$V_{PIN1} = 2\text{V}$ , $V_{CC} = 15.0\text{V}$ , $T_{AMB} = 25^{\circ}\text{C}$<br>$V_{PIN16} = 0.7\text{V}$ |
| <b>Crystal</b>                           | 2,3   |       |      |       |        |   |
| Frequency                                |       | 2     |      | 20    | MHz    | See Figure 5 for application  |
| <b>External reference</b>                | 3     |       |      |       |        |   |
| Input frequency                          |       | 2     |      | 20    | MHz    | Sinewave coupled via 10nF blocking capacitor  |
| Drive level                              |       | 0.2   |      | 0.5   | Vp-p   | Sinewave coupled via 10nF blocking capacitor  |
| <b>Buffered REF/COMP</b>                 | 11    |       |      |       |        |   |
| Output amplitude                         |       |       | 0.35 |       | Vp-p   | AC coupled, see Note 2  |
| Output impedance                         |       |       | 250  |       | Ω      | 0.5 to 20MHz<br>Enabled by bit RE = 1   |
| <b>Phase Detector</b>                    |       |       |      |       |        |   |
| Comparison frequency                     |       |       | 4    |       | MHz    |   |
| Equivalent phase noise at phase detector |       |       | -152 |       | dBc/Hz | $f_{COMP} = 2\text{MHz}$ , SSB, See Note 4  |
|  |       |       | -158 |       | dBc/Hz | $f_{COMP} = 125\text{kHz}$ , SSB, See Note 4  |
| <b>RF division ratio</b>                 |       | 56    |      | 32767 |        |   |
| <b>Reference division ratio</b>          |       |       |      |       |        | See Table 2   |

cont...

**Table 1 - Electrical Characteristics (continued)**

| Characteristic  | Pin | Value         |      |                       | Units        | Conditions  |
|---|-----|---------------|------|-----------------------|--------------|---|
|   |     | Min.          | Typ. | Max.                  |              |   |
| <b>Output Ports P3 - P0</b><br>Sink current<br>Leakage current                    | 6-9 | 2             |      | 10                    | mA<br>μA     | $V_{PORT} = 0.7V$<br>$V_{PORT} = V_{CC}$ See Note 1   |
| <b>Address select</b><br>Input high current<br>Input low current                  | 10  |               |      | 1<br>-0.5             | mA<br>μA     | See Table 5<br>$V_{IN} = V_{CC}$<br>$V_{IN} = V_{EE}$   |
| <b>Logic level select</b><br>Input high level<br>Input low level<br>Input current | 6   | 3<br>0<br>-10 |      | $V_{CC}$<br>1.5<br>10 | V<br>V<br>μA | See Note 3<br>5V I <sup>2</sup> C logic level selected<br>3.3V I <sup>2</sup> C logic level selected<br>$V_{IN} = V_{EE}$ to $V_{CC}$ |

**NOTES**

1. Output ports high impedance on power-up, with SDA and SCL at logic '0'.
2. If the REF/COMP output is not used, the output should be left open circuit or connected to  $V_{CC}$  and disabled by setting RE = '0'.
3. Bi-directional port. When used as an output, the input logic state is ignored. When used as an input, the port should be switched into high impedance (off) state.
4. Figures measured at 2kHz deviation, SSB (within loop bandwidth).

**Functional Description**

The SP5730 contains all the elements necessary, with the exception of a frequency reference, loop filter and external high voltage transistor, to control a varactor tuned local oscillator, so forming a complete PLL frequency synthesised source. The device allows for operation with a high comparison frequency and is fabricated in high speed logic, which enables the generation of a loop with good phase noise performance. It can also be operated with comparison frequencies appropriate for frequency offsets as required in digital terrestrial television (DTT) receivers.

The RF input signal is fed to an internal preamplifier, which provides gain and reverse isolation from the divider signals. The output of the preamplifier interfaces with the 15-bit fully programmable divider which is of MN1A architecture, where the dual modulus prescaler is 48/9, the A counter is 3 bits, and the M counter is 12 bits.

The output of the programmable divider is applied to the phase comparator where it is compared in both phase and frequency domains with the comparison frequency. This frequency is derived either from the on-chip crystal controlled oscillator or from an external reference source. In both cases the reference frequency is divided down to the comparison frequency by the reference divider which is programmable into 1 of 29 ratios as detailed in Table 2.

The output of the phase detector feeds a charge pump and loop amplifier section, which when used with an external high voltage transistor and loop filter, integrates the current pulses into the varactor line voltage. The programmable divider output  $f_{PD}/2$  can be switched to port P0 by programming the device into test mode. The test modes are described in Table 6.

**Programming**

The SP5730 is controlled by an I<sup>2</sup>C data bus and is compatible with both standard and fast mode formats and with I<sup>2</sup>C data generated from nominal 3.3V and 5V sources. The I<sup>2</sup>C logic level is selected by the bi-directional port P3/ LOGLEV. 5V logic levels are selected by connecting P3/ LOGLEV to  $V_{CC}$  or leaving it open circuit; 3.3V logic levels are set by connecting P3/LOGLEV to ground. If this port is used as an input the P3 data should be programmed to high impedance. If used as an output only 5V logic levels can be used, in which case the logic state imposed by the port on the input is ignored.

Data and clock are fed in on the SDA and SCL lines respectively as defined by I<sup>2</sup>C bus format. The synthesiser can either accept data (write mode), or send data (read mode). The LSB of the address byte (R/W) sets the device into write mode if it is low, and read mode if it is high. Tables 3 and 4 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I<sup>2</sup>C bus system. Table 5 shows how the address is selected by applying a voltage to the address input.

When the device receives a valid address byte, it pulls the SDA line low during the acknowledge period, and during following acknowledge periods after further data bytes are received.

When the device is programmed into read mode, the controller accepting the data must be pulled low during all status byte acknowledge periods to read another status byte. If the controller fails to pull the SDA line low during this period, the device generates an internal STOP condition, which inhibits further reading.

Table 2 - Reference division ratios

| R4 | R3 | R2 | R1 | R0 | Division ratio |
|----|----|----|----|----|----------------|
| 0  | 0  | 0  | 0  | 0  | 2              |
| 0  | 0  | 0  | 0  | 1  | 4              |
| 0  | 0  | 0  | 1  | 0  | 8              |
| 0  | 0  | 0  | 1  | 1  | 16             |
| 0  | 0  | 1  | 0  | 0  | 32             |
| 0  | 0  | 1  | 0  | 1  | 64             |
| 0  | 0  | 1  | 1  | 0  | 128            |
| 0  | 0  | 1  | 1  | 1  | 256            |
| 0  | 1  | 0  | 0  | 0  | Illegal state  |
| 0  | 1  | 0  | 0  | 1  | 5              |
| 0  | 1  | 0  | 1  | 0  | 10             |
| 0  | 1  | 0  | 1  | 1  | 20             |
| 0  | 1  | 1  | 0  | 0  | 40             |
| 0  | 1  | 1  | 0  | 1  | 80             |
| 0  | 1  | 1  | 1  | 0  | 160            |
| 0  | 1  | 1  | 1  | 1  | 320            |
| 1  | 0  | 0  | 0  | 0  | Illegal state  |
| 1  | 0  | 0  | 0  | 1  | 6              |
| 1  | 0  | 0  | 1  | 0  | 12             |
| 1  | 0  | 0  | 1  | 1  | 24             |
| 1  | 0  | 1  | 0  | 0  | 48             |
| 1  | 0  | 1  | 0  | 1  | 96             |
| 1  | 0  | 1  | 1  | 0  | 192            |
| 1  | 0  | 1  | 1  | 1  | 384            |
| 1  | 1  | 0  | 0  | 0  | Illegal state  |
| 1  | 1  | 0  | 0  | 1  | 7              |
| 1  | 1  | 0  | 1  | 0  | 14             |
| 1  | 1  | 0  | 1  | 1  | 28             |
| 1  | 1  | 1  | 0  | 0  | 56             |
| 1  | 1  | 1  | 0  | 1  | 112            |
| 1  | 1  | 1  | 1  | 0  | 224            |
| 1  | 1  | 1  | 1  | 1  | 448            |

**Write mode**

With reference to Table 3, bytes 2 and 3 contain frequency information bits 2<sup>14</sup>-2<sup>0</sup> inclusive. Bytes 4 and 5 control the reference divider ratio (see Table 2), charge pump setting (see Table 7), REF/COMP output (see Table 8), output ports and test modes (see Table 6).

After reception and acknowledgement of a correct address (byte 1), the first bit of the following byte determines whether the byte is interpreted as a byte 2 or

4, a logic '0' indicating byte 2, and a logic '1' indicating byte 4. Having interpreted this byte as either byte 2 or 4, the following data byte will be interpreted as byte 3 or 5 respectively. Having received two complete data bytes, additional data bytes can be entered, where byte interpretation follows the same procedure, without re-addressing the device. This procedure continues until a STOP condition is received. The STOP condition can be generated after any data byte; if, however, it occurs during a byte transmission, the previous byte data is retained. To facilitate smooth fine tuning, the frequency data bytes are only accepted by the device after all 15 bits of frequency data have been received, or after the generation of a STOP condition.

**Read mode**

When the device is in read mode, the status byte read from the device takes the form shown in Table 4.

Bit 1 (POR) is the power-on reset indicator, and this is set to a logic '1' if the V<sub>CC</sub> supply to the device has dropped below 3V (at 25°C), e.g. when the device is initially turned on. The POR is reset to '0' when the read sequence is terminated by a STOP command. When POR is set high this indicates the programmed information may be corrupted and the device reset to power up condition.

Bit 2 (FL) indicates whether the device is phase locked, a logic '1' is present if the device is locked, and a logic '0' if it is not.

**Programmable features**

- **RF programmable divider** Function as described above.
- **Reference programmable divider** Function as described above.
- **Charge pump current** The charge pump current can be programmed by bits C1 and C0 within data byte 5, as defined in Table 7.
- **Test mode** The test modes are invoked by setting bits RE, RS, T1 and T0 as described in Table 6.
- **Reference/Comparison frequency output** The reference frequency f<sub>REF</sub> or comparison frequency f<sub>COMP</sub> can be switched to the REF/COMP output, function as defined in Table 8. RE and RS default to logic '1' during device power up, thus enabling the comparison frequency f<sub>COMP</sub> at the REF/COMP output.

**Table 3 - Write data format (MSB transmitted first)**

|                      | MSB            |                 |                 |                 |                 | LSB             |                |                |   |        |
|----------------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|---|--------|
| Address              | 1              | 1               | 0               | 0               | 0               | MA1             | MA0            | 0              | A | Byte 1 |
| Programmable divider | 0              | 2 <sup>14</sup> | 2 <sup>13</sup> | 2 <sup>12</sup> | 2 <sup>11</sup> | 2 <sup>10</sup> | 2 <sup>9</sup> | 2 <sup>8</sup> | A | Byte 2 |
| Programmable divider | 2 <sup>7</sup> | 2 <sup>6</sup>  | 2 <sup>5</sup>  | 2 <sup>4</sup>  | 2 <sup>3</sup>  | 2 <sup>2</sup>  | 2 <sup>1</sup> | 2 <sup>0</sup> | A | Byte 3 |
| Control data         | 1              | T1              | T0              | R4              | R3              | R2              | R1             | R0             | A | Byte 4 |
| Control data         | C1             | C0              | RE              | RS              | P3              | P2              | P1             | P0             | A | Byte 5 |

**Key to Table 3.**

- A** Acknowledge bit
- MA1, MA0** Variable address bits (see Table 5)
- 2<sup>14-20</sup>** Programmable division ratio control bits
- R4-R0** Reference division ratio select (see Table 2)
- C1, C0** Charge pump current select (see Table 7)
- RE** Reference oscillator output enable
- RS** REF/COMP output select when RE=1 (see Table 8)
- T1-T0** Test mode control bits (see Table 6)
- P3-P0** P3, P2, P1 and P0 port output states

**Table 4 - Read data format (MSB transmitted first)**

|             | MSB |    |   |   |   | LSB |     |   |   |        |
|-------------|-----|----|---|---|---|-----|-----|---|---|--------|
| Address     | 1   | 1  | 0 | 0 | 0 | MA1 | MA0 | 1 | A | Byte 1 |
| Status byte | POR | FL | 0 | 0 | 0 | 0   | 0   | 0 | A | Byte 2 |

**Key to table 4,**

- A** Acknowledge bit
- MA1, MA0** Variable address bits (see Table 5)
- POR** Power On Reset indicator
- FL** Phase lock flag

**Table 5 - Address selection**

| MA1 | MA0 | Address input voltage level                |
|-----|-----|--|
| 0   | 0   | 0 to 0.1V <sub>CC</sub>                    |
| 0   | 1   | Open circuit                               |
| 1   | 0   | 0.4V <sub>CC</sub> to 0.6V <sub>CC</sub> * |
| 1   | 1   | 0.9V <sub>CC</sub> to V <sub>CC</sub>      |

\* Programmed by connecting a 15kΩ resistor from pin 10 to V<sub>CC</sub>

**Table 6 - Test modes**

| RE•RS | T1 | T0 | Test mode description                     |
|-------|----|----|---|
| 0     | 0  | 0  | Normal operation                          |
| 1     | 0  | 0  | Normal operation, P0 = f <sub>PD</sub> /2 |
| X     | 0  | 1  | Charge pump sink*, FL = '0'               |
| X     | 1  | 0  | Charge pump source*, FL = '0'             |
| X     | 1  | 1  | Charge pump disabled*, FL = '1'           |

\* Clocks need to be present on crystal and RF inputs to enable charge pump test modes and to toggle Status byte bit FL.  
X = don't care

**Table 7 - Charge pump current**

| C1 | C0 | Current (µA) |       |       |
|----|----|--------------|-------|-------|
|    |    | Min.         | Typ.  | Max.  |
| 0  | 0  | ±116         | ±155  | ±194  |
| 0  | 1  | ±247         | ±330  | ±412  |
| 1  | 0  | ±517         | ±690  | ±862  |
| 1  | 1  | ±1087        | ±1450 | ±1812 |

**Table 8 - REF/COMP output**

| RE | RS | REF/COMP output            |
|----|----|----------------------------|
| 0  | X  | High impedance             |
| 1  | 0  | f <sub>REF</sub> selected  |
| 1  | 1  | f <sub>COMP</sub> selected |

X = don't care

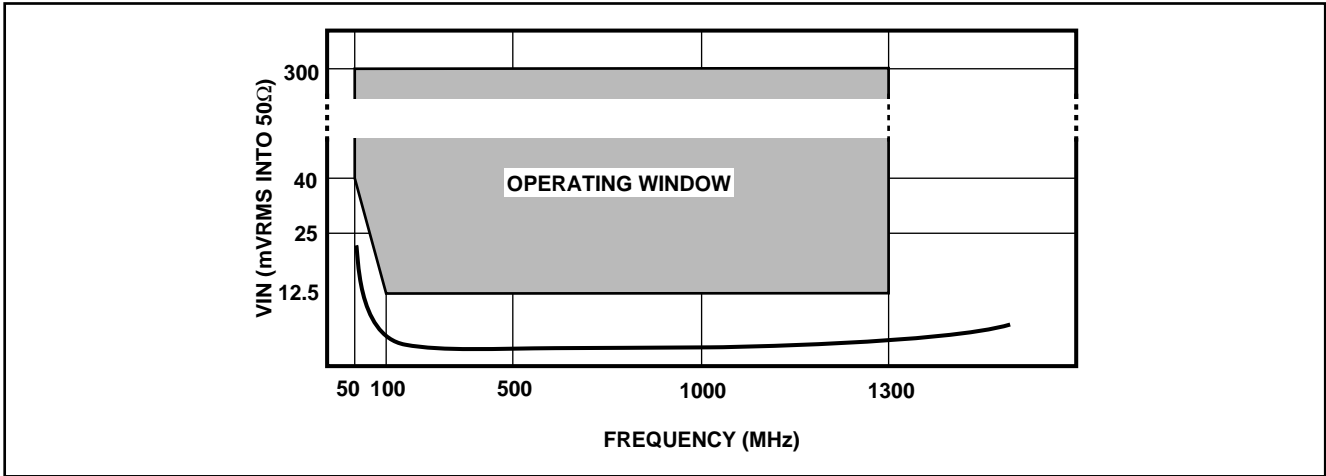


Figure 3 - Typical RF input sensitivity

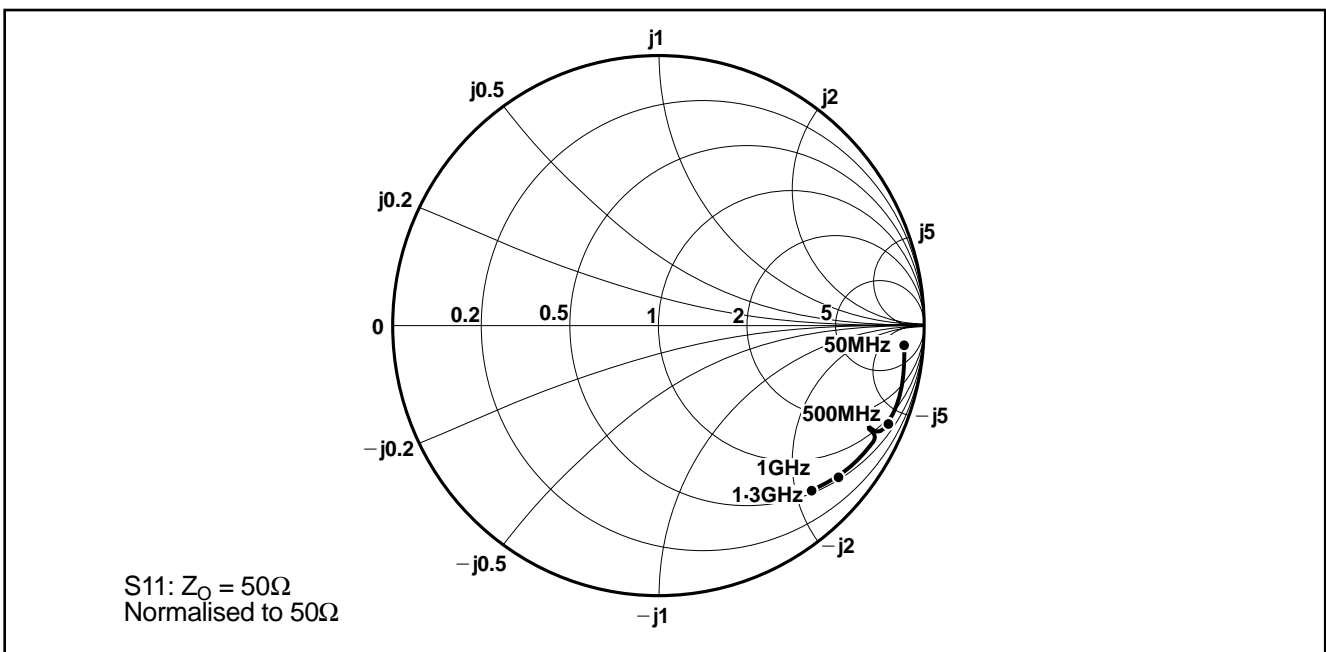


Figure 4 - RF input impedance

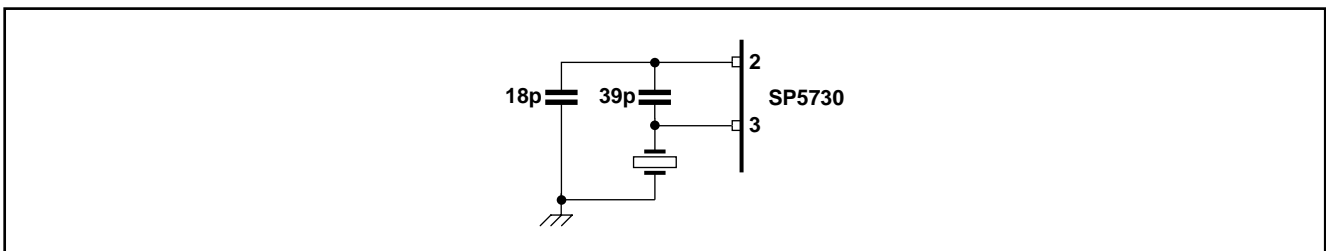
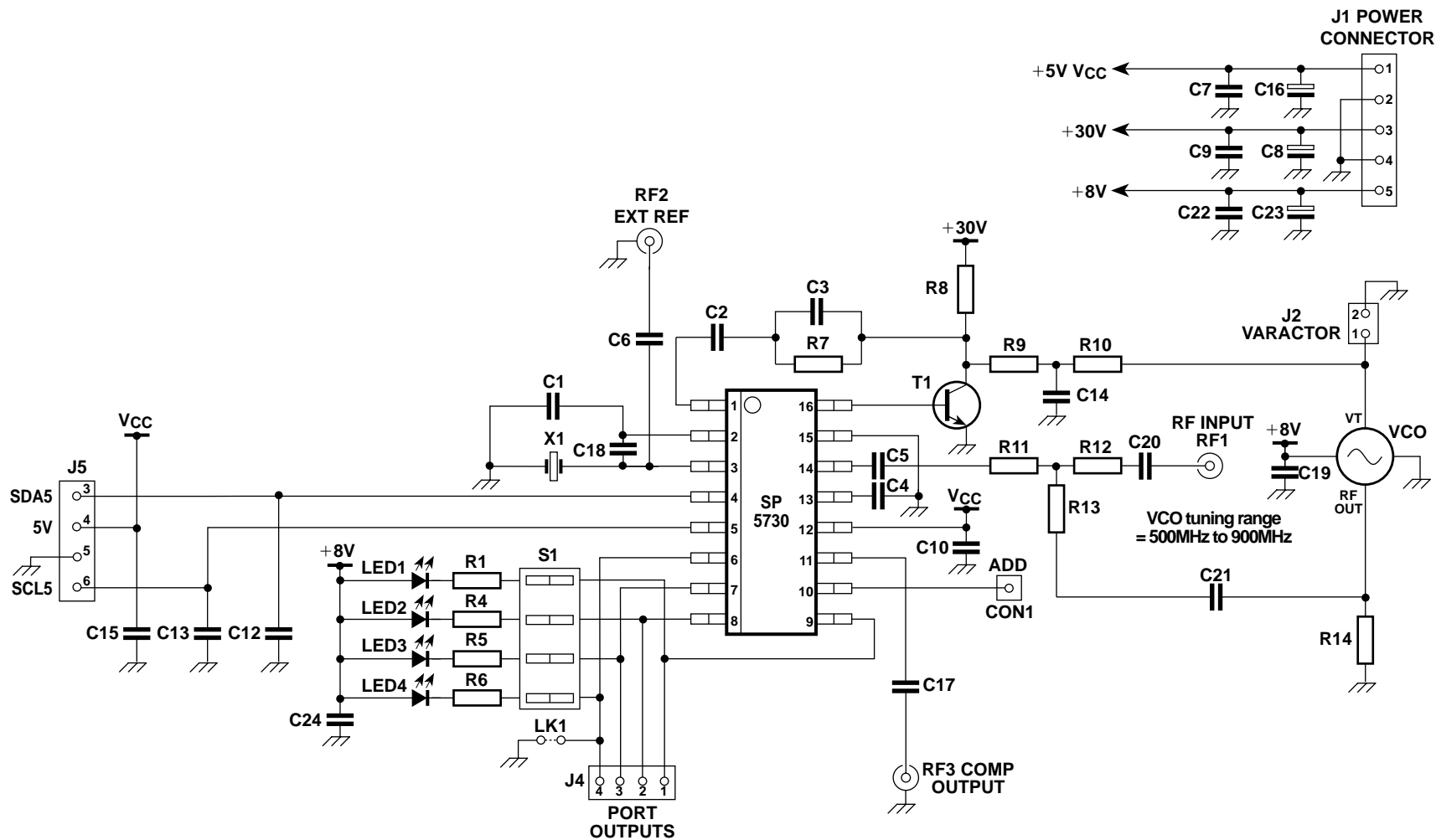


Figure 5 - Crystal oscillator application

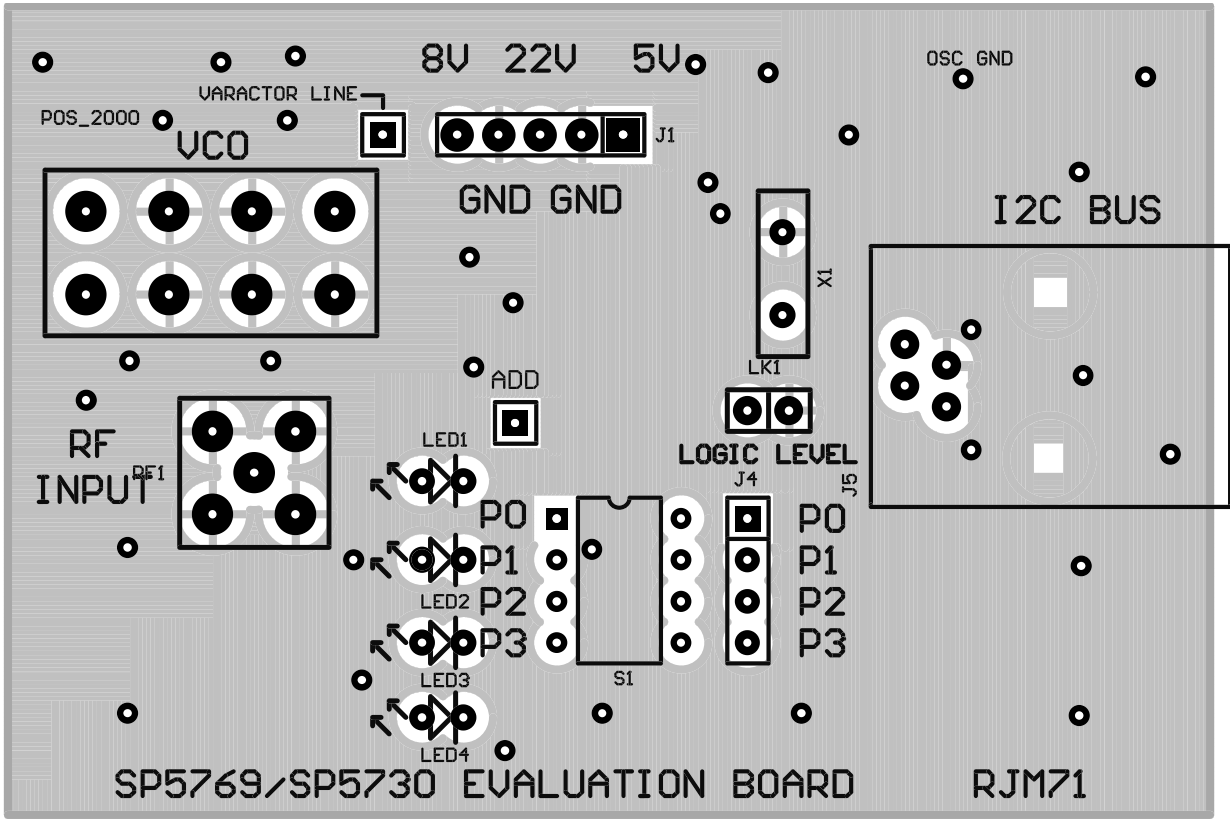
Figure 6 - SP5730 evaluation board



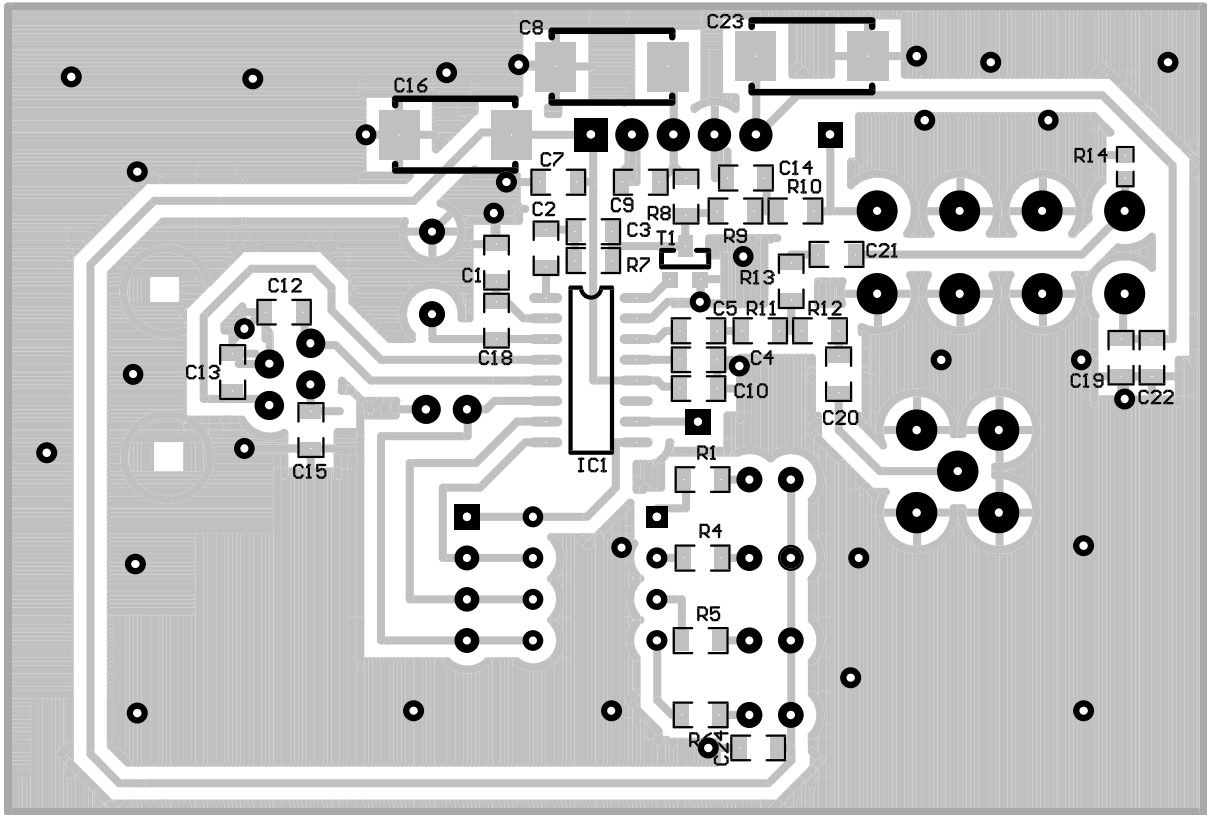
| Component | Value/type | Component | Value/type |
|-----------|------------|-----------|------------|
| C1        | 18pF       | C22       | 100pF      |
| C2        | 2.2nF      | C23       | 4.7μF      |
| C3        | 68pF       | C24       | 1nF        |
| C4        | 1nF        | LED 1     | HLMPK-150  |
| C5        | 1nF        | LED 2     | HLMPK-150  |
| C6        | 10nF       | R1        | 4.7kΩ      |
| C7        | 100nF      | R4        | 4.7kΩ      |
| C8        | 4.7μF      | R5        | 4.7kΩ      |
| C9        | 100nF      | R6        | 4.7kΩ      |
| C10       | 100pF      | R7        | 13.3kΩ     |
| C11       | 1nF        | R8        | 22kΩ       |
| C12       | 100pF      | R9        | 1kΩ        |
| C13       | 100pF      | R10       | 0Ω         |
| C14       | 4.7nF      | R11       | 16Ω        |
| C15       | 100pF      | R12       | 16Ω        |
| C16       | 4.7μF      | R13       | 16Ω        |
| C17       | 10nF       | R14       | 68Ω        |
| C18       | 39pF       | S1        | SW DIP-2   |
| C19       | 100pF      | T1        | BCW31      |
| C20       | 1nF        | VCO       | POS_900    |
| C21       | 1nF        | X1        | 4MHz       |

**Table 9 - Component values for Figure 6**



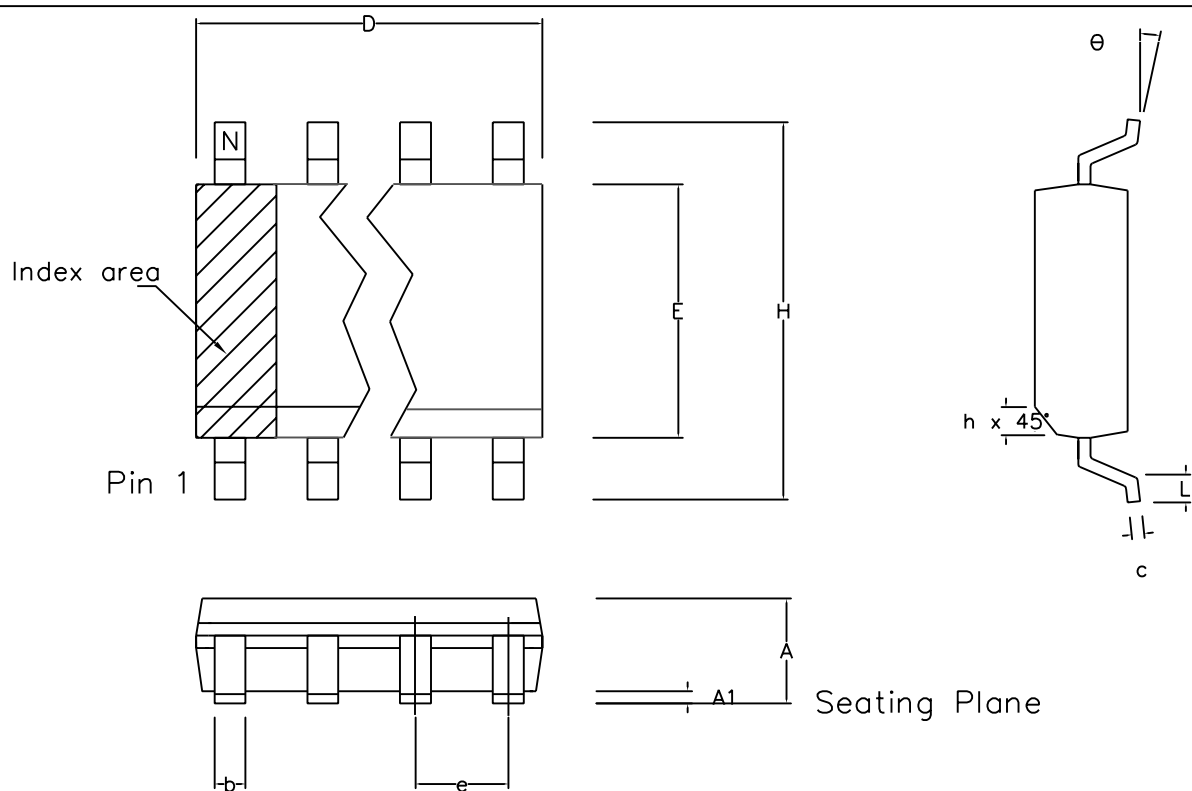


Top view



Bottom view


Figure 7 - SP5730 evaluation board layout

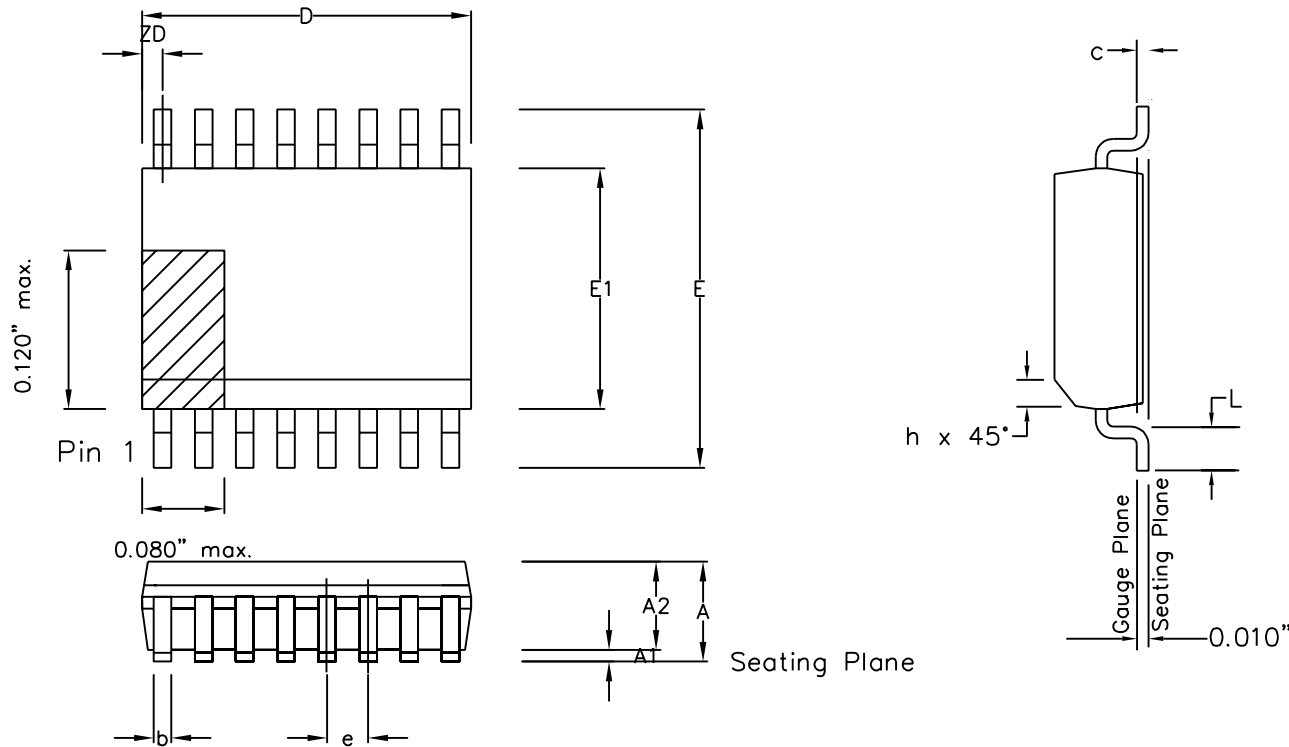


|                                   | Min mm   | Max mm | Min inch  | Max inch |
|-----------------------------------|----------|--------|-----------|----------|
| A                                 | 1.35     | 1.75   | 0.053     | 0.069    |
| A1                                | 0.10     | 0.25   | 0.004     | 0.010    |
| D                                 | 9.80     | 10.00  | 0.386     | 0.394    |
| H                                 | 5.80     | 6.20   | 0.228     | 0.244    |
| E                                 | 3.80     | 4.00   | 0.150     | 0.157    |
| L                                 | 0.40     | 1.27   | 0.016     | 0.050    |
| e                                 | 1.27 BSC |        | 0.050 BSC |          |
| b                                 | 0.33     | 0.51   | 0.013     | 0.020    |
| c                                 | 0.19     | 0.25   | 0.008     | 0.010    |
| O                                 | 0°       | 8°     | 0°        | 8°       |
| h                                 | 0.25     | 0.50   | 0.010     | 0.020    |
| Pin Features                      |          |        |           |          |
| N                                 | 16       |        | 16        |          |
| Conforms to JEDEC MS-012AC Iss. C |          |        |           |          |

Notes:

1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

|   |        |         |         |        |         |   |                                  |  |
|---|--------|---------|---------|--------|---------|---|----------------------------------|--|
| © Zarlink Semiconductor 2002 All rights reserved. |        |         |         |        |         |  <b>ZARLINK</b><br>SEMICONDUCTOR | Package Code DC                  |  |
| ISSUE   | 1      | 2       | 3       | 4      | 5       |   | Previous package codes<br>MP / S | Package Outline for<br>16 lead SOIC<br>(0.150" Body Width) |
| ACN   | 6745   | 201938  | 202597  | 203706 | 212431  |   |                                  |  |
| DATE  | 7Apr95 | 27Feb97 | 12Jun97 | 9Dec97 | 25Mar02 |   |                                  |  |
| APPRD.  |        |         |         |        |         |   |                                  | GPD00012   |



| Symbol                            | Control Dimensions<br>in inches |       | Altern. Dimensions<br>in millimetres |      |
|-----------------------------------|---------------------------------|-------|--------------------------------------|------|
|                                   | MIN                             | MAX   | MIN                                  | MAX  |
| A                                 | 0.053                           | 0.069 | 1.35                                 | 1.75 |
| A1                                | 0.004                           | 0.010 | 0.10                                 | 0.25 |
| A2                                | —                               | 0.059 | —                                    | 1.50 |
| D                                 | 0.189                           | 0.197 | 4.80                                 | 5.00 |
| ZD                                | 0.009                           | REF.  | 0.23                                 | REF. |
| E                                 | 0.228                           | 0.244 | 5.79                                 | 6.20 |
| E1                                | 0.150                           | 0.157 | 3.81                                 | 3.99 |
| L                                 | 0.016                           | 0.050 | 0.41                                 | 1.27 |
| e                                 | 0.025                           | BSC.  | 0.64                                 | BSC. |
| b                                 | 0.008                           | 0.012 | 0.20                                 | 0.30 |
| c                                 | 0.007                           | 0.010 | 0.18                                 | 0.25 |
| θ                                 | 0°                              | 8°    | 0°                                   | 8°   |
| h                                 | 0.010                           | 0.020 | 0.25                                 | 0.50 |
| Pin features                      |                                 |       |                                      |      |
| N                                 | 16                              |       |                                      |      |
| Conforms to JEDEC MO-137AB Iss. A |                                 |       |                                      |      |

This drawing supersedes  
418/ED/51617/001 (Swindon/Plymouth)

Notes:

1. The chamfer on the body is optional. If it is not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protrusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension.

|   |         |         |        |
|---|---------|---------|--------|
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| ISSUE   | 1       | 2       | 3      |
| ACN   | 201928  | 207313  | 212474 |
| DATE  | 27Feb97 | 24Aug99 | 3Apr02 |
| APPRD.  |         |         |        |



|                        |        |
|------------------------|--------|
| Previous package codes | QP / Q |
|------------------------|--------|

|  |          |
|--|----------|
| Package Code   | DG       |
| Package Outline for 16 lead QSOP (0.150" Body Width) |          |
|  | GPD00290 |



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