SP6025
Dual LLC Synchronous Rectifier

DESCRIPTION

The fundamental of SP6025 synchronous rectifier (SR) driver IC combines our U.S. patented methods that utilize the principle of "prediction" logic circuit and current mode. The IC deliberates previous cycle timing to linear control the SR in present cycle by "predictive" algorithm that makes adjustments to the turn-off time, in order to achieve maximum efficiency and avoid cross-conduction at the same time. Specially, SP6025 is designed for LLC applications, and variable switching frequency system.

The SP6025 is a dual, fast turn-off intelligent controller to drive two N-ch power MOSFETs in LLC resonant converters for synchronous rectification.

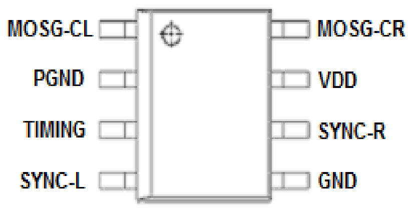
APPLICATIONS

- Storage area network power supplies
- Telecommunication converters
- Embedded systems
- Industrial & commercial systems using high current processors

FEATURES

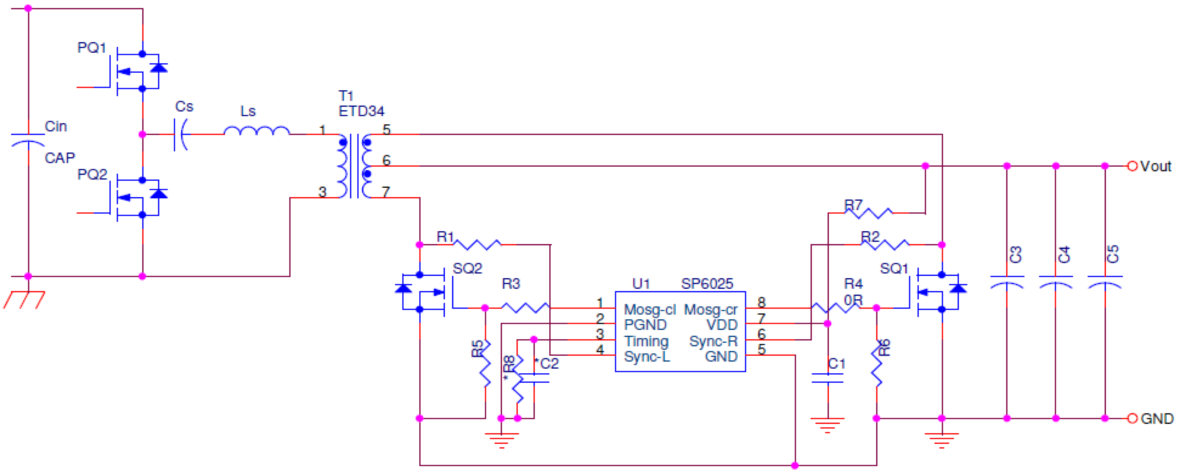
- Offers efficiency improvement over Schottky Diode.
- Low Standby Power to meet DOE Lot 6 Requirement.
- Dual gate driver for N-channel MOSFETs
- Prediction gate timing control.
- Minimum MOSFET body diode conduction.
- Self-detect DCM /CCM to enhance the performance under the variable switching frequency condition.
- Current mode operation in DCM, Prediction mode control in CCM.
- Operating frequency up to 250 KHz.
- Synchronize to transformer secondary voltage waveform.
- Rapid tacking function in prediction mode to adapt rapid load changing.
- Multi-blanking time to avoid the interference of turn on noise.

PIN CONFIGURATION (SOP-8)



PART MARKING

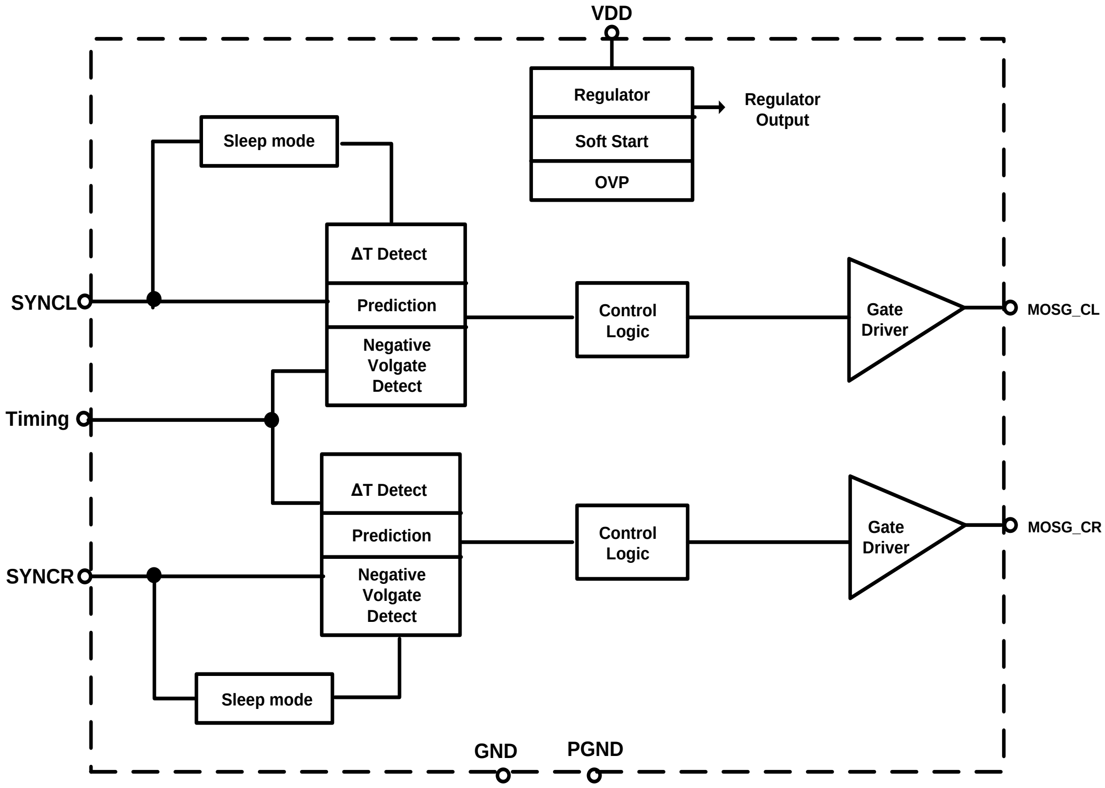
TYPICAL APPLCATION CIRCUIT



PIN DESCRIPTION

Pin	Symbol	Description
1	MOSG_CL	MOSFET_L gate driver.
2	PGND	Power ground connection.
3	TIMING	Discontinuous current filter timing adjustment resistor.
4	SYNC_L	Synchronized signal from the V_{DS} of SR MOSFET.
5	GND	Source pin ground connection.
6	SYNC_R	Synchronized signal from the V_{DS} of SR MOSFET.
7	VDD	DC supply voltage.
8	MOSG_CR	MOSFET_R gate driver.

BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Part Marking
SP6025S8RGB	SOP-8	SP6025

※ SP6025S8RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOULTE MAXIMUM RATINGS (T_A=25℃, unless otherwise specified.)

The following ratings designate persistent limits beyond which damage to the device may occur.

Symbol	Paramete	Value	Unit
V_{DD}	DC Supply Voltage	40	V
SYNC-R/L	Sync input pin(*Internal sync clamp voltage~V_{DD}+1V)	40	V
MOSG-R/L	Output pin	12	V
TIMING	In/Out pin	5.5	V
I_{OUT}	Peak Source Current (Pulsed)	0.35	A
P_D	Power Dissipation @ T_A=25℃ (1)	1.1	W
T_J	Operating Junction Temperature Range	-40 to125	℃
T_{STG}	Storage Temperature Range	-40 to 150	℃
T_{LEAD}	Lead Soldering Temperature for 5 sec.	260	℃

THERMAL RESISTANCE

Symbol	Paramete	Value	Unit
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (2)	90	℃/W
$R_{\theta JC}$	Thermal Resistance Junction to Case (2)	45	℃/W

(1) P_D(MAX) =[T_J(MAX)- T_A]/ θ_{JA}.
(2)The power dissipation and thermal resistance are evaluated under copper board mounted with free air conditions

ELECTRICAL CHARACTERISTICS

(T_A=25℃, V_{DD}=24V, Freq. =50 KHz, Duty Cycle=50%, unless otherwise specified.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SUPPLY INPUT						
I_{DD}	Supply current	No load	2	3	4	mA
		V_{SYNC}=V_{DD}, (Sleep mode)	0.15	0.22	0.45	mA
I_{DD} Clamp	Clamp current	V_{DD}=37V		1.5		mA
		V_{DD}=38.5V		6	10	mA
V_{DD} on	Enable voltage		3.15	3.35	3.75	V
V_{DD} hysteresis	Enable voltage		0.1	0.3	0.5	V
V_{OVP}	Over voltage protection		33	35	37	V
V_{OVP} hysteresis			1	3	5	V
SYNC REFERENCE (SYNC)						
V_{SYNC}_on	Turn-on threshold			-250		mV
V_{Gate}_low	Gate pull low threshold			-35		mV
V_{SYNC}_off	Turn-off threshold			20		mV
I_{SYNC}	Sync input current	$[V_{DS}-(V_{DD}+1)]/R_{SYNC}$, R_{SYNC}=1KΩ			30	mA
V_{SYNC}_clamp	Sync clamp voltage (3)			V_{DD}+1		V
CONTROL CIRCUIT SECTION						
TDon	Turn-on delay	C_{LOAD}=4.7nF,V_{GS}=2V		145	165	nS
TDoff	Turn-off total delay	V_{SYNC}=0V,C_{LOAD}=4.7nF, R_{GATE}=0Ω, V_{GS}=2V		55	65	nS
TBon	Turn-on total blanking time			1		uS
VBoff	Turn-off blanking V_{DS} threshold			1.8		V
Ttiming	Falling slope detection timer Vsync from 1.8V to -50mV	Rtiming=100KΩ		130		nS
Vtiming	Reference Voltage	Rtiming=100KΩ	1.155	1.195	1.23	V
T_{LL1}	Light-load-enter pulse width	SR MOS V_{DS} pulse width<T_{LL1}		1		uS
T_{LL-DEL}	Light-load-enter delay	Continuous counting cycles		4		cycle
T_{LL2}	Light-load-enter pause width	SR MOS V_{DS} pulse width>T_{LL2}		20		uS
Tpred	Prediction time	Fixed setting		175	300	nS
MOSFET GATE DRIVER(MOSG-C)						
Vout_Pred	Output clamp voltage in Prediction mode	Trising < Tset of rising		9.5		V
Vout_Current	Output clamp voltage in Current mode	Trising > Tset of rising		6.5		V
Tr	Rise time	Load=4.7nF(4)		250		nS
Tf	Fall time	Load=4.7nF(4)		15		nS
	Pull up impedance	Peak current		14		Ω
	Pull down impedance			0.8		Ω

Notes:
(3) See application note: calculation formula 7.2
(4) Guaranteed by design and characterization

PERFORMANCE CHARACTERISTICS (T_A=25℃, unless otherwise specified.)

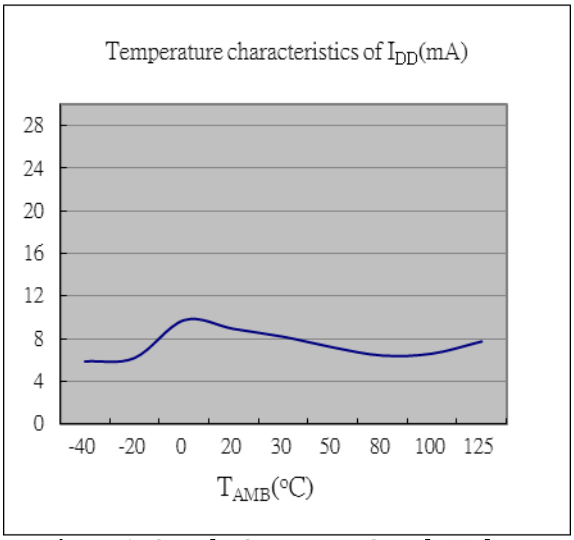


Figure 1: Supply Current vs Supply Voltage

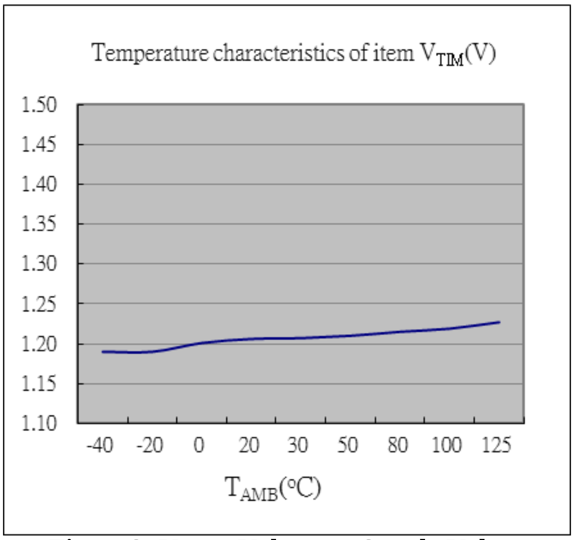


Figure 2: V_{Timing} Voltage vs Supply Voltage

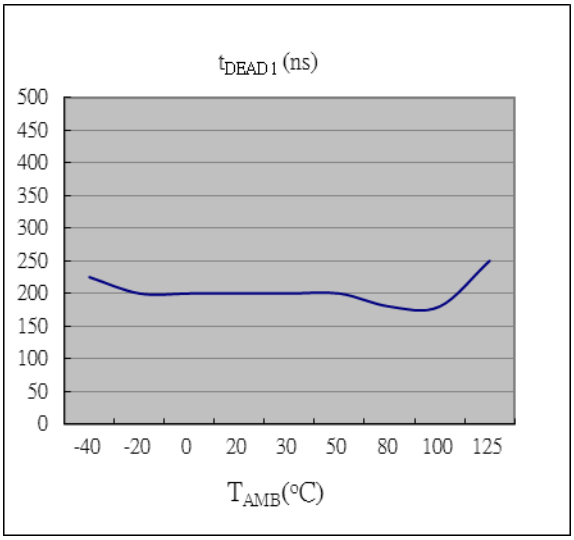


Figure 3: $t_{DEAD\ 1}$vs Temperature (℃)

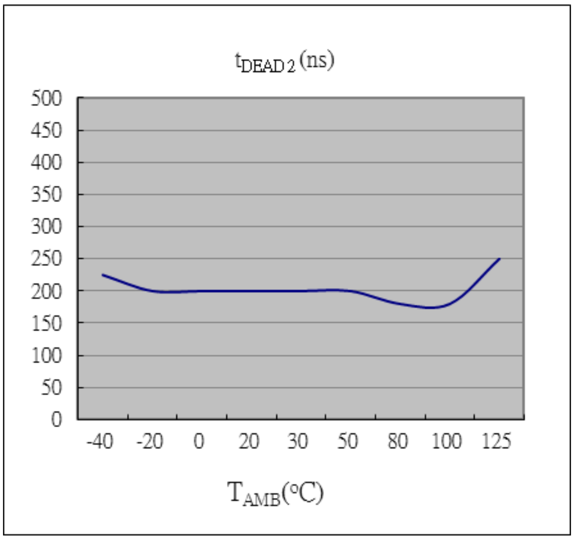
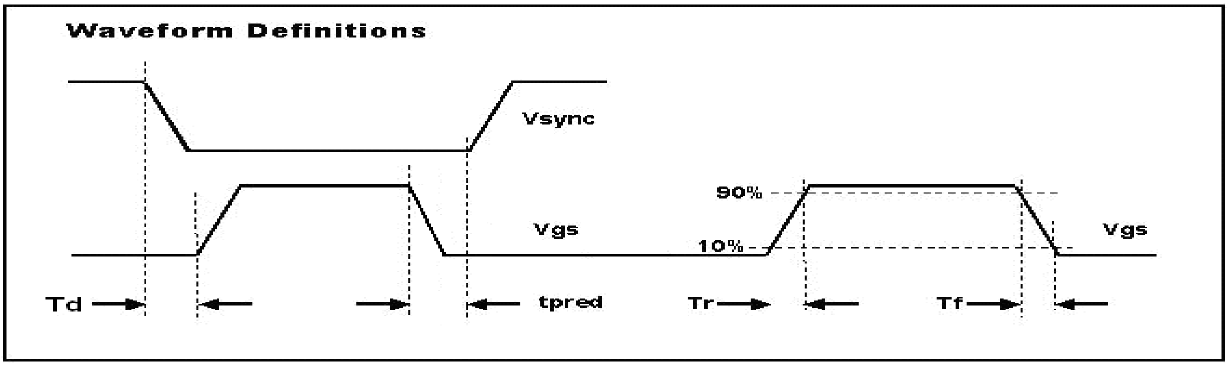


Figure 4: $t_{DEAD\ 2}$ vs Temperature (℃)

(*) Tr & Tf are measured among 10% and 90% of starting and final voltage.



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