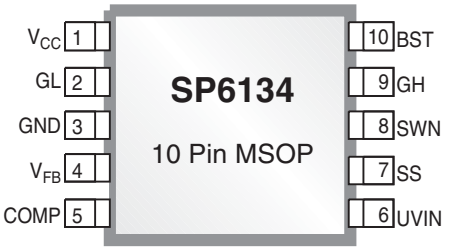
SP6134

Dual Supply Synchronous Buck Controller

FEATURES

- 3V to 15V Step Down Achieved Using Dual Input
- Small 10-Pin MSOP Package
- 2A to 15A Ouput Capability
- Highly Integrated Design, Minimal Components
- UVLO Detects Both V_{CC} and V_{IN}
- Short Circuit Protection with Auto-Restart
- On-Board 1.5Ω sink (2Ω source) NFET Drivers
- Programmable Soft Start
- Fast Transient Response
- High Efficiency: Greater than 94% Possible
- Asynchronous Start-Up into a Pre-Charged Output
- U.S. Patent #6,922,041



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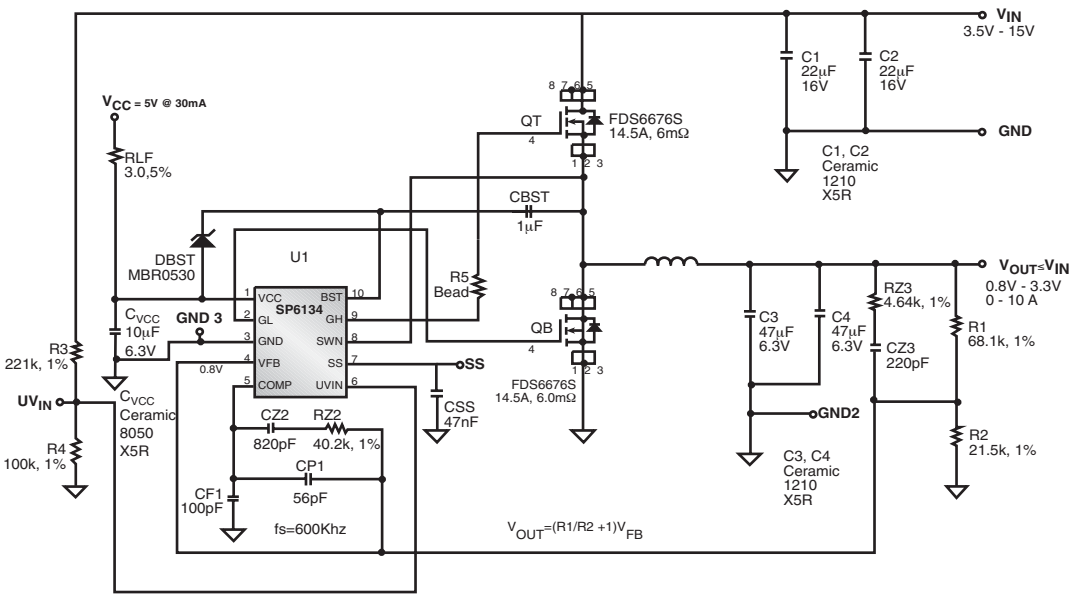
APPLICATIONS

- 12V DPA
- Communications Systems
- Graphics Cards

DESCRIPTION

The SP6134 is a synchronous step-down switching regulator controller optimized for high efficiency. The part is designed to be especially attractive for dual supply, 12V step down with 5V used to power the controller. This lower V_{CC} voltage minimizes power dissipation in the part. The SP6134 is designed to drive a pair of external NFETs using a fixed 600kHz frequency, PWM voltage mode architecture. Protection features include UVLO, thermal shutdown and output short circuit protection. The SP6134 is available in the cost and space saving 10-pin MSOP.

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} 7V
BST 22V
BST-SWN ..... -0.3V to 7V
SWN ..... -1V to 15V
GH ..... -0.3V to BST+0.3V
GH-SWN 7V
All other pins ..... -0.3V to V_{CC}+0.3V

Peak Output Current < 10us
GH,GL 2A

Storage Temperature ..... -65°C to 150°C
Power Dissipation 1W
Lead Temperature (Soldering, 10 sec) ..... 300°C
ESD Rating ..... 2kV HBM
Thermal Resistance ..... 41.9°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified: 0°C < T_{AMB} < 70°C, 4.5V < V_{CC} < 5.5V, BST=V_{CC},SWN = GND = 0V, UVIN = 3.0V, CV_{CC} = 10µF, C_{COMP} = 0.1µF, CGH = CGL = 3.3nF, C_{SS} = 50nF, Typical measured at V_{CC}=5V. The ♦ denotes the specifications which apply over the full operating temperature range, unless otherwise specified.

PARAMETER	MIN	TYP	MAX	UNITS	♦	CONDITIONS
QUIESCENT CURRENT						
V_{CC} Supply Current		1.5	3	mA		V_{FB} =0.9V (No switching)
BST Supply Current		0.2	0.4	mA	♦	V_{FB} =0.9V (No switching)
PROTECTION: UVLO						
V_{CC} UVLO Start Threshold	4.00	4.25	4.5	V	♦	
V_{CC} UVLO Stop Threshold	3.80	4.05	4.4	V	♦	
V_{CC} UVLO Hysteresis	100	200	300	mV		
UVIN Start Threshold	2.3	2.5	2.65	V	♦	
UVIN Stop Threshold	2.0	2.2	2.35	V	♦	
UVIN Hysteresis		300		mV		
ERROR AMPLIFIER REFERENCE						
Error Amplifier Reference	0.792	0.800	0.808	V		2X Gain Config., Measure COMP/2
Error Amplifier Reference Over Line and Temperature	0.788	0.800	0.812	V	♦	
Error Amplifier Transconductance		6		ms		
Error Amplifier Gain		60		dB		No Load
COMP Sink Current		150		µA		V_{FB} = 0.9V, COMP = 0.9V
COMP Source Current		150		µA		V_{FB} = 0.7V, COMP = 2.2V
V_{FB} Input Bias Current		50	200	nA	♦	V_{FB} = 0.8V
Internal Pole		4		MHz		
COMP Clamp		2.5		V		V_{FB}=0.7V, T_A = 25°C
COMP Clamp Temp. Coefficient		-2		mV/°C		
CONTROL LOOP: PWM COMPARATOR, RAMP & LOOP DELAY PATH						
Ramp Amplitude	0.92	1.1	1.28	V	♦	
RAMP Offset		1.1		V		T_A = 25°C, RAMP COMP until GH starts switching
RAMP Offset Temp. Coefficient		-2		mV/°C		
GH Minimum Pulse Width		90	180	ns	♦	
Maximum Controllable Duty Ratio	92	97		%	♦	Maximum Duty Ratio Measured just before pulse skipping begins
Maximum Duty Ratio	100			%		Valid for 20 Cycles
Internal Oscillator Frequency	540 510	600 600	660 690	kHz	♦	

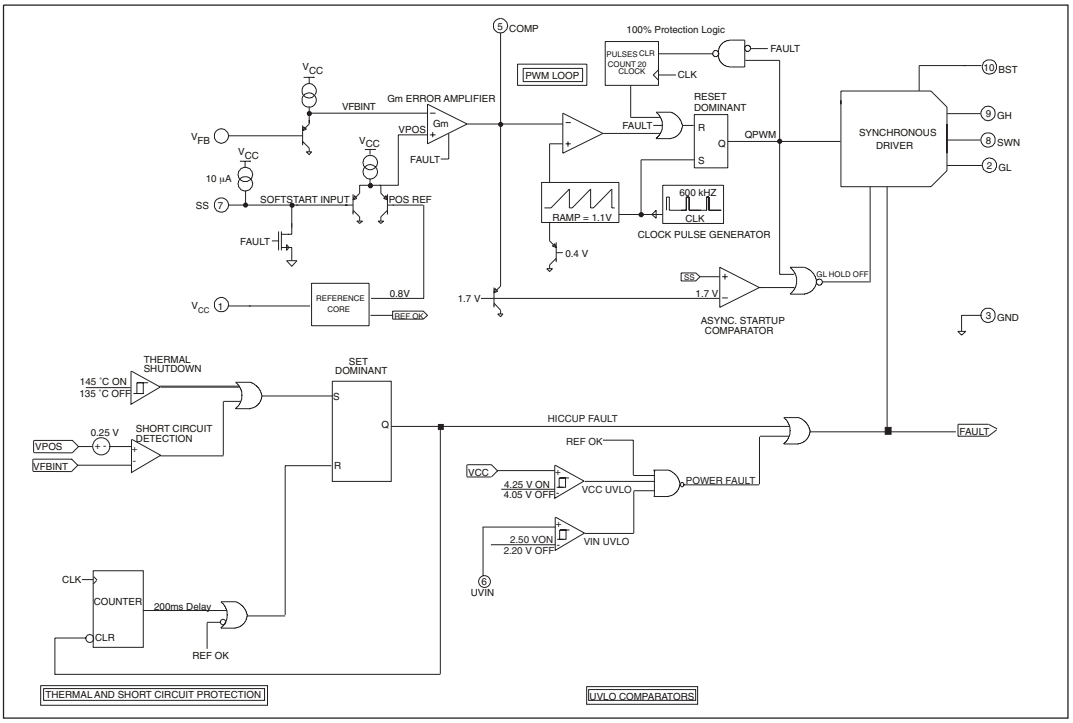
Unless otherwise specified: 0°C < T_{AMB} < 70°C, 4.5V < V_{CC} < 5.5V, BST=V_{CC},SWN = GND = 0V, UVIN = 3.0V, CV_{CC} = 10µF, C_{COMP} = 0.1µF, CGH = CGL = 3.3nF, C_{SS} = 50nF, Typical measured at V_{CC}=5V. The ♦ denotes the specifications which apply over the full operating temperature range, unless otherwise specified.

PARAMETER	MIN	TYP	MAX	UNITS	♦	CONDITIONS
TIMERS: SOFTSTART						
SS Charge Current:		10		µA		
SS Discharge Current:	1			mA	♦	Fault Present, SS = 0.2V
PROTECTION: SHORT CIRCUIT & THERMAL						
Short Circuit Threshold Voltage	0.2	0.25	0.3	V	♦	Measured V_{REF} (0.8V) - V_{FB}
Hiccup Timeout		100		ms		V_{FB} = 0V
Number of Allowable Clock Cycles at 100% Duty Cycle		20		Cycles		V_{FB} = 0.7V
Minimum GL Pulse After 20 Cycles		0.5		Cycles		V_{FB} = 0.7V
Thermal Shutdown Temperature		145		°C		
Thermal Recovery Temperature		135		°C		
Thermal Hysteresis		10		°C		
OUTPUT: NFET GATE DRIVERS						
GH & GL Rise Times		35	50	ns	♦	Measured 10% to 90%
GH & GL Fall Times		30	40	ns	♦	Measured 90% to 10%
GL to GH Non Overlap Time		45	70	ns	♦	GH & GL Measured at 2.0V
SWN to GL Non Overlap Time		20	30	ns	♦	Measured SWN = 100mV to GL = 2.0V
GH & GL Pull Down Resistance		50		KΩ		Resistor Pull-Down
Driver Pull Down Resistance		1.5	1.9	Ω	♦	Note 1
Driver Pull Up Resistance		2.5	3.0	Ω	♦	Note 1

Note 1: Gauranteed by design, not 100% tested.

PIN #	PIN NAME	DESCRIPTION
1	V_{CC}	Bias Supply Input. Connect to external 5V supply. Used to power internal circuits and low side gate driver.
2	GL	High current driver output for the low side NFET switch. It is always low if GH is high or during a fault. Resistor pull down ensure low state at low voltage.
3	GND	Ground Pin. The control circuitry of the IC and lower power driver are referenced to this pin. Return separately from other ground traces to the (-) terminal of C_{OUT}.
4	V_{FB}	Feedback Voltage and Short Circuit Detection pin. It is the inverting input of the Error Amplifier and serves as the output voltage feedback point for the Buck Converter. The output voltage is sensed and can be adjusted through an external resistor divider. Whenever V_{FB} drops 0.25V below the positive reference, a short circuit fault is detected and the IC enters hiccup mode.
5	COMP	Output of the Error Amplifier. It is internally connected to the non-inverting input of the PWM comparator. An optimal filter combination is chosen and connected to this pin and either ground or V_{FB} to stabilize the voltage mode loop.
6	UVIN	UVLO input for V_{IN} voltage. Connect a resistor divider between V_{IN} and UVIN to set minimum operating voltage.
7	SS	Soft Start. Connect an external capacitor between SS and GND to set the soft start rate based on the 10μA source current. The SS pin is held low via a 1mA (min) current during all fault conditions.
8	SWN	Lower supply rail for the GH high-side gate driver. Connect this pin to the switching node at the junction between the two external power MOSFET transistors.
9	GH	High current driver output for the high side NFET switch. It is always low if GL is high or during a fault. Resistor pull down ensure low state at low voltage.
10	BST	High side driver supply pin. Connect BST to the external boost diode and capacitor as shown in the Typical Application Circuit on page 1. High side driver is connected between BST pin and SWN pin.

FUNCTIONAL DIAGRAM



THEORY OF OPERATION

General Overview

The SP6134 is a fixed frequency, voltage mode, synchronous PWM controller optimized for high efficiency. The part has been designed to be especially attractive for split plane applications utilizing 5V to power the controller and 3V to 12V for step down conversion.

The heart of the SP6134 is a wide bandwidth transconductance amplifier designed to accommodate Type II and Type III compensation schemes. A precision 0.8V reference present on the positive terminal of the error amplifier permits the programming of the output voltage down to 0.8V via the V_{FB} pin. The output of the error amplifier, COMP, compared to a 1.1V peak-to-peak ramp is responsible for trailing edge PWM control. This voltage ramp and PWM control logic are governed by the internal oscillator that accurately sets the PWM frequency to 600kHz.

The SP6134 contains two unique control features that are very powerful in distributed applications. First, asynchronous driver control is enabled during start up to prohibit the low side NFET from pulling down the output until the high side NFET has attempted to turn on. Second, a 100% duty cycle timeout ensures that the low side NFET is periodically enhanced during extended periods at 100% duty cycle. This guarantees the synchronized refreshing of the BST capacitor during very large duty ratios.

The SP6134 also contains a number of valuable protection features. A programmable input (V_{IN}) UVLO allows a user to set the exact value at which the conversion voltage is at a safe point to begin down conversion, and an internal V_{CC} UVLO ensures that the controller itself has enough voltage to properly operate. Other pro-

tection features include thermal shutdown and short-circuit detection. In the event that either a thermal, short-circuit, or UVLO fault is detected, the SP6134 is forced into an idle state where the output drivers are held off for a finite period before a re-start is attempted.

Under Voltage Lock Out (UVLO)

The SP6134 contains two separate UVLO comparators to monitor the bias (V_{CC}) and conversion (V_{IN}) voltages independently. The V_{CC} UVLO threshold is internally set to 4.25V, whereas the V_{IN} UVLO threshold is programmable through the UVIN pin. When the UVIN pin is greater than 2.5V, the SP6134 is permitted to start up pending the removal of all other faults. Both the V_{CC} and V_{IN} UVLO comparators have been designed with hysteresis to prevent noise from resetting a fault.

Soft Start

"Soft Start" is achieved when a power converter ramps up the output voltage while controlling the magnitude of the input supply source current. In a modern step down converter, ramping up the positive terminal of the error amplifier controls soft start. As a result, excess source current can be defined as the current required to charge the output capacitor.

$$IV_{IN} = C_{OUT} * DV_{OUT} / DTSoft\text{-}start$$

The SP6134 provides the user with the option to program the soft start rate by tying a capacitor from the SS pin to GND. The selection of this capacitor is based on the 10uA pull up current present at the SS pin and the 0.8V reference voltage. Therefore, the excess source can be redefined as:

$$IV_{IN} = C_{OUT} * DV_{OUT} * 10\mu A / (C_{SS} * 0.8V)$$

Hiccup

Upon the detection of a power, thermal, or short-circuit fault, the SP6134 is forced into an idle state for 100mS (typical). The SS and COMP pins are immediately pulled low, and the gate drivers are held off for the duration of the timeout period. Power and thermal faults have to be removed before a restart may be attempted, whereas, a short-circuit fault is internally cleared shortly after the fault latch is set. Therefore, a restart attempt is guaranteed every 100mS (typical) as long as the short-circuit condition persists.

Thermal and Short-Circuit Protection

Because the SP6134 is designed to drive large NFETs running at high current, there is a chance that either the controller or power converter will become too hot. Therefore, an internal thermal shutdown (145°C) has been included to prevent the IC from malfunctioning at extreme temperatures.

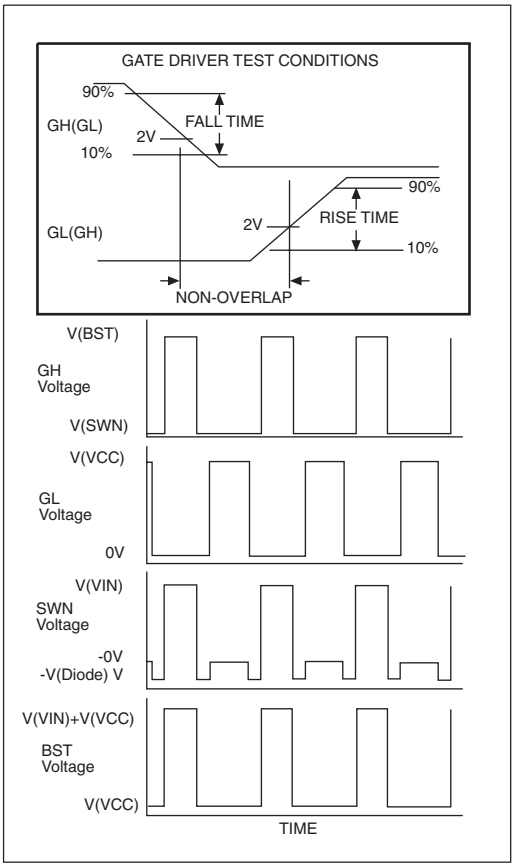
A short-circuit detection comparator has also been included in the SP6134 to protect against the accidental short or sever build up of current at the output of the power converter. This comparator constantly monitors the positive and negative terminals of the error amplifier, and if the V_{FB} pin ever falls more than 250mV (typical) below the positive reference, a short-circuit fault is set. Because the SS pin overrides the internal 0.8V reference during soft start, the SP6134 is capable of detecting short-circuit faults throughout the duration of soft start as well as in regular operation.

Error Amplifier and Voltage Loop

As stated before, the heart of the SP6134 voltage error loop is a high performance, wide bandwidth transconductance amplifier. Because of the amplifier's current limited (+/-150μA) transconductance, there are many ways to compensate the voltage loop or to control the COMP pin externally. If a simple, single pole, single

zero response is required, then compensation can be a simple as an RC to ground. If a more complex compensation is required, then the amplifier has enough bandwidth (45° at 4 MHz) and enough gain (60dB) to run Type III compensation schemes with adequate gain and phase margins at cross over frequencies greater than 50kHz.

The common mode output of the error amplifier is 0.9V to 2.2V. Therefore, the PWM voltage ramp has been set between 1.1V and 2.2V to ensure proper 0% to 100% duty cycle capability. The voltage loop also includes two other very important features. One is an asynchronous start up mode. Basically, the GL driver can not turn on unless the GH driver has attempted to turn on or the SS pin has exceeded 1.7V. This feature prevents the controller from "dragging down" the output voltage during startup or in fault modes. The second feature is a 100% duty cycle timeout that ensures synchronized refreshing of the BST capacitor at very high duty ratios. In the event that the GH driver is on for 20 continuous clock cycles, a reset is given to the PWM flip flop half way through the 21st cycle. This forces GL to rise for the remainder of the cycle, in turn refreshing the BST capacitor.



Gate Drivers

The SP6134 contains a pair of powerful 2Ω SOURCE and 1.5Ω SINK drivers. These state of the art drivers are designed to drive external NFETs capable of handling up to 30A. Rise, fall, and non-overlap times have all been minized to achieve maximum efficiency. All drive pins GH, GL & SWN are monitored continuously to ensure that only one external NFET is ever on at any given time.

Inductor Selection

There are many factors to consider in selecting the inductor including cost, efficiency, size and EMI. In a typical SP6134 circuit, the inductor is chosen primarily for value, saturation current and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response. Low inductor values provide the smallest size, but cause large ripple currents, poor efficiency and more output capacitance to smooth out the larger ripple current. The inductor must also be able to handle the peak current at the switching frequency without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss. A good compromise between size, loss and cost is to set the inductor ripple current to be within 20% to 40% of the maximum output current.

The switching frequency and the inductor operating point determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{IN(\max)} - V_{OUT})}{V_{IN(\max)}\ F_S\ K_r\ I_{OUT(\max)}}$$

where:

Fs = switching frequency

Kr = ratio of the ac inductor ripple current to the maximum output current

The peak to peak inductor ripple current is:

$$I_{PP} = \frac{V_{OUT}(V_{IN(\max)} - V_{OUT})}{V_{IN(\max)}\ F_S\ L}$$

Once the required inductor value is selected, the proper selection of core material is based on peak inductor current and efficiency requirements. The core must be large enough not to saturate at the peak inductor current

$$I_{PEAK} = I_{OUT(\max)} + \frac{I_{PP}}{2}$$

and provide low core loss at the high switching frequency. Low cost powdered iron cores have a gradual saturation characteristic but can introduce considerable ac core loss, especially when the inductor value is relatively low and the ripple current is high. Ferrite materials, on the other hand, are more expensive and have an abrupt saturation characteristic with the inductance dropping sharply when the peak design current is exceeded. Nevertheless, they are preferred at high switching frequencies because they present very low core loss and the design only needs to prevent saturation. In general, ferrite or molypermalloy materials are better choice for all but the most cost sensitive applications.

The power dissipated in the inductor is equal to the sum of the core and copper losses. To minimize copper losses, the winding resistance needs to be minimized, but this usually comes at the expense of a larger inductor. Core losses have a more significant contribution at low output current where the copper losses are at a minimum, and can typically be neglected at higher output currents where the copper losses dominate. Core loss information is usually available from the magnetic vendor.

The copper loss in the inductor can be calculated using the following equation:

$$P_{L(Cu)} = I^2_{L(RMS)}\ R_{WINDING}$$

where $I_{L(RMS)}$ is the RMS inductor current that can be calculated as follows:

$$I_{L(RMS)} = I_{OUT(max)}\sqrt{1 + \frac{1}{3}\left(\frac{I_{PP}}{I_{OUT(max)}}\right)^2}$$

Output Capacitor Selection

The required ESR (Equivalent Series Resistance) and capacitance drive the selection of the type and quantity of the output capacitors. The ESR must be small enough that both the resistive voltage deviation due to a step change in the load current and the output ripple voltage do not exceed the tolerance limits expected on the output voltage. During an output load transient, the output capacitor must supply all the additional current demanded by the load until the SP6134CU adjusts the inductor current to the new value.

Therefore the capacitance must be large enough so that the output voltage is help up while the inductor current ramps up or down to the value corresponding to the new load current. Additionally, the ESR in the output capacitor causes a step in the output voltage equal to the current. Because of the fast transient response and inherent 100% and 0% duty cycle capability provided by the SP6134CU when exposed to output load transient, the output capacitor is typically chosen for ESR, not for capacitance value.

The output capacitor's ESR, combined with the inductor ripple current, is typically the main contributor to output voltage ripple. The maximum allowable ESR required to maintain a specified output voltage ripple can be calculated by:

$$RESR \leq \frac{\Delta V_{OUT}}{I_{PK\text{-}PK}}$$

where:

ΔV_{OUT} = Peak to Peak Output Voltage Ripple

$I_{PK\text{-}PK}$ = Peak to Peak Inductor Ripple Current

The total output ripple is a combination of the ESR and the output capacitance value and can be calculated as follows:

$$\Delta V_{OUT} = \sqrt{\left(\frac{I_{PP}\,(1-D)}{C_{OUT} F_S}\right)^2 + (I_{PP} R_{ESR})^2}$$

where:

F_S = Switching Frequency

D = Duty Cycle

C_{OUT} = Output Capacitance Value

Input Capacitor Selection

The input capacitor should be selected for ripple current rating, capacitance and voltage rating. The input capacitor must meet the ripple current requirement imposed by the switching current. In continuous conduction mode, the source current of the high-side MOSFET is approximately a square wave of duty cycle V_{OUT}/V_{IN}. Most of this current is supplied by the input bypass capacitors. The RMS value of input capacitor current is determined at the maximum output current and under the assumption that the peak to peak inductor ripple current is low, it is given by:

$$I_{CIN(rms)} = I_{OUT(max)} \sqrt{D(1 - D)}$$

The worse case occurs when the duty cycle D is 50% and gives an RMS current value equal to $I_{OUT}/2$.

Select input capacitors with adequate ripple current rating to ensure reliable operation.

The power dissipated in the input capacitor is:

$$P_{CIN} = I^2_{CIN(rms)}\ R_{ESR(CIN)}$$

This can become a significant part of power losses in a converter and hurt the overall energy transfer efficiency. The input voltage ripple primarily depends on the input capacitor ESR and capacitance. Ignoring the inductor ripple current, the input voltage ripple can be determined by:

$$\Delta V_{IN} = I_{out(\max)}\ R_{ESR(CIN)} + \frac{I_{OUT(MAX)} V_{OUT} (V_{IN} - V_{OUT})}{F_S C_{IN} V_{IN}^2}$$

The capacitor type suitable for the output capacitors can also be used for the input capacitors.

However, exercise extra caution when tantalum capacitors are considered. Tantalum capacitors are known for catastrophic failure when exposed to surge current, and input capacitors are prone to such surge current when power supplies are connected "live" to low impedance power sources.

MOSFET Selection

The losses associated with MOSFETs can be divided into conduction and switching losses. Conduction losses are related to the on resistance of MOSFETs, and increase with the load current. Switching losses occur on each on/off transition when the MOSFETs experience both high current and voltage. Since the bottom MOSFET switches current from/to a paralleled diode (either its own body diode or a Schottky diode), the voltage across the MOSFET is no more than 1V during switching transition. As a result, its switching losses are negligible. The switching losses are difficult to quantify due to all the variables affecting turn on/off time. However, the following equation provides an approximation on the switching losses associated with the top MOSFET driven by SP6134.

$$P_{SH(\max)} = 12 C_{rss} V_{IN(\max)} I_{OUT(\max)} F_S$$

where

C_{rss} = reverse transfer capacitance of the top MOSFET

Switching losses need to be taken into account for high switching frequency, since they are directly proportional to switching frequency. The conduction losses associated with top and bottom MOSFETs are determined by:

$$P_{CH(\max)} = R_{DS(ON)} I_{OUT(\max)}{}^2 D$$

$$P_{CL(\max)} = R_{DS(ON)} I_{OUT(\max)}{}^2 (1 - D)$$

where

$P_{CH(max)}$ = conduction losses of the high side MOSFET

$P_{CL(max)}$ = conduction losses of the low side MOSFET

$R_{DS(ON)}$ = drain to source on resistance.

The total power losses of the top MOSFET are the sum of switching and conduction losses. For synchronous buck converters of efficiency over 90%, allow no more than 4% power losses for high or low side MOSFETs. For input voltages of 3.3V and 5V, conduction losses often dominate switching losses. Therefore, lowering the $R_{DS(ON)}$ of the MOSFETs always improves efficiency even though it gives rise to higher switching losses due to increased C_{rss}.

Top and bottom MOSFETs experience unequal conduction losses if their on time is unequal. For applications running at large or small duty cycle, it makes sense to use different top and bottom MOSFETs. Alternatively, parallel multiple MOSFETs to conduct large duty factor.

$R_{DS(ON)}$ varies greatly with the gate driver voltage. The MOSFET vendors often specify $R_{DS(ON)}$ on multiple gate to source voltages (V_{GS}), as well as provide typical curve of $R_{DS(ON)}$ versus V_{GS}. For 5V input, use the $R_{DS(ON)}$ specified at 4.5V V_{GS}. At the time of this publication, vendors, such as Fairchild, Siliconix and International Rectifier, have started to specify $R_{DS(ON)}$ at V_{GS} less than 3V. This has provided necessary data for designs in which these MOSFETs are driven with 3.3V and made it possible to use SP6134 in 3.3V only applications.

Thermal calculation must be conducted to ensure the MOSFET can handle the maximum load current. The junction temperature of the MOSFET, determined as follows, must stay below the maximum rating.

$$T_{J(\max)} = T_{A(\max)} + \frac{P_{MOSFET(\max)}}{R_{\theta JA}}$$

where

$T_{A(max)}$ = maximum ambient temperature

P*MOSFET(max)* = maximum power dissipation of the MOSFET

$R_{\Theta JA}$ = junction to ambient thermal resistance.

$R_{\Theta JA}$ of the device depends greatly on the board layout, as well as device package. Significant

thermal improvement can be achieved in the maximum power dissipation through the proper design of copper mounting pads on the circuit board. For example, in a SO-8 package, placing two 0.04 square inches copper pad directly under the package, without occupying additional board space, can increase the maximum power from approximately 1 to 1.2W. For DPAK package, enlarging the tap mounting pad to 1 square inches reduces the $R_{\Theta}JA$ from 96°C/W to 40°C/W.

Schottky Diode Selection

When paralleled with the bottom MOSFET, an optional Schottky diode can improve efficiency and reduce noises. Without this Schottky diode, the body diode of the bottom MOSFET conducts the current during the non-overlap time when both MOSFETs are turned off. Unfortunately, the body diode has high forward voltage and reverse recovery problem. The reverse recovery of the body diode causes additional switching noises when the diode turns off. The Schottky diode alleviates these noises and additionally improves efficiency thanks to its low forward voltage. The reverse voltage across the diode is equal to input voltage, and the diode must be able to handle the peak current equal to the maximum load current.

The power dissipation of the Schottky diode is determined by

$$P_{DIODE} = 2V_F I_{OUT} T_{NOL} F_S$$

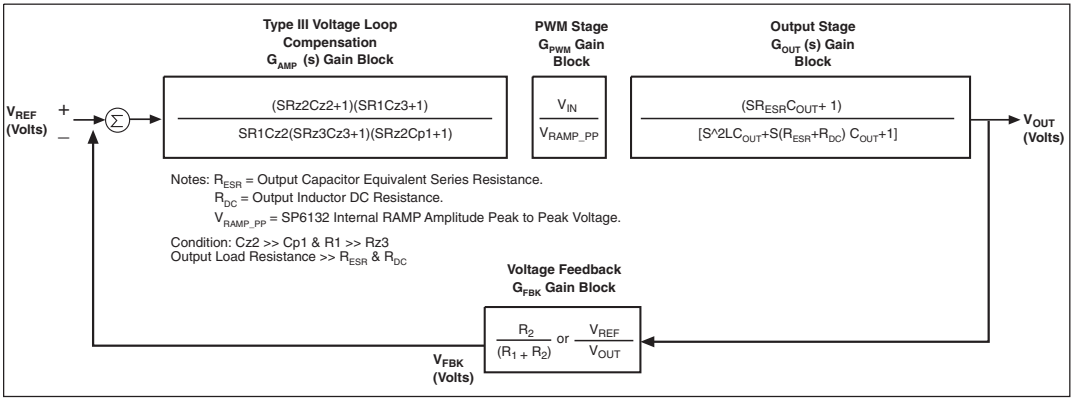
where

T_{NOL} = non-overlap time between GH and GL.

V_F = forward voltage of the Schottky diode.

Loop Compensation Design

The open loop gain of the whole system can be divided into the gain of the error amplifier, PWM modulator, buck converter output stage, and feedback resistor divider. In order to crossover at the selected frequency FCO, the gain of the error amplifier has to compensate for the attenuation caused by the rest of the loop at this frequency.



SP6134 Voltage Mode Control Loop with Loop Dynamic

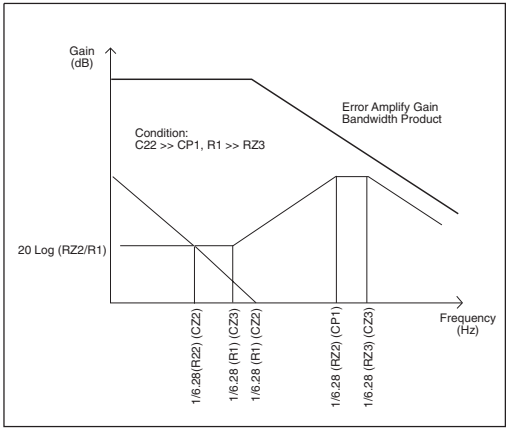
The goal of loop compensation is to manipulate loop frequency response such that its gain crosses over 0db at a slope of -20db/dec. The first step of compensation design is to pick the loop crossover frequency. High crossover frequency is desirable for fast transient response, but often jeopardizes the system stability. Crossover frequency should be higher than the ESR zero but less than 1/5 of the switching frequency. The ESR zero is contributed by the ESR associated with the output capacitors and can be determined by:

$$f_{Z(ESR)} = \frac{1}{2\pi\, C_{OUT}\, R_{ESR}}$$

The next step is to calculated the complex conjugate poles contributed by the LC output filter,

$$f_{P(LC)} = \frac{1}{2\pi\, \sqrt{L\, C_{OUT}}}$$

When the output capacitors are of a Ceramic Type, the SP6134EB Evaluation Board requires a Type III compensation circuit to give a phase boost of 180° in order to counteract the effects of an under damped resonance of the output filter at the double pole frequency.



Bode Plot of Type III Error Amplify Compensation.

INDUCTORS - SURFACE MOUNT							
Inductor Specification							
Inductance (uH)	Manufacturer/Part No.	Series R mΩ	I_{SAT} (a)	Size LxW(mm)	Size Ht.(mm)	Inductor Type	Manufacturer Website
2.7	**Easy Magnet SC5018-2R7M**	**4.30**	**12.0**	**12.6x12.6**	**4.5**	**Shielded Ferrite Core**	inter-technical.com
2.7	TDK RLF 12560T-2R7N110	4.50	12.2	12.5x12.8	6.0	Shielded Ferrite Core	tdk.com
3.3	Coilcraft DO5010P-332HC	8.60	17.0	14.7x15.2	8.0	Unshielded Ferrite Core	coilcraft.com
1.2	Easy Magnet SC5018-1R2M	1.96	20.0	12.6x12.6	4.5	Shielded Ferrite Core	inter-technical.com
1.2	Inter-Technical SC4015-1R2M	4.37	17.0	10.0x10.0	3.8	Shielded Ferrite Core	inter-technical.com
1.5	Coilcraft DO5010P-152HC	4.00	25.0	14.7x15.2	8.0	Unshielded Ferrite Core	coilcraft.com
1.9	TDK RLF 12560T-1R9N120	3.60	13.2	12.5x12.8	6.0	Shielded Ferrite Core	tdk.com

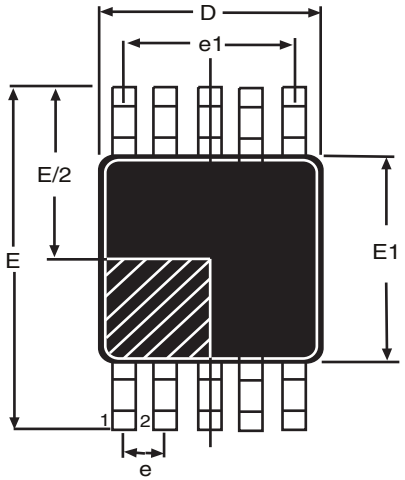
CAPACITORS -SURFACE MOUNT								
Capacitance (uF)	Manufacturer/Part No.	ESR Ω (max)	Ripple Current (A)@45°C	Size LxW(mm)	Size Ht.(mm)	Voltage (V)	Capacitor Type	Manufacturer Website
22	**TDK C3225X5R1C226M**	**0.002**	**4.00**	**3.2x2.5**	**2.0**	**16.0**	**X5R Ceramic**	tdk.com
47	**TDK C3225X5ROJ476M**	**0.002**	**4.00**	**3.2x2.5**	**2.5**	**6.3**	**X5R Ceramic**	tdk.com

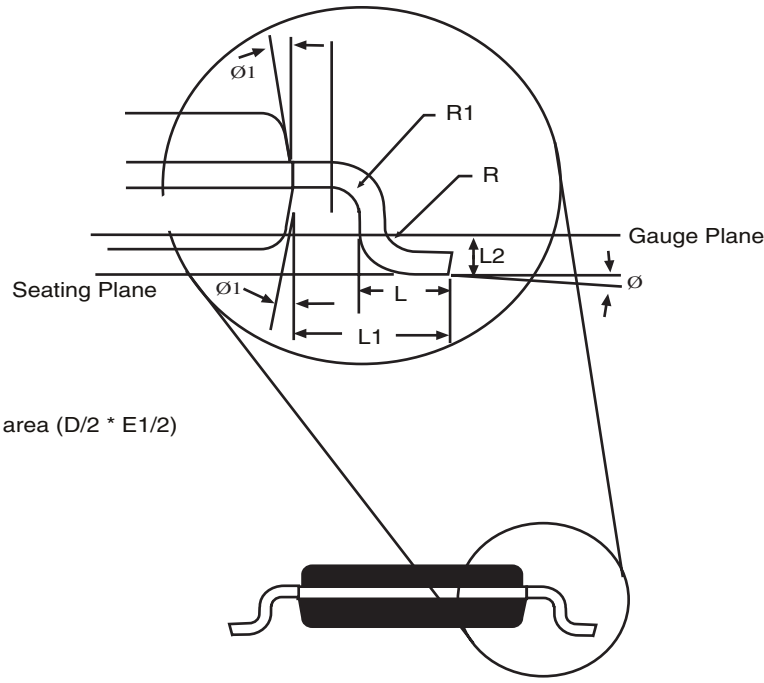
MOSFET - Surface Mount								
MOSFET	Manufacturer/Part No.	RDS (on) Ω (max)	ID Current (A)	Qg nC(Typ)	Qg nC(Max)	Voltage (V)	Foot Print	Manufacturer Website
N-Channel	**Fairchild Semi FDS6676S**	**0.006**	**14.50**	**43**	**60.0**	**30.0**	**SO-8**	fairchildsemi.com
N-Channel	Fairchild Semi FD7088N3	0.005	21.10	37	48.0	30.0	SO-8	fairchildsemi.com
N-Channel	Vishay Si4336DY	0.004	25.0	32	50.0	30.0	SO-8	vishay.com

Note: Components highlighted in Bold are those used on the SP6134 Evaluation Board.

Table 1. Input and Output Stage Components Selection Charts.

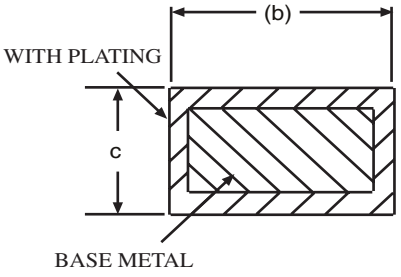
(ALL DIMENSIONS IN MILLIMETERS)

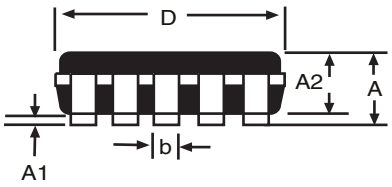




Pin #1 indentifier must be indicated within this shaded area (D/2 * E1/2)

Dimensions in (mm)	10-PIN MSOP JEDEC MO-187 (BA) Variation		
	MIN	NOM	MAX
A	-	-	1.1
A1	0	-	0.15
A2	0.75	0.85	0.95
b	0.17	-	0.27
c	0.08	-	0.23
D	3.00 BSC		
E	4.90 BSC		
E1	3.00 BSC		
e	0.50 BSC		
e1	2.00 BSC		
L	0.4	0.60	0.80
L1	-	0.95	-
L2	-	0.25	-
N	-	10	-
R	0.07	-	-
R1	0.07	-	-
Ø	0°		8°
Ø1	0°	-	15°





ORDERING INFORMATION

Part Number	Top Mark	Temperature	Package
SP6134CU	SP6134CU	0°C to +70°C	10 Pin MSOP
SP6134CU/TR	SP6134CU	0°C to +70°C	10 Pin MSOP
SP6134EU	SP6134EU	-40°C to +85°C	10 Pin MSOP
SP6134EU/TR	SP6134EU	--40°C to +85°C	10 Pin MSOP

Available in lead free packaging. To order add "-L" suffix to part number.

Example: SP6134EU/TR = standard; SP6134EU-L/TR = lead free

/TR = Tape and Reel

Pack quantity is 2500 for MSOP.

Solved by Sipex™

Sipex Corporation

Headquarters and Sales Office
233 South Hillview Drive
Milpitas, CA 95035
TEL: (408) 934-7500
FAX: (408) 935-7600

Appendix and Web Link Information

For further assistance:

Email:	Sipexsupport@sipex.com
WWW Support page:	http://www.sipex.com/content.aspx?p=support
Sipex Application Notes:	http://www.sipex.com/applicationNotes.aspx
Product Change Notices:	http://www.sipex.com/content.aspx?p=pcn

Sipex Corporation
Headquarters and
Sales Office
233 South Hillview Drive
Milpitas, CA95035
tel: (408) 934-7500
faX: (408) 935-7600

The following sections contain information which is more changeable in nature and is therefore generated as appendices.

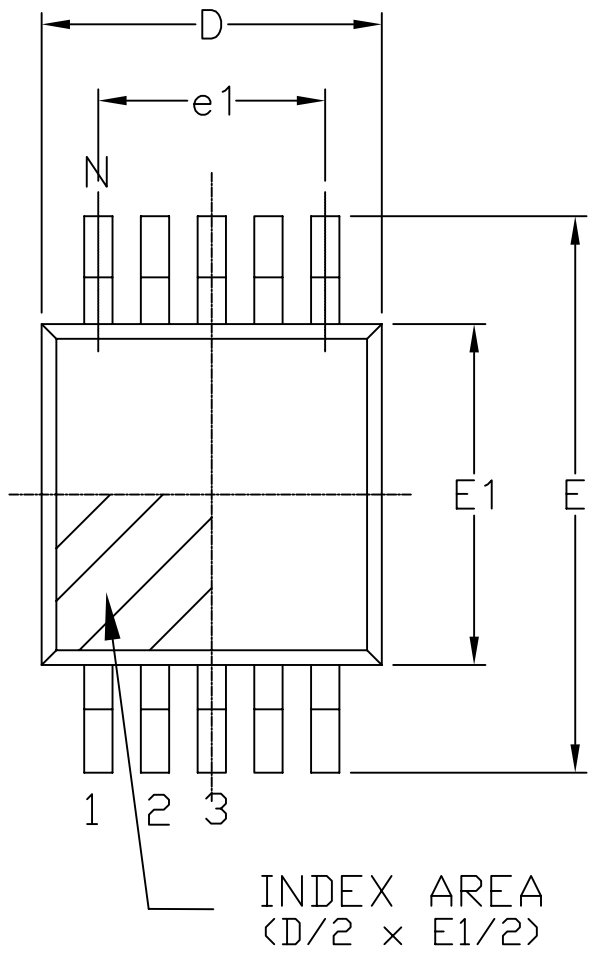
1) **Package Outline Drawings**
2) **Ordering Information**

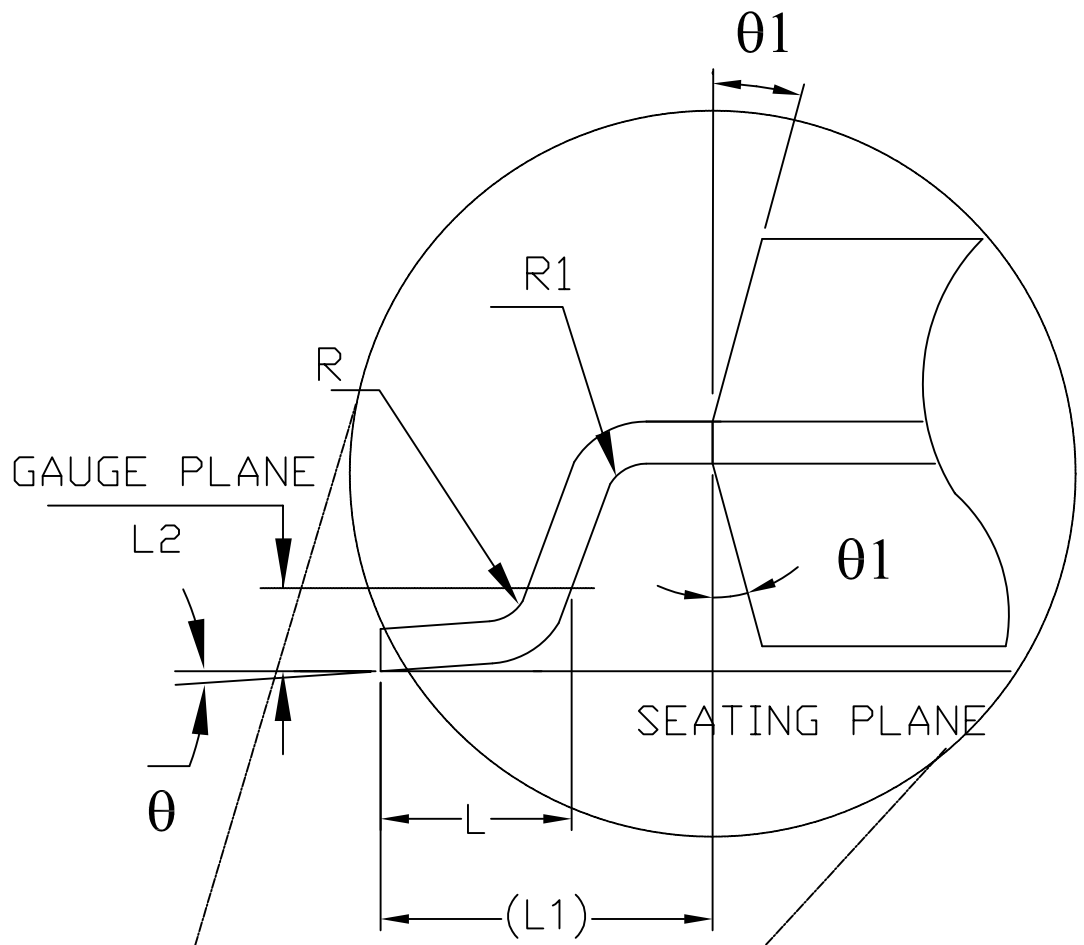
If Available:

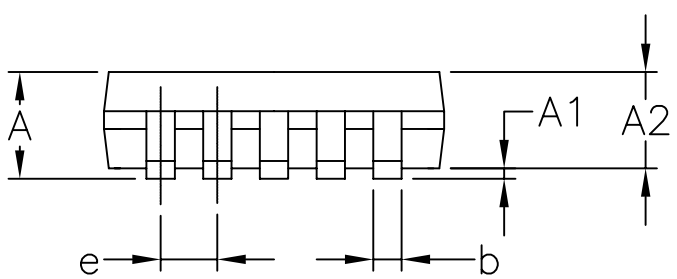
3) **Frequently Asked Questions**
4) **Evaluation Board Manuals**
5) **Reliability Reports**
6) **Product Characterization Reports**
7) **Application Notes for this product**
8) **Design Solutions for this product**

REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	08/09/05	JL
B	DRAWING FORMAT MODIFICATION	07/19/06	JL

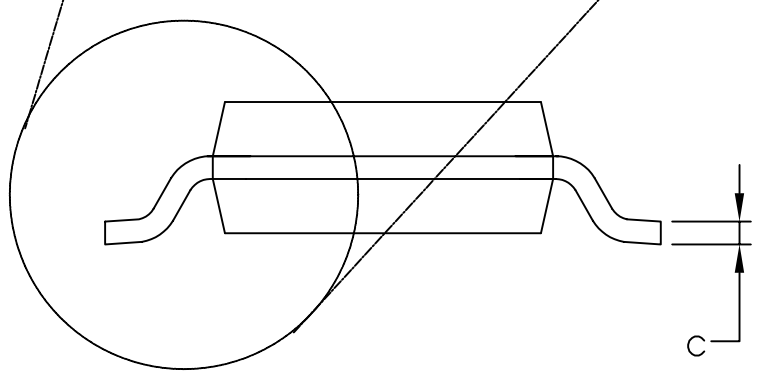
Top View







Side View



Front View

10 Pin MSOP JEDEC MO-187 Variation BA						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.10	—	—	0.043
A1	0.00	—	0.15	0.000	—	0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.17	—	0.33	0.007	—	0.013
c	0.08	—	0.23	0.003	—	0.009
E	4.90 BSC			0.193 BSC		
E1	3.00 BSC			0.118 BSC		
e	0.50 BSC			0.020 BSC		
e1	2.00 BSC			0.079 BSC		
L	0.40	0.60	0.80	0.016	0.024	0.031
L1	0.95 REF			0.037 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
D	3.00 BSC			0.118 BSC		
N	10			10		

Solved by Sipex™

SIPEX CORPORATION			
10 PIN MSOP PACKAGE OUTLINE			
Packaging Approval:		Drawing No:	10-PIN MSOP
By: JL	Date: 07/19/06	Revision: B	Sheet: 1 OF 1

Product Lines

Power Management
- Boost Regulators
- Buck Regulators
- Charge Pumps
- LED Drivers
- Linear Regulators
- Power Blox™
- PWM Controllers
- References
- Supervisors
- USB Vbus Switches

Interface
- Multiprotocol
- RS232
- RS422
- RS485
- USB

Optical Storage
- Advanced Power Control
- Photo Detector IC

SP6134 product details

You are here : Home : Products : PWM Con

Dual-Supply Synchronous Buck Controller

Quick Links
- Download Datasheet
- Check Price Availability

Design-In Supp
- Email: Tech
- PWM Contro Product Sele
- Applications
- Evaluation B
- Quality Infor
- Part Nomen
- Design Solu

Features

- 3V to 15V Step Down Achieved Using Dual Input
- Small 10-PiMSOP Package
- 2A to 15A Output Capability
- Highly Integrated Design, Minimal Components
- UVLO Detects Both VCC and VIN
- Short Circuit Protection with Auto-Restart
- On-Board 1.5Ω sink (2Ω source) NFET Drivers
- Programmable Soft Start
- Fast Transient Response
- High Efficiency: Greater than 94% Possible
- Asynchronous Start-Up into a Pre-Charged Output

Fixed Switching Frequency

Ordering Part Number

Part Number	Package Code	RoHS	MIN. Temp. (°C)	MAX. Temp. (°C)	Status	Buy	Samples
SP6134CU-L	MSOP10	▪	0	70	Active	Buy Now	Order Sa
SP6134CU-L/TR	MSOP10	▪	0	70	Active	Buy Now	Order Sa
SP6134EU-L	MSOP10	▪	-40	85	Active	Buy Now	Order Sa
SP6134EU-L/TR	MSOP10	▪	-40	85	Active	Buy Now	Order Sa
PWM Controller SP6134							
SP6134EB	Board		0	70	Active	Buy Now	Order Sa
SP6134CU	MSOP10		0	70	EOL	Buy Now	
SP6134EU	MSOP10		-40	85	EOL	Buy Now	
SP6134EU/TR	MSOP10		0	70	EOL	Buy Now	
SP6134CU/TR	MSOP10		0	70	OBS	Buy Now	

Part Status Legend

Active - the part is released for sale, standard product.

EOL (End of Life) - the part is no longer being manufactured, there may or may not be inventory still in stock.

CF (Contact Factory) - the part is still active but customers should check with the factory for availability. Longer lead-times may apply.

PRE (Pre-introduction) - the part has not been introduced or the part number is an early version available for sample only.

OBS (Obsolete) - the part is no longer being manufactured and may not be ordered.

NRND (Not Recommended for New Designs) - the part is not recommended for new designs.

APPLICATION NOTE ANP7

Using SP6134 to Provide a High Output Boost to Drive

Introduction

Conventional flat-panel LCDs use cold cathode fluorescent lamps for backlighting. The colors of light that a CCFL emits span the range of the visible spectrum, and a person looking at the backlight sees this mixture of frequencies as white light.

Each pixel has three tiny filters, one red, one green, and one blue; adjusting the amount of light through those filters yields mixtures of various quantities of red, green, and blue light. Because of the way the human eye works, different mixtures of those primary colors are all it takes for a person to perceive all the different colors across the visible spectrum.

In high-end large screen LCD TVs and monitors, manufacturers are now using an array of red, green, and blue LEDs for backlighting. Since the blue and green light from the LEDs can be filtered out completely using appropriate filters, you get the pure, saturated red of a red LED (unlike with the "white" light source of the CCFL, which permits a range of red frequencies through the filter). These pure primary color LEDs therefore provide richer color and sharper contrast, vastly improving viewing quality.

Smaller LCD monitors in applications such as automotive, portable computing, personal video players and industrial applications are increasingly also migrating to LED (white LEDs) for backlighting.

In LCD monitors, the LEDs are connected in series because a series configuration provides inherent brightness and color matching, eliminating the need for ballast resistors or factory calibration.

As an example, a 19-in LCD TV requires 11 LEDs in series, which implies an output voltage requirement as high as 40V. The input supply of such a monitor is usually provided by an adaptor and is 12-15V.

Sipex's SP613X family of controllers can be easily configured in the boost mode to provide a high output voltage boost from a 12V input. Figure 1 shows the circuit schematic for driving 2, 11 LED strings of 60mA current using the SP6134.

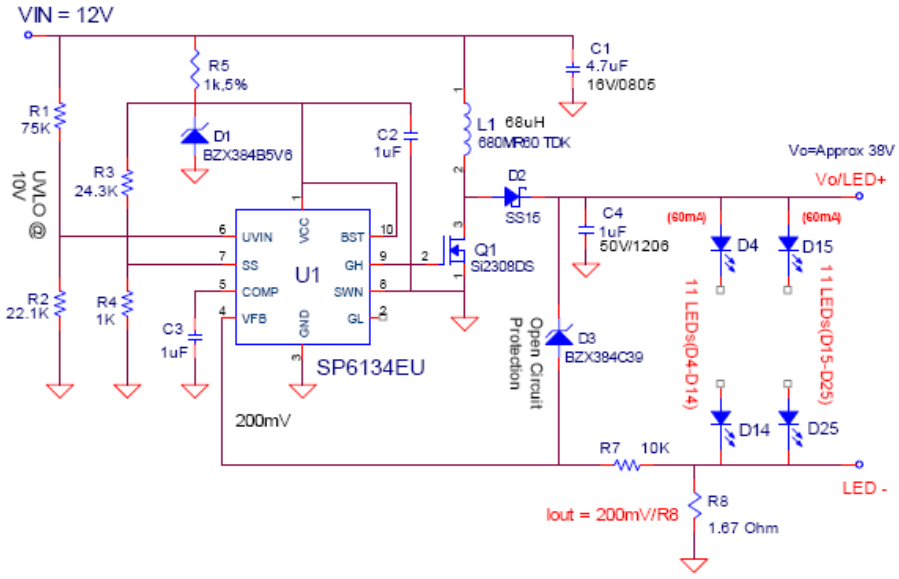


Figure 1- SP6134 configured in the boost mode to drive two 11 LED strings of 60mA each

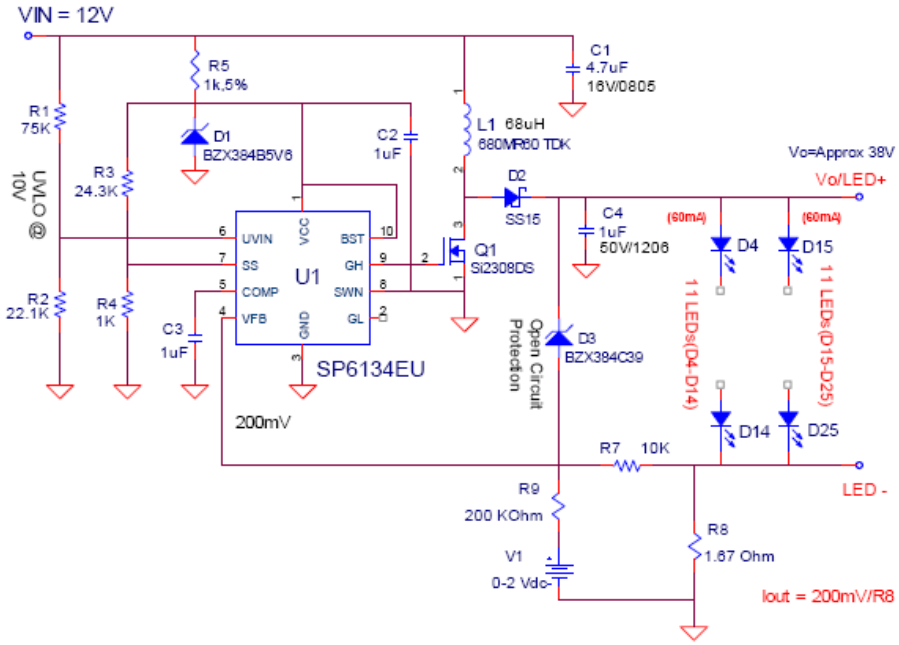


Figure 2- For dimming of LEDs, R9 and variable DC source V1 is added to circuit of figure 1

Theory of Operation

Sipex's SP6134 in figure 1 is configured to perform 2 functions necessary for driving a large number of series connected LEDs: It provides a regulated output current and boosts the output voltage to a value necessary to satisfy the forward voltage drop of LEDs. Higher output voltage is achieved with a standard DC/DC boost function. Current regulation is achieved as follows: a 200 mV reference voltage for error amplifier is obtained through resistor divider R3, R4 from zener D1. This reference forces the voltage at VFB pin and across R8 to be 200mV. An output current of Iout = (200 mV / R8) is established. PWM signal applied to the gate of Q1 will adjust accordingly to maintain the output current.

Setting the output current

The desired output current is set with R8 from R8 = 0.200(V)/Iout, for example to get an output current of 120 mA: R8 = 0.2(V)/0.12(A) = 1.67(Ohm).

Open-Circuit protection

D3 provides circuit protection when the LEDs are disconnected from the circuit or fail open. In this example a **BZX384C39** will clamp the output voltage at 40 V. R7 will limit zener current to 0.2(V)/10(KOhm) = 20(uA).

Schottky diode selection

SP6134's high switching frequency of 600 KHz necessitates a high-speed rectification diode (D2). A Schottky diode is recommended due to its fast recovery time and low Vf. The diode's current and reverse breakdown voltage must satisfy the circuit requirements. For the specific example shown in figure 1 a **SS15** (1A, 50V) was used.

Inductor selection

Inductor value and required current capability have to be determined. Calculate peak inductor current as follows: Let inductor current ripple (ILpp) equal 50% of average inductor current (ILavg) where:
ILavg = (Vin/Vo) x Iload = (38/12) x 0.12 = 0.38 A then:
ILpp = 0.5x0.38 A = 0.19 A,
ILpeak = ILavg + 1/2ILpp = 0.38 + 0.095 = 0.475 A
Calculate L from:
L = [Vin x (Vo – Vin)] / (Vo x f x ILpp) = [12(38 – 12)] / (38 x 600 KHz x 0.19 A) = 72 uH

TDK's SLF7045T- 680MR60 (68 uH, 0.175 Ohm, 0.6 A) is an example that meets above requirements.

Power MOSFET selection

MOSFET voltage and Rds(on) rating have to be determined. When the MOSFET is “OFF” it has to block the output voltage that approaches 40 V. MOSFET voltage rating has to be at least 50 V. Determine the required Rds(on) as follows:

Let MOSFET total losses equal 5% of output power then:

Loss(MOSFET) = 0.05 x 38V x 0.12A = 0.228 W

In this example conduction losses dominate. Calculate Rds(on) from:

Rds(on) = Loss(MOSFET) / $(Irms)^2$:

Let Irms = ILavg (calculated in previous page) then: Rds(on) = 0.228 W / (0.38^2) = 1.6 Ohm

Siliconix’s **Si2308DS** (0.22 Ohm, 60-V) is an example that meets above requirements.

Dimming Control

1-DC voltage

A variable DC voltage V1 as shown in figure 2 can be used for dimming the LEDs. V1 establishes a current in the loop formed by V1, R7, R8 and R9. As V1 increases the loop current (Iloop) increases. Voltage across R8 is reduced by 200 mV – (Iloop x R7). A corresponding reduction in LED current and brightness follows.

2- PWM

The DC source in figure 2 can be replaced with a PWM signal as shown in figure 3. The variable duty cycle PWM and RC filter achieve the same result.

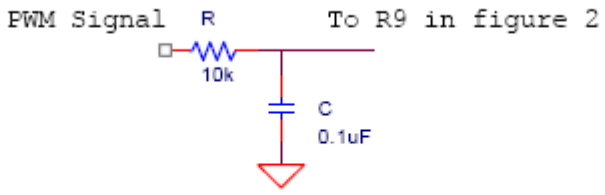


Figure 3- A PWM signal used for LED brightness control

For further assistance:

Email:	Sipexsupport@sipex.com
WWW Support page:	http://www.sipex.com/content.aspx?p=support
Live Technical Chat:	http://www.geolink-group.com/sipex/
Sipex Application Notes:	http://www.sipex.com/applicationNotes.aspx

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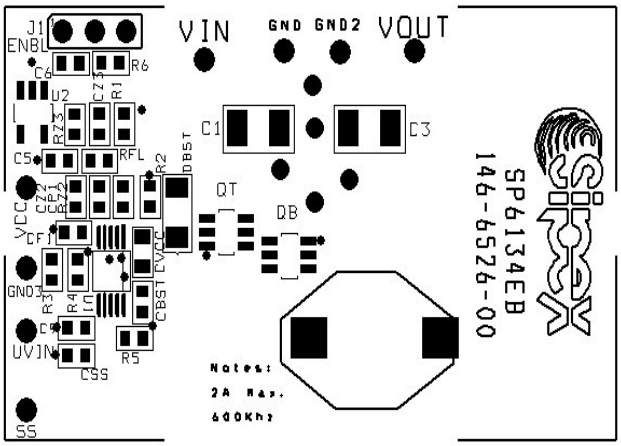
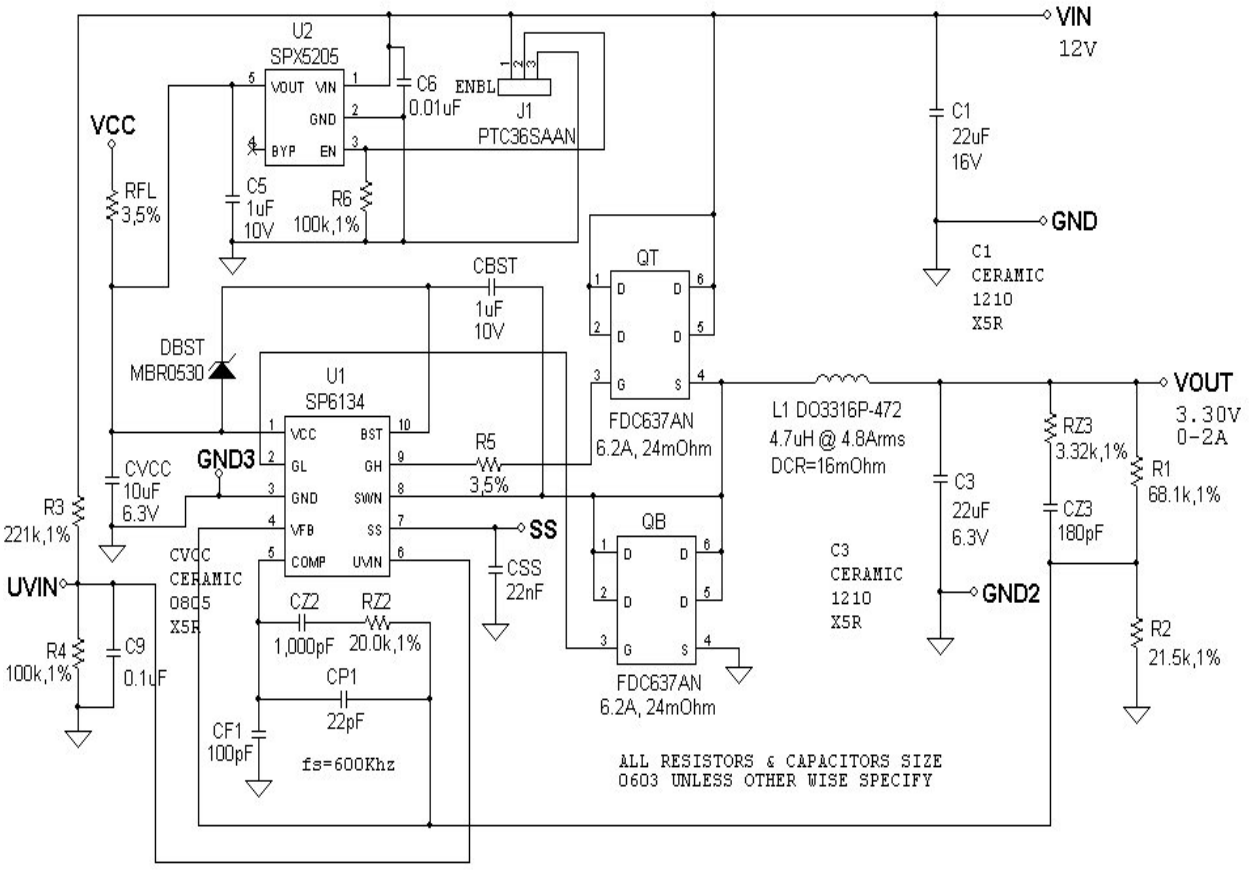
Headquarters and
Sales Office
233 South Hillview Drive
Milpitas, CA95035
tel: (408) 934-7500
faX: (408) 935-7600

SP6134 (2A MAX.) Evaluation Board Manual

- Easy Evaluation for the SP6134CU 12V Input, 0 to 2A Output Synchronous Buck Converter
- Precision 0.80V with ±1% High Accuracy Reference.
- UVIN and Output Dead Short Circuit Shutdown Protection Features.
- High Efficiency: 92%
- Feature Rich: UVIN, Programmable Softstart, External VCC Supply and Output Dead Short Circuit Shutdown Protection.



SP6134EB SCHEMATIC



USING THE EVALUATION BOARD

1) Powering Up the SP6134EB Circuit

Connect the SP6134 Evaluation Board with an external +12V power supply. Connect with short leads and large diameter wire directly to the “VIN” and “GND” posts. Connect a Load between the VOUT and GND2 posts, again using short leads with large diameter wire to minimize inductance and voltage drops.

2) Measuring Output Load Characteristics

It’s best to GND reference scope and digital meters using the Star GND post in the center of the board. VOUT ripple can best be seen touching probe tip to the pad for COUT and scope GND collar touching Star GND post – avoid a GND lead on the scope which will increase noise pickup.

3) Using the Evaluation Board with Different Output Voltages

While the SP6134 Evaluation Board has been tested and delivered with the output set to 3.30V, by simply changing one resistor, R2, the SP6134 can be set to other output voltages. The relationship in the following formula is based on a voltage divider from the output to the feedback pin VFB, which is set to an internal reference voltage of 0.80V. Standard 1% metal film resistors of surface mount size 0603 are recommended.

$$Vout = 0.80V\ (R1 / R2 + 1) \Rightarrow R2 = R1 / [(Vout / 0.80V) - 1\ ]$$

Where R1 = 68.1KΩ and for Vout = 0.80V setting, simply remove R2 from the board. Furthermore, one could select the value of R1 and R2 combination to meet the exact output voltage setting by restricting R1 resistance range such that $50K\Omega \leq R1 \leq 100K\Omega$ for overall system loop stability.

Note that since the SP6134 Evaluation Board design was optimized for 12V down conversion to 3.30V, changes of output voltage and/or input voltage will alter performance from the data given in the Power Supply Data section.

POWER SUPPLY DATA

The SP6134EB is designed with a very accurate 1.0% reference over line, load and temperature. Figure 1 data shows a typical SP6134CU Evaluation Board efficiency plot, with efficiencies to 91% and output currents to 2A. SP6134CU Load Regulation shown in Figure 2 shows only 0.02% change in output voltage from no load to 2A load. Figures 3 and 4 illustrate a 1A to 2A and 0A to 2A Load Steps. Start-up Response in Figures 5, 6 and 7 show a controlled start-up with different output load behavior when power is applied where the input current rises smoothly as the Softstart ramp increases. In Figure 8 the SP6134CU is configured for hiccup mode in response to an output dead short circuit condition and will Softstart until the over-load is removed. Figure 9 and 10 show output voltage ripple less than 22mV at no load to 2A load.

While data on individual power supply boards may vary, the capability of the SP6134CU of achieving high accuracy over a range of load conditions shown here is quite impressive and desirable for accurate power supply design.

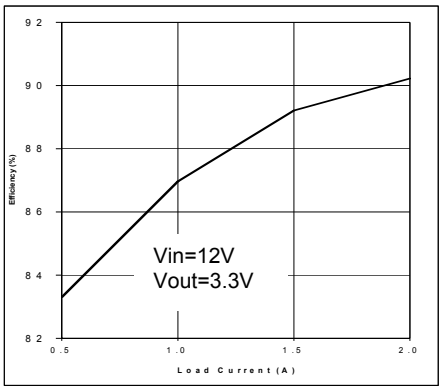


Figure 1. Efficiency vs Load

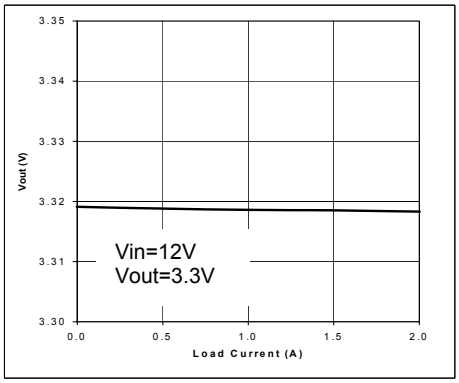


Figure 2. Load Regulation

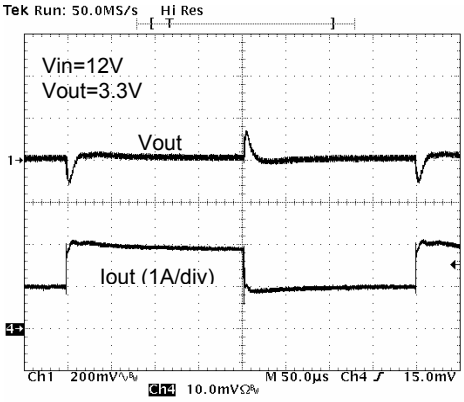


Figure 3. Load Step Response: 1->2A

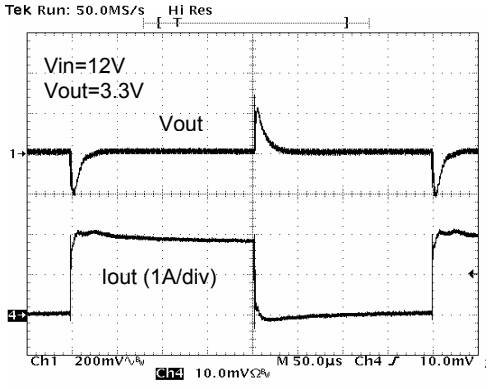


Figure 4. Load Step Response: 0->2A

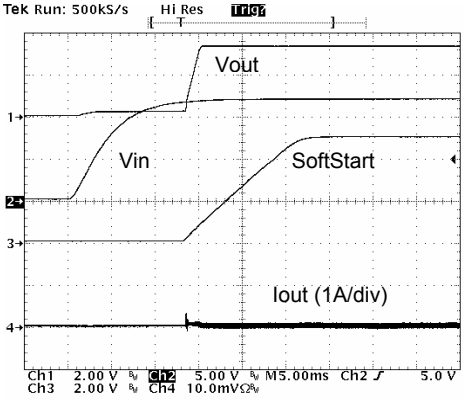


Figure 5. Start-Up Response: No Load

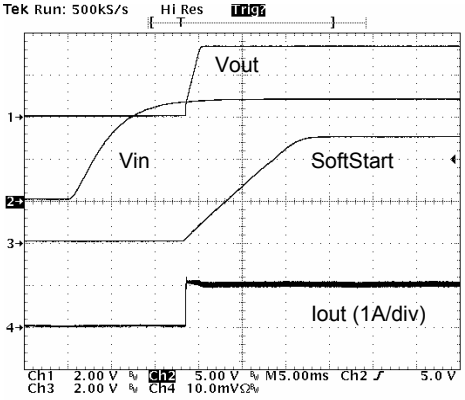


Figure 6. Start-Up Response: 1A Load

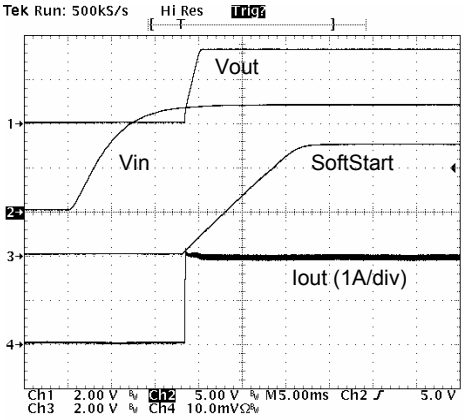


Figure 7. Start-Up Response: 2A Load

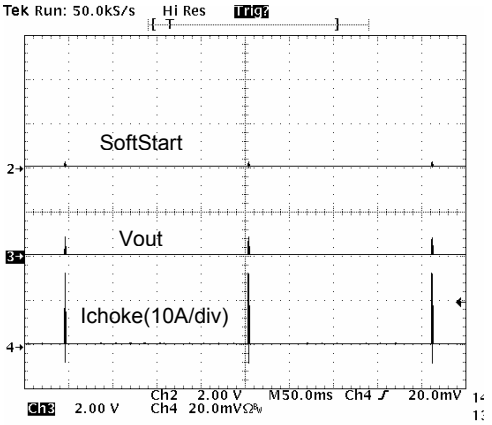
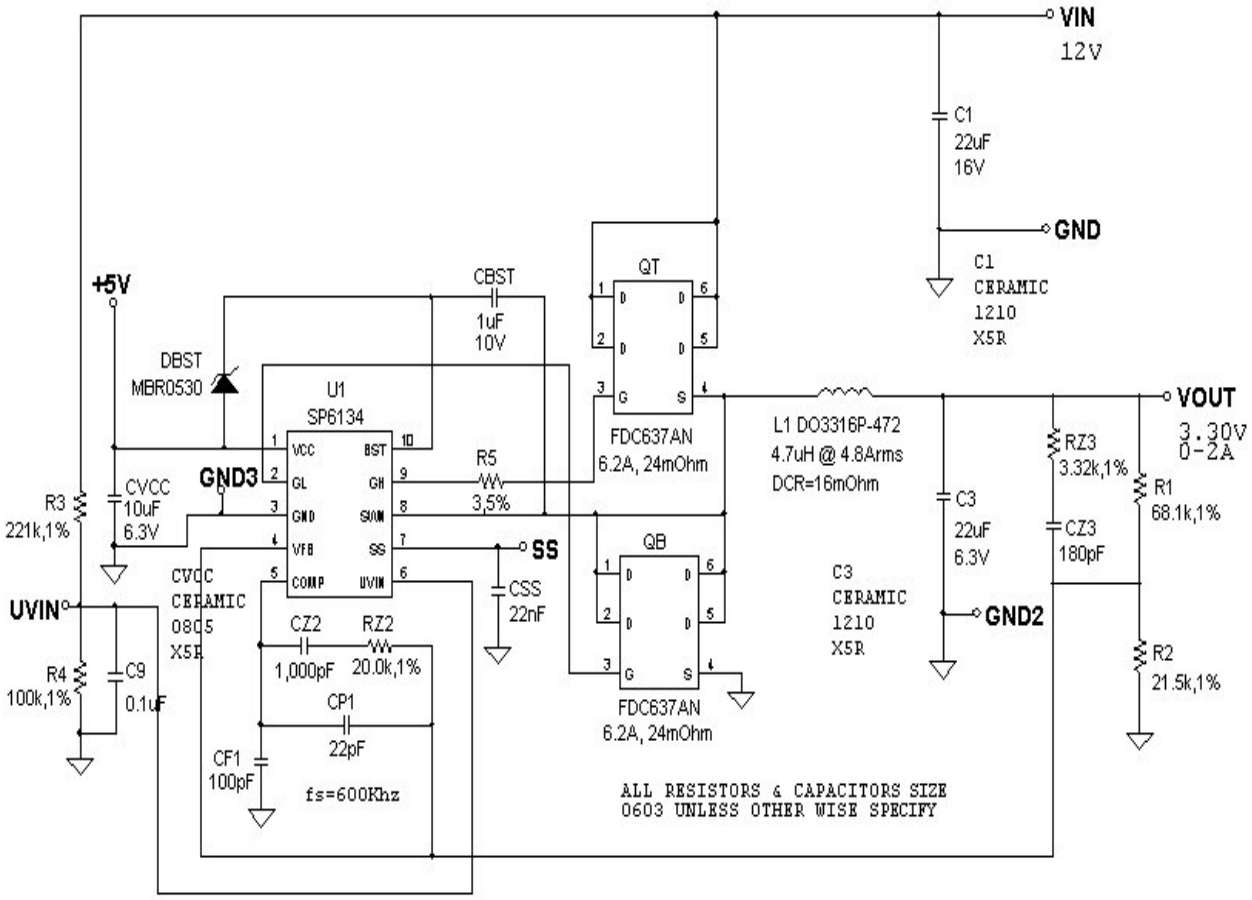


Figure 8. Output Load Short Circuit

+5V BIAS SUPPLY APPLICATION SCHEMATIC

In this application example, the SP6134CU is power by an external +5V bias supply which current consumption of 16mA Maximum. If this supply is not available than it is recommend Sipex SPX5205 Low-Noise LDO Voltage Regulator which is included on the SP6134CU Evaluation Board.



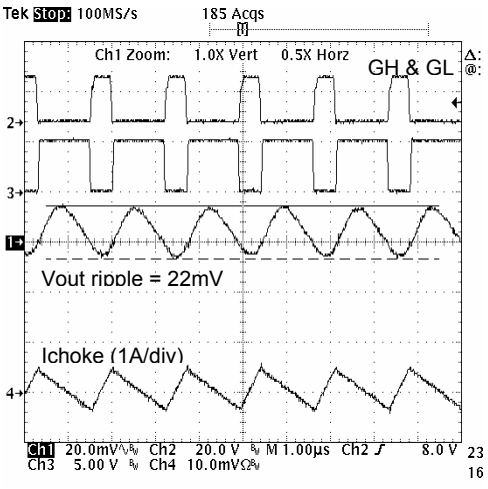


Figure 9. Output Ripple: No Load

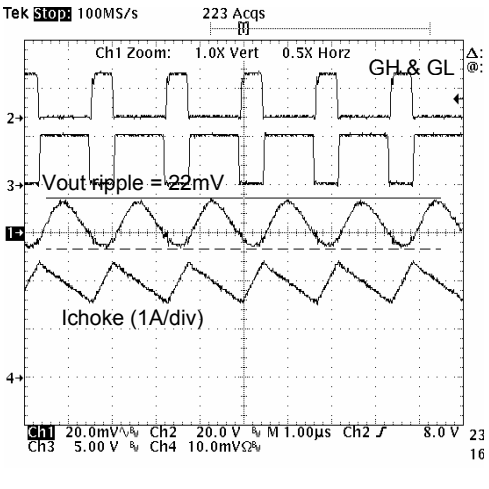


Figure 10. Output Ripple: 2A Load

DIFFERENT +5V BIAS SUPPLY SCHEMES APPLICATION SCHEMATIC

The SP6134CU VCC Bias Supply can be derived from Vin or external bias with several biasing options depending on the output power, load current, and additional biasing for the protection feature circuitry under many different application considerations. For example the transistor plus zener diode +5V bias supply could be used as shown in Figure 11. The reason is that if there is significant SP6134CU output stage current is needed to drive both the external MOSFET gate charges especially when application that require a few external parallel MOSFETs to achieve high output current. However, Figure 12 shows a very simple zener diode +5V VCC bias supply when very low external gate charge is used. In any case the SP6134CU is consuming no more than 16mA since both of the external MOSFETs gate charge is small base on its smaller footprint selections. Figure 13 shows an application circuit with SP6134CU using Sipex SPX5205 Low Drop Out (LDO) Voltage Regulator for +5V VCC Bias Supply. Note that there is an advantage of using the LDO for the +5V VCC bias since the LDO output voltage is very stable and precise allowing other to derived the voltage from it as example when additional over current clamp limit is added.

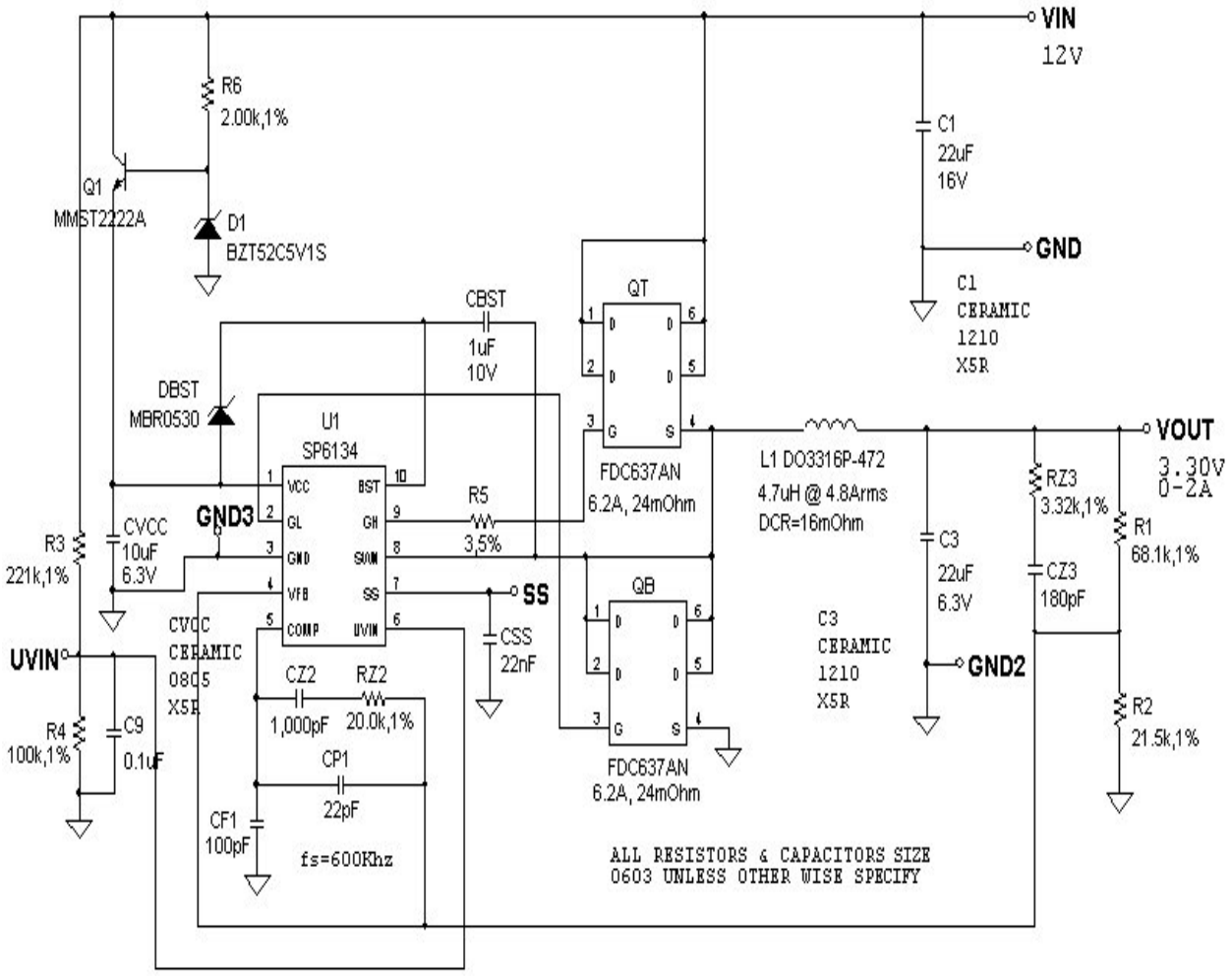


Figure 11. Transistor plus Zener Diode +5V Supply Application Schematic

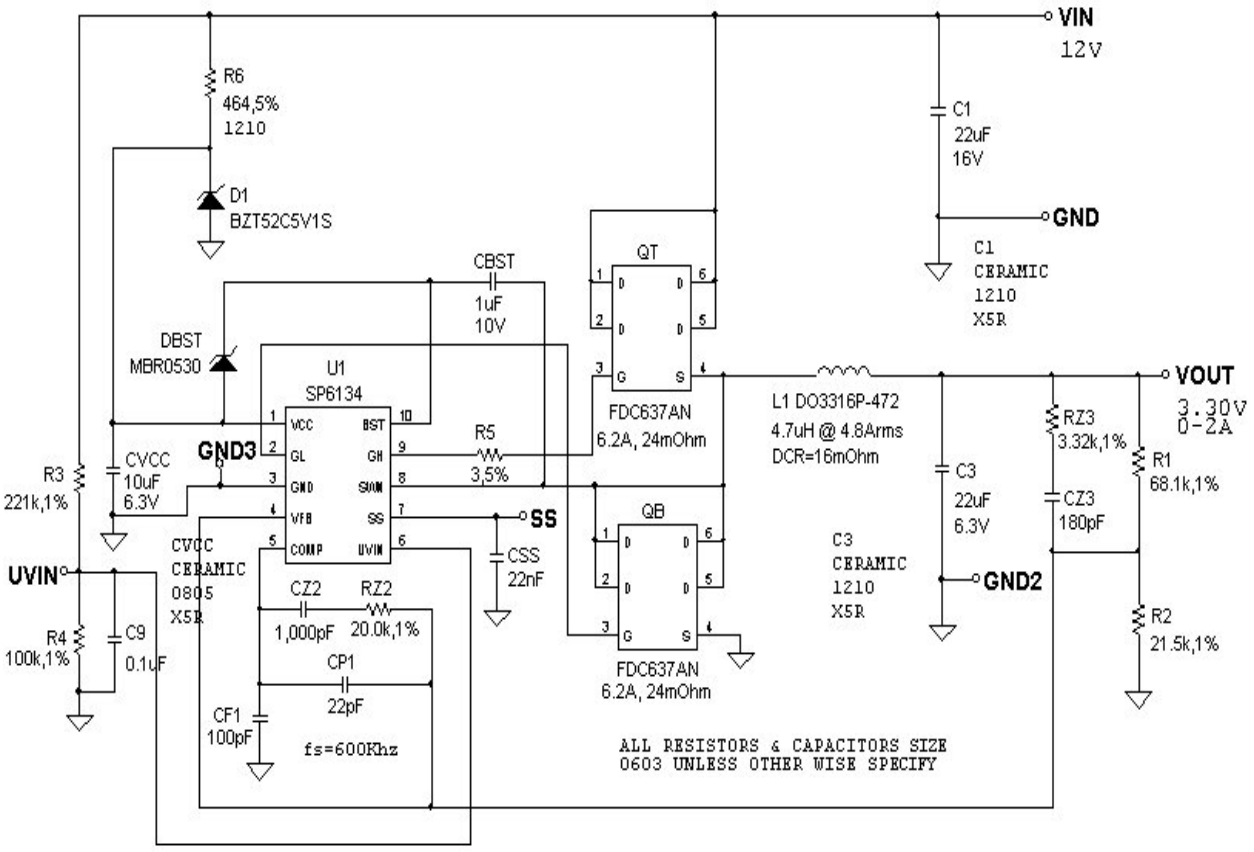


Figure 12. Very Simple Zener Diode +5V Bias Supply Application Schematic

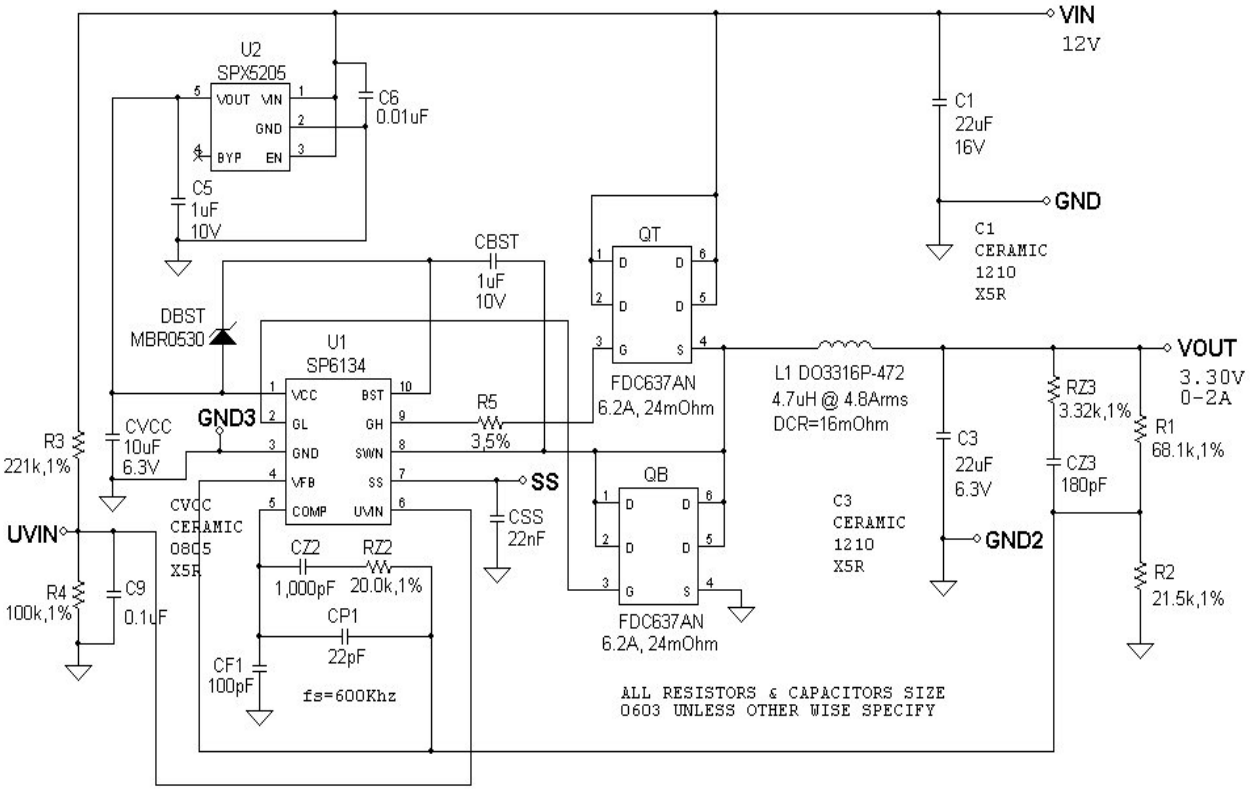


Figure 13. Simple SPX5205 +5V Low Drop Out (LDO) Bias Supply Application Schematic

SP6134CU OVER CURRENT LIMIT PROTECTION APPLICATION SCHEMATIC

The SP6134CU provides short circuit protection by sensing the output voltage at ground. However for a better and robust over current clamping protection, a comparator circuit could be used. A simplifies over current clamping circuit block diagram is shown on Figure 14. The output current clamping threshold and RC filter time constant resistors and capacitors component selections are approximately by the following equations (1) and (2).

Iout_limit ≅ (R/R')(VCC/Rdc) …… (1)

L/Rdc ≅ 2RC …… (2)

It is strongly recommend setting the over current limit threshold 130 to 150% of the maximum output load current for reliable operation under all operational condition. In Figure 15. application example, the over current limit is set at around 5A. Note that the comparator VCC is derived from the +5V Low Drop Out (LDO) Bias Supply output.

Figure 15 shows SP6134CU Evaluation Board integrates with external SPX5205 LDO for +5V VCC bias supply and output over current limit clamp comparator application circuitry. Note that the over current limit comparator referent voltage is derived from LDO output voltage. In addition, an external Power Schottky Diode DS (STPS2L25U) is added in parallel with Drain to Source of the Synchronous MOSFET in order to improve the efficiency of the converter at high output current application especially.

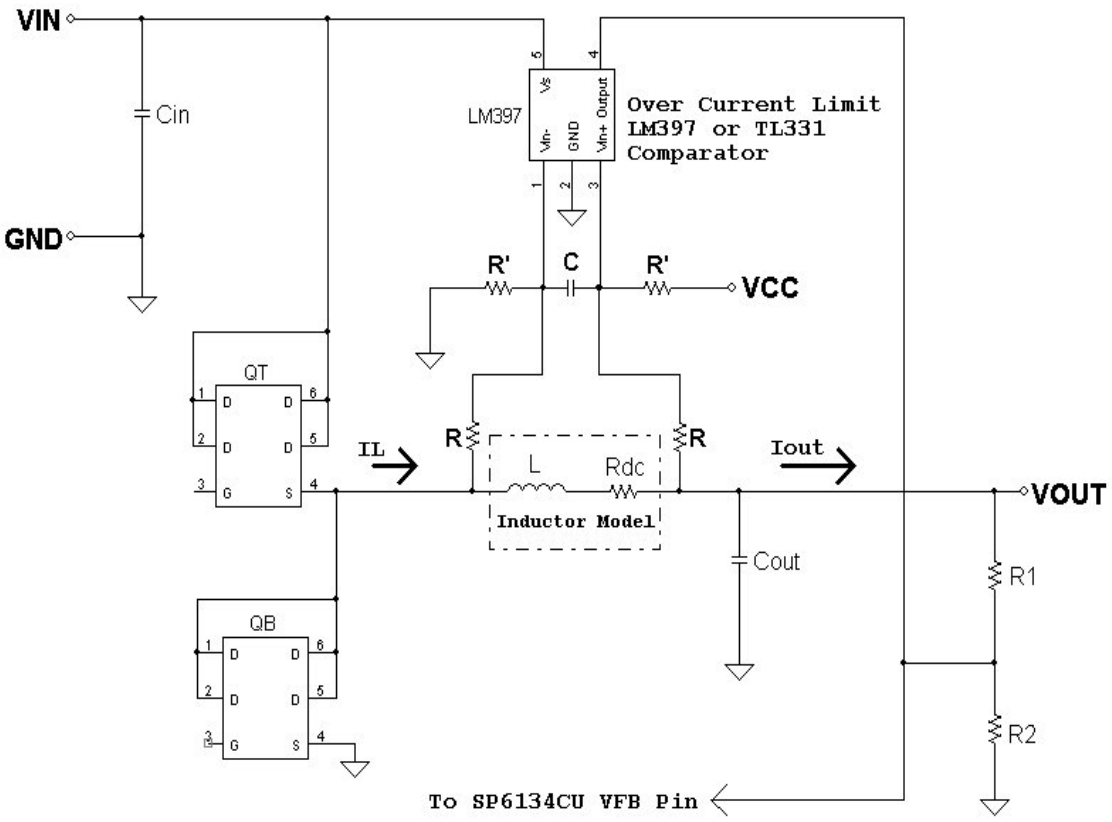


Figure 14. Simple Over Current Clamping Protection Circuit Block Diagram

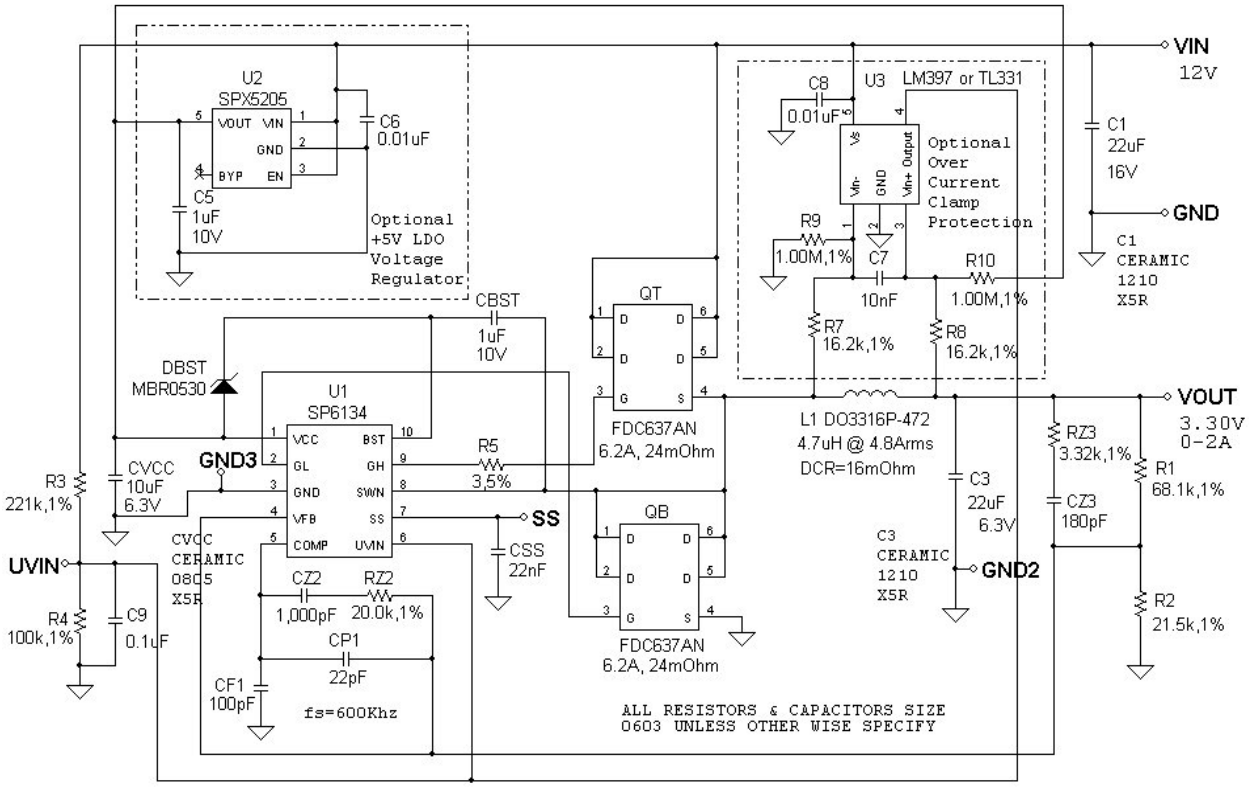


Figure 15. SP6134EB Over Current Clamping Protection Application Schematic

Table 1: SP6134EB Suggested Components and Vendor Lists

INDUCTORS - SURFACE MOUNT							
Inductance (uH)	Manufacturer/Part No.	Inductor Specification					Manufacturer Website
		Series R mOhms	Isat (A)	Size LxW(mm)	Ht.(mm)	Inductor Type	
4.7	**Coilcraft DO3316P-472**	**16.0**	**4.8**	**12.95x9.40**	**5.5**	**Unshielded Ferrite Core**	www.coilcraft.com
4.2	TDK SLF12565T-4R2N5R5	15.0	5.5	12.5x12.5	6.5	Shielded Ferrite Core	www.tdk.com
4.7	Inter-Technical SC5020-4R7M	6.7	12.0	12.6x13.6	5.1	Shielded Ferrite Core	www.inter-technical.com
5.6	TDK SLF12575T-5R6N6R3	11.6	6.3	12.5x12.5	7.5	Shielded Ferrite Core	www.tdk.com
6.8	Coilcraft DO3316P-682	19.0	4.4	12.95x9.40	5.5	Unshielded Ferrite Core	www.coilcraft.com

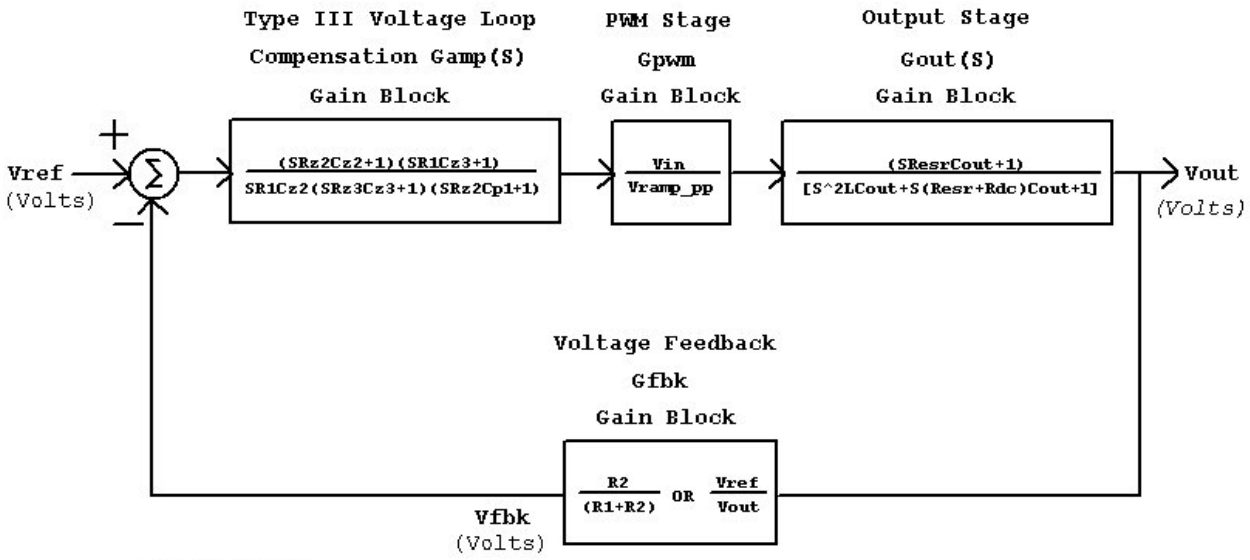
CAPACITORS - SURFACE MOUNT								
Capacitance(uF)	Manufacturer/Part No.	Capacitor Specification						Manufacturer Website
		ESR ohms (max)	Ripple Current (A) @45C	Size LxW(mm)	Ht.(mm)	Voltage (V)	Capacitor Type	
22	**TDK C3225X5R1C226M**	**0.002**	**4.00**	**3.2x2.5**	**2.0**	**16.0**	**X5R Ceramic**	www.tdk.com
22	**TDK C3225X5R0J226M**	**0.002**	**4.00**	**3.2x2.5**	**2.5**	**6.3**	**X5R Ceramic**	www.tdk.com

MOSFETS - SURFACE MOUNT								
MOSFET	Manufacturer/Part No.	MOSFET Specification						Manufacturer Website
		RDS(on) ohms (max)	ID Current (A)	Qg nC (Typ)	nC (Max)	Voltage (V)	Foot Print	
N-Channel	**Fairchild Semi FDC637AN**	**0.024**	**6.2**	**10.5**	**16.0**	**20.0**	**SuperSOT-6**	www.fairchildsemi.com
N-Channel	Vishay Siliconix Si2316DS	0.085	2.6	4.3	7.0	30.0	SOT-23	www.vishay.com

Note: Components highlighted in **bold** are those used on the SP6134 (2A MAX.) Evaluation Board.

LOOP COMPENSATION DESIGN

The open loop gain of the SP6134EB can be divided into the gain of the error amplifier **Gamp(s)**, PWM modulator **Gpwm**, buck converter output stage **Gout(s)**, and feedback resistor divider **Gfbk**. In order to crossover at the selecting frequency **fco**, the gain of the error amplifier has to compensate for the attenuation caused by the rest of the loop at this frequency. The goal of loop compensation is to manipulate the open loop frequency response such that its gain crosses over 0dB at a slope of –20dB/dec.
The open loop crossover frequency should be higher than the ESR zero of the output capacitors but less than 1/5 of the switching frequency **fs** to insure proper operation. Since the SP6134EB is designed with a Ceramic Type output capacitors, a Type III compensation circuit is required to give a phase boost of 180° in order to counteract the effects of the output **LC** under damped resonance double pole frequency.



Definitions:

Resr := Output Capacitor Equivalent Series Resitance

Rdc := Output Inductor DC Resistance

Vramp_pp := SP6134 Internal RAMP Amplitude Peak to Peak Voltage

Conditions:

Cz2 >> Cp1 and R1 >> Rz3

Output Load Resistance >> Resr and Rdc

Figure 16. SP6134EB Voltage Mode Control Loop with Loop Dynamic

The simple guidelines for positioning the poles and zeros and for calculating the component values for a type III compensation are as follows.

a. Choose **fco** = fs / 10

b. Calculate **fp_LC**
fp_LC = 1 / 2π [(L) (C)] ^ 1/2

c. Calculate **fz_ESR**
fz_ESR = 1 / 2π (Resr) (Cout)

d. Select **R1** component value such that 50kΩ ≤ R1 ≤ 100kΩ

e. Calculate **R2** base on the desired Vout
R2 = R1 / [(Vout / 0.80V) – 1]

f. Select the ratio of **Rz2 / R1** gain for the desired gain bandwidth
Rz2 = (R1) (Vramp_pp / Vin_max) (fco / fp_LC)

g. Calculate **Cz2** by placing the zero at ½ of the output filter pole frequency
Cz2 = 1 / π (Rz2) (fp_LC)

h. Calculate **Cp1** by placing the first pole at ESR zero frequency
Cp1 = 1 / 2π (Rz2) (fz_ESR)

i. Calculate **Rz3** by setting the second pole at ½ of the switching frequency and the second zero at the output filter double pole frequency
Rz3 = 2 (R1) (fp_LC) / fs

j. Calculate **Cz3** from **Rz3** component value above
Cz3 = 1 / π (Rz3) (fs)

k. Choose 100pF ≤ **Cf1** ≤ 220pF to stabilize the SP6134CU internal Error Amplify

As a particular example, consider for the following SP6134EB with a type III Voltage Loop Compensation component selections:

Vin_max = 15V
Vout = 3.30V @ 0 to 2A load
Select L = 4.7uH => yield ≈ 45% of maximum 2A output current ripple.
Select Cout = 22uF Ceramic capacitors (Resr ≈ 2mΩ)
fs = 600khz SP6134CU internal Oscillator Frequency
Vramp_pp = 1.0V SP6134CU internal Ramp Peak to Peak Amplitude

Step by step design procedures:

a. **fco** = 600khz / 10 = 60khz

b. **fp_LC** = 1 / 2π [(4.7uH)(22uF)]^1/2 ≅ 16khz

c. **fz_ESR** = 1 / 2π (2mΩ)(22uF) ≈ 3.6Mhz

d. **R1** = 68.1kΩ, 1%

e. **R2** = 68.1kΩ / [(3.30V / 0.80V) – 1] ≅ 21.5kΩ, 1%

f. **Rz2** = 68.1kΩ (1.0V / 15V) (60khz / 16khz) ≈ 20.0kΩ, 1%

g. **Cz2** = 1 / π (20.0kΩ) (16khz) ≈ 1,000pF, COG

h. **Cp1** = 1 / 2π (20.0kΩ) (3.6Mhz) ≈ 2pF => **Cp1** = 22pF, COG for noise filtering

i. **Rz3** = 2 (68.1kΩ) (16khz) / 600khz ≈ 3.32kΩ, 1%

j. **Cz3** = 1 / π (3.32kΩ) (600khz) ≅ 180pF, COG

k. **Cf1** = 100pF to stabilize SP6134CU internal Error Amplify

PC LAYOUT DRAWINGS

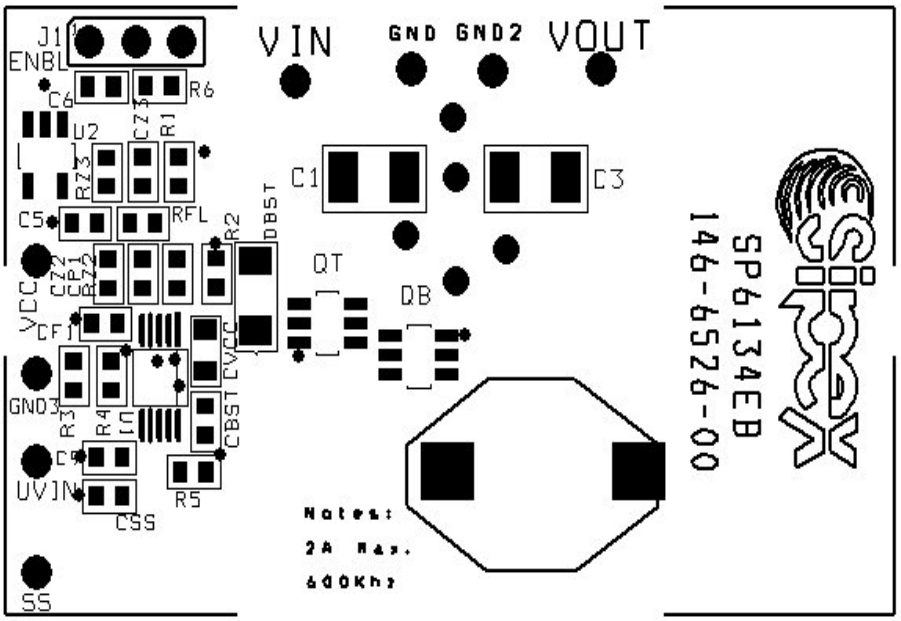


Figure 17. SP6134EB Component Placement

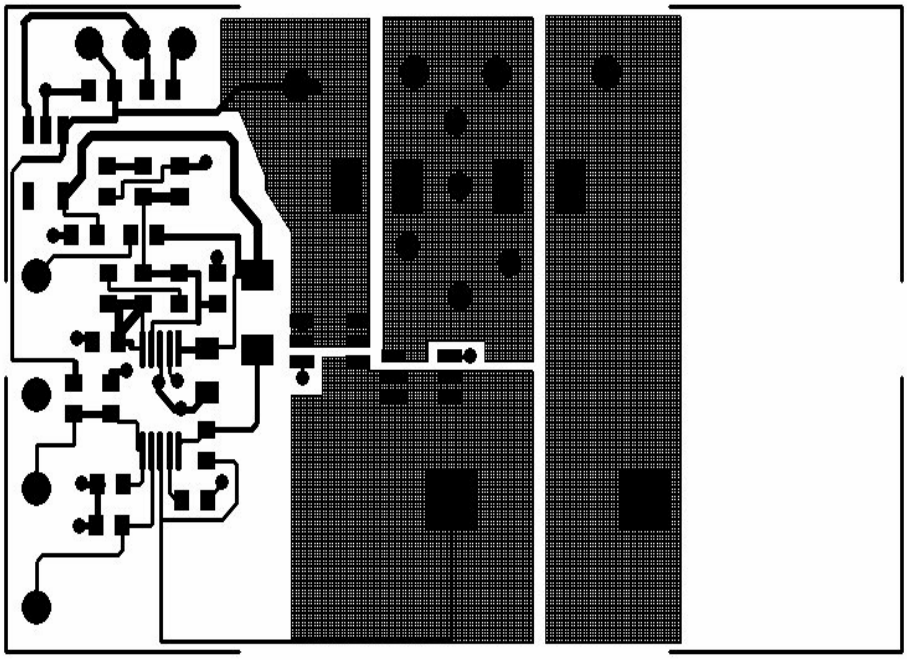


Figure 18. SP6134EB PC Layout Top Side

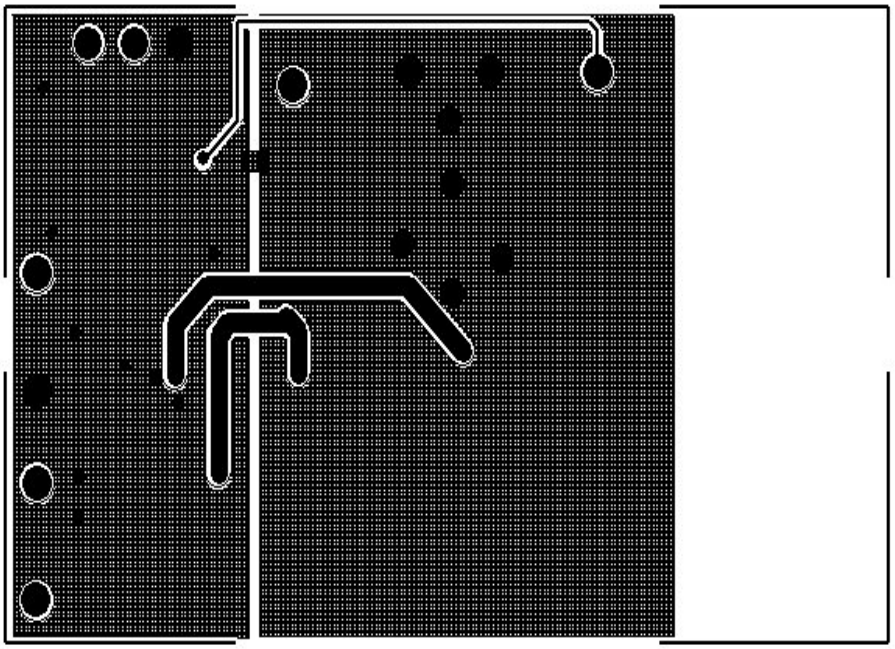


Figure 19. SP6134EB PC Layout Bottom Side

Table 3: SP6134EB List of Materials

SP6134 (2A MAX.) Evaluation Board List of Materials						
Line No.	Ref. Des.	Qty.	Manuf.	Manuf. Part Number	Layout Size	Component
1	PCB	1	Sipex	146-6526-02	1.75"X2.75"	SP6134EB
2	U1	1	Sipex	SP6134CU	MSOP-10	2-15A Any-FET Buck Ctrl
3	U2	1	Sipex	SPX5205M5-5.0	SOT-23-5	150mA LDO Voltage Reg
4	QT, QB	2	Fairchild Semi	FDC637AN	SOT-6	NFET
5	DBST	1	ON-Semi	MBR0530	SOD-123	0.5A Schottky
6	L1	1	Coilcraft	DO3316P-472	12.95X9.4mm	4.70uH Coil 4.8Arms 16mohm
7	C3	1	TDK	C3225X5R0J226M	1210	22uF Ceramic X5R 6.3V
8	C1	1	TDK	C3225X5R1C226M	1210	22uF Ceramic X5R 16V
9	CVCC	1	TDK	C2012X5R0J106M	0805	10uF Ceramic X5R 6.3V
10	C6	1	TDK	C1608X5R1C103K	0603	0.01uF Ceramic X5R 16V
11	C9	1	TDK	C1608X5R1C104K	0603	0.1uF Ceramic X5R 16V
12	C5, CBST	2	TDK	C1608X5R1A105K	0603	1.0uF Ceramic X5R 10V
13	CSS	1	TDK	C1608X7R1H223K	0603	22,000pF Ceramic X7R 50V
14	CZ2	1	TDK	C1608COG1H102J	0603	1,000pF Ceramic X7R 50V
15	CP1	1	TDK	C1608COG1H220J	0603	22pF Ceramic COG 50V
16	CF1	1	TDK	C1608COG1H101J	0603	100pF Ceramic COG 50V
17	CZ3	1	TDK	C1608COG1H181J	0603	180pF Ceramic COG 50V
18	RZ2	1	Panasonic	ERJ-3EKF2002V	0603	20.0K Ohm Thick Film Res 1%
19	R2	1	Panasonic	ERJ-3EKF2152V	0603	21.5K Ohm Thick Film Res 1%
20	RZ3	1	Panasonic	ERJ-3EKF3321V	0603	3.32K Ohm Thick Film Res 1%
21	R1	1	Panasonic	ERJ-3EKF6812V	0603	68.1K Ohm Thick Film Res 1%
22	R3	1	Panasonic	ERJ-3EKF2213V	0603	221K Ohm Thick Film Res 1%
23	R4, R6	2	Panasonic	ERJ-3EKF1003V	0603	100K Ohm Thick Film Res 1%
24	R5, RFL	1	Yageo America	9C06031A3R0JLHFT	0603	3.0 Ohm Thick Film Res 5%
25	J1	1	Sullins	PTC36SAAN	.32x.12	36-Pin (3x12) Header
26	(J1)	1	Sullins	STC02SYAN	.2x.1	Shunt
27	VIN, VOUT, VCC, GND, GND2, GND3	6	Vector Electronic	K24C/M	.042 Dia	Test Point Post
28	UVIN, SS	2	Mill-Max	3137-3002-10-0080	.042 Dia	Test Point Female Pin

ORDERING INFORMATION

Model	Temperature Range	Package Type
SP6134EB	0°C to +70°C	SP6134 Evaluation Board
SP6134CU	0°C to +70°C	10-pin MSOP

Design Solution 12

SP6134 12V Boost to 28V output at 400mA

Date: Jan.12, 2006

Designed by: Brian Kennedy (bkennedy@sipex.com)

Part Number: SP6134EU

Application Description: Provide high output voltage from 12Vin

Electrical Requirements:

Input Voltage	9.0V – 20V
Output Voltage	28V
Output Current	400mA

Circuit Description:

This circuit has been designed to provide 28V output at 400mA. High output voltage and low cost dictated the choice of the controller and external components. In order to reduce cost, a non-synchronous boost regulator topology was chosen. The SP6134 is a synchronous buck regulator that is being used instead as a boost DC/DC controller to drive an N-channel MOSFET for charging the inductor in the discontinuous mode. As a non-synchronous boost, a second MOSFET driver is not needed and, instead, a small inexpensive MBR0540 Schottky diode is used in the discharge phase to charge the output capacitor. High switching frequency (600 kHz) allows the use of a small 3.3uH inductor.

This report includes the application schematic complete with component part numbers and figures 1-11 illustrating electrical performance of the design.

Design Solution 12

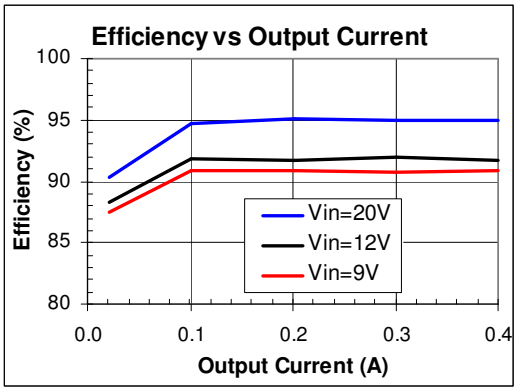


Figure 1. Efficiency Graph

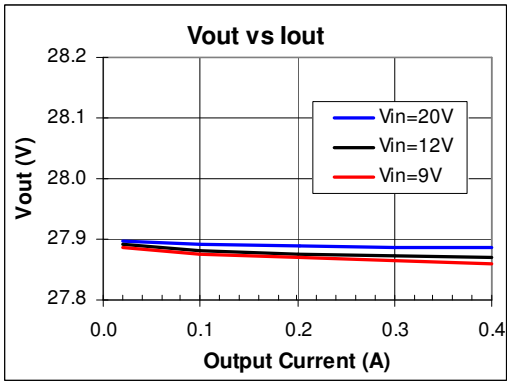


Figure 2. Output regulation Graph

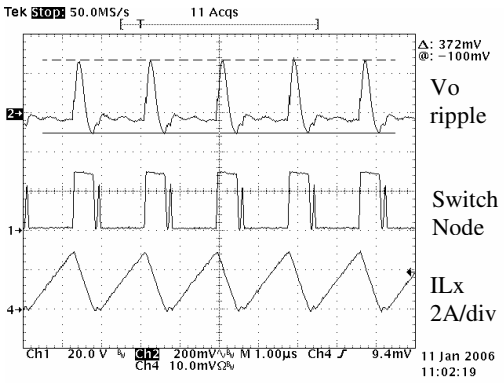


Figure 3. Switching behaviors

Vin=9V, Vo=28V, 400mA Load

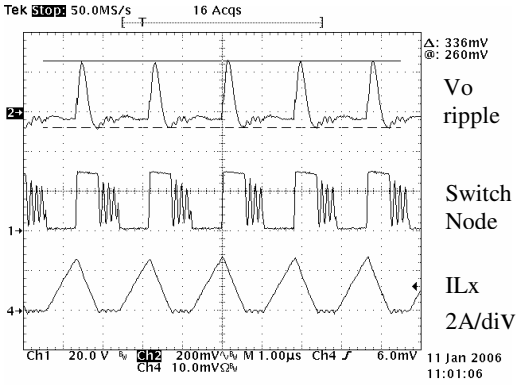


Figure 4. Switching behaviors

Vin=12V, Vo=28V, 400mA

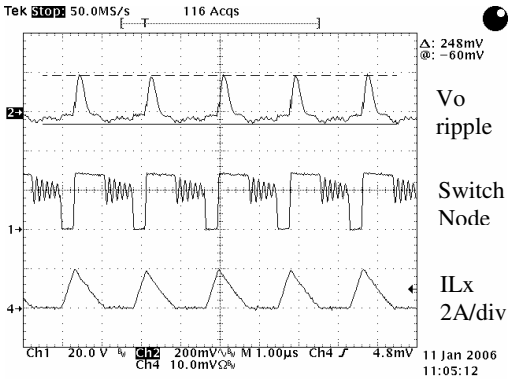


Figure 5. Switching behaviors

Vin=20V, Vo=28V, 400mA Load

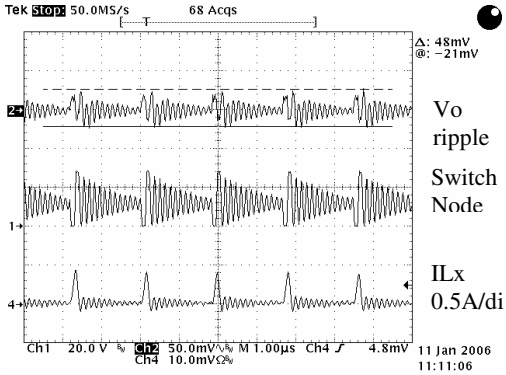


Figure 6. Switching behaviors

Vin=12V, Vo=28V, 20mA Load

Design Solution 12

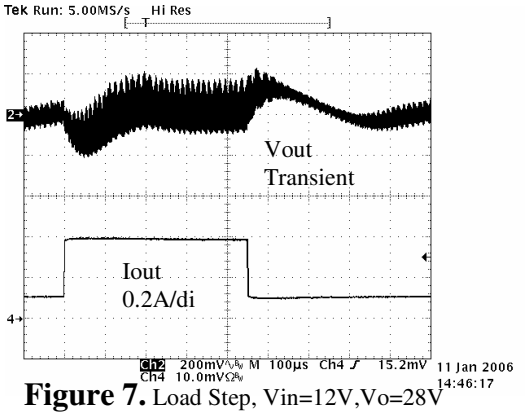


Figure 7. Load Step, Vin=12V,Vo=28V
Iout= 100-400mA @ 1KHz

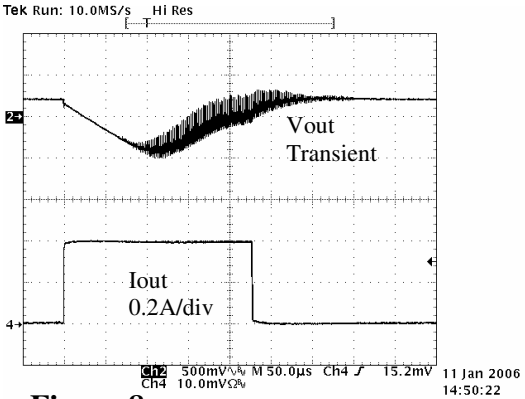


Figure 8. Load Step, Vin=12V,Vo=28V
Iout= 0-400mA @ 1KHz

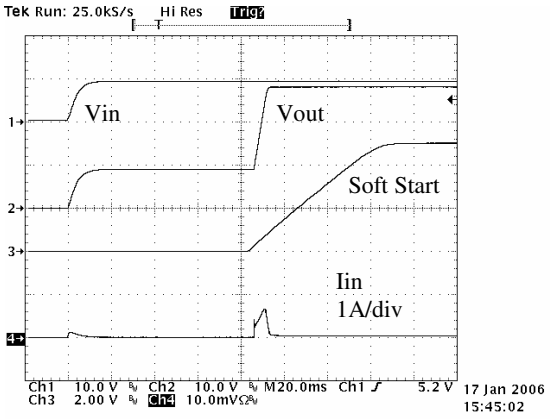


Figure 9. Start up
Vin=9V, Iout=10mA

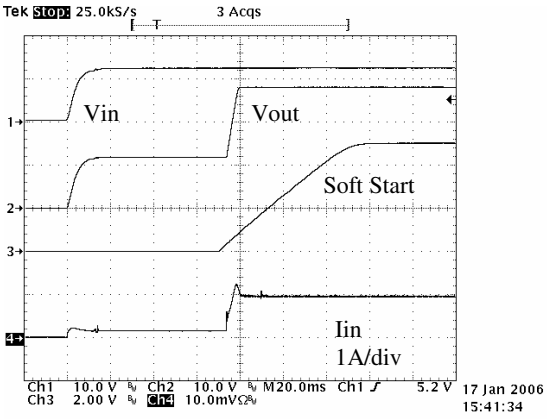


Figure 10. Start up
Vin=12V, Iout=400mA

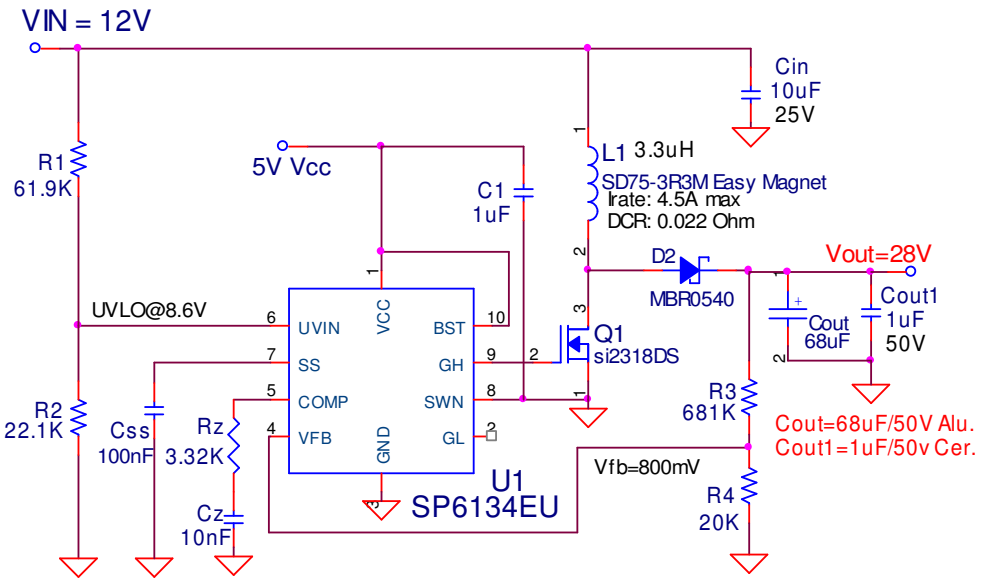


Figure 11. Application Schematic

Design Solution 15

Using the SP6134 for Powering High Power LEDs with High Input Voltage and Load Dump Protection

Designed by: Matthew Szaniawski (mszaniawski@sipex.com)

Part Number: SP6134

Application Description: Powering 750mA LED constant current

Electrical Requirements:

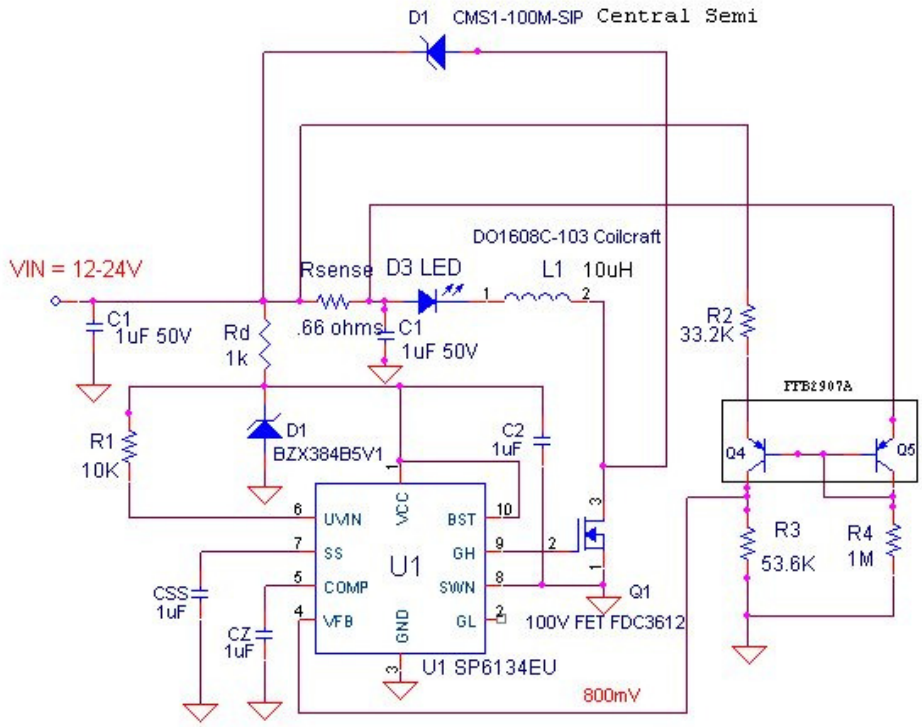
Input Voltage	8.5V - 50V
Output Voltage	V_f of LED
Output Current	750mA

Circuit Description:

This circuit has been designed to provide a constant current source for an LED using high side current sensing. The high side current sensing allows this buck topology to deliver a constant current through the LED over a wide input voltage range. A single white LED was used in testing. The high side current sensing is accomplished by using transistors Q4 and Q5. Ideally transistor Q4 and Q5 should be in the same package so that the dies are matched. By knowing that the base voltages of transistors Q4 and Q5 are at the same potential and the transistor diode voltage drops are closely matched, then the voltage across R2 and R_{sense} will be approximately the same. Below are the guideline formulae to determine R2, R3 and R_{sense}.

Step 1: Choose the sense voltage (V_{sense}) ; this voltage should be between 300mV and 600mV.
Step 2: Choose R2 between 30K ohms and 50K ohms
Step 3: $R3 = \frac{(V_{fb} \cdot R2)}{V_{sense}}$ V_{fb} for SP6134 is .8V
Step 4: $R_{sesnse} = \frac{V_{sense}}{I_{load}}$

This report includes application schematic, figures 2-5 illustrating electrical performance of the design, and a complete Bill of materials.



About Rd
For operation between 12V and 24V Rd needs to be about 1K.
Two 2K resistors were used in parallel.

Figure 1. Schematic

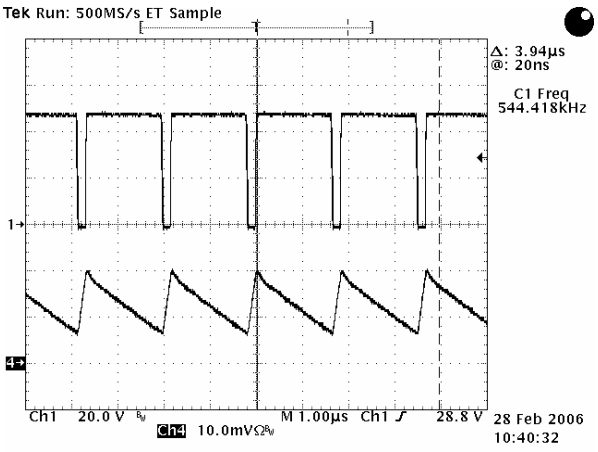


Figure 2. I_{out} 750mA V_{in} 45Vin.
Channel 1 Switch node Channel 4 500mA per division

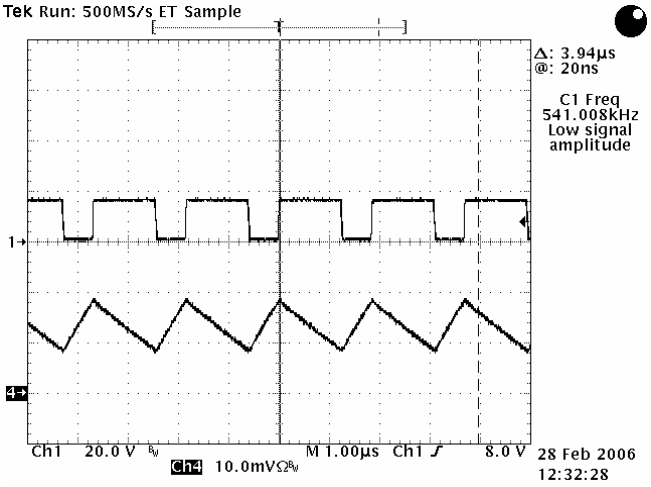


Figure 3. I_{out} 750mA V_{in} 16V
Channel 1 Switch node Channel 4 current set to 500mA per division

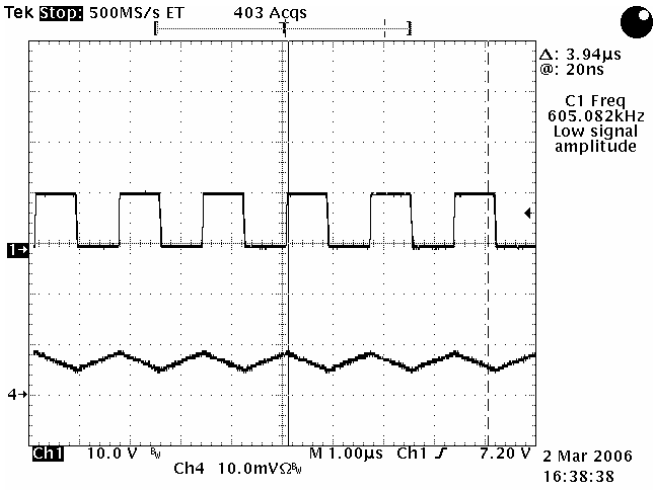


Figure 4. I_{out} 750mA V_{in} 9V
Channel 1 Switch node Channel 4 current set to 1A per Division

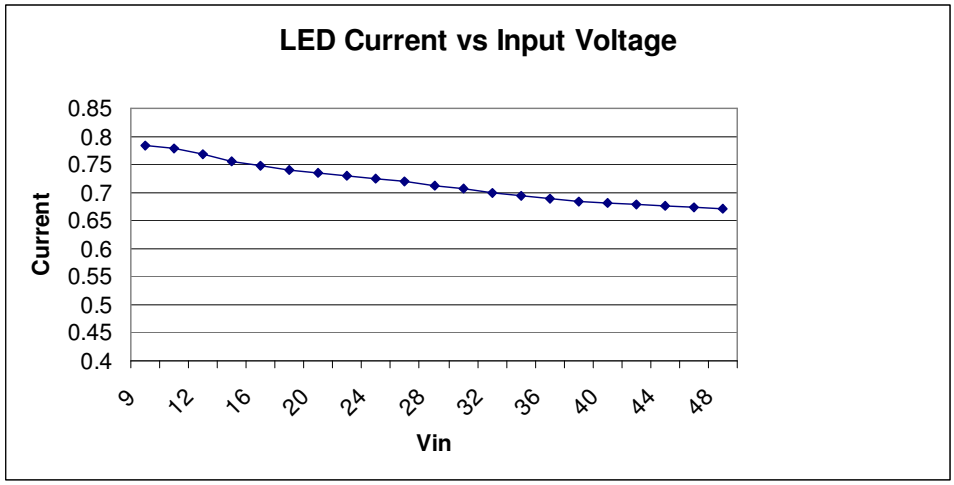


Figure 5. Load Current vs. Input voltage

SP6134 Evaluation Board Rev. 00 List of Materials							3/3/2006
Line No.	Ref. Des.	Qty.	Manuf.	Manuf. Part Number	Layout Size	Component	Vendor Phone Number
2	U1	1	Sipex	SP6134EU	MSOP-10	2-NFET Buck Controller	978-667-7800
3	Dz	1	Vishay Semi	BZX384B5V1	SOD-323	5.1V Zener Diode	800-344-4539
4	L1	1	Coilcraft	DO1608C-103	6.8X6.8mm	10uH Inductor	
5	Cin1 Cin2 Css CZ C2	5	Murata	GRM31MR71H105KA88	1206	1uF Ceramic X5R 50V	
6	Q4 Q5	1	Fairchild	FFB2907A	SC70-6	Dual PNP transistor 60V	
7	Q1	1	Fairchild	FDC3612		100V N-channel FET	
8	R2	1	Panasonic	ERJ-3EKF3322V	0603	33.2K Ohm Thick Film Res 1%	800-344-4539
9	R3	1	Panasonic	ERJ-3EKF5362V	0603	53.6K Ohm Thick Film Res 1%	800-344-4539
10	R4	1	Panasonic	ERJ-3EKF1005V	0603	1MOhm Thick Film Res 1%	800-344-4539
11	R1	1	Panasonic	ERJ-3EKF1002V	0603	10K Ohm Thick Film Res 1%	800-344-4539
12	Rd	2	Panasonic	ERJ-8EWF100V	1206	1K Ohm Thick Film Res 1%	800-344-4539
13	Rsense	1	Panasonic	ERJ-8GEYJ2R0	1206	2 ohm Thick Film Res 1%	800-344-4539
	Rsense	1	Panasonic	ERJ-8GEYJ1R0	1206	1 ohm Thick Film Res 1%	800-344-4539
14	D1	1	Central Semi	CMS1-100-SIP	SM-8	Schottcky Diode 2A 100V	

Figure 6. BOM

Design Solution # 41

Reducing Parasitic Oscillations at the Switching Node

Designed by: Shahin Maloyan

Part Numbers: SP6133/6, SP6134, SP6132

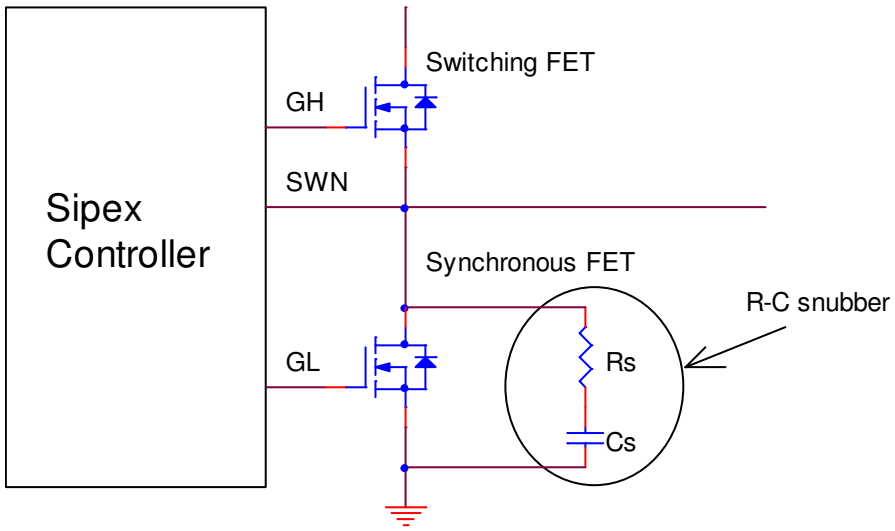
Application Description: Any noise-sensitive application where synchronous buck converters are used.

Electrical Requirements:

Input Voltage	5V – 24V
Output Current	higher than 10A

Circuit Description:
There usually exist high-frequency parasitic oscillations at the node between the switching FET and synchronous FET (SWN). It is not uncommon to see SWN peak voltage as high as 2.5xV_{IN}. The oscillations are a product of parasitic inductance in the DC-Loop of the Printed Circuit Board (PCB) and snappy reverse-recovery of synchronous FET's body diode. A dissipative R-C snubber across the synchronous FET dampens the oscillation quickly and reduces the peak voltage.

This report includes the application schematic and a procedure for determining the R-C snubber components Resistors and Capacitors.



Application Schematic

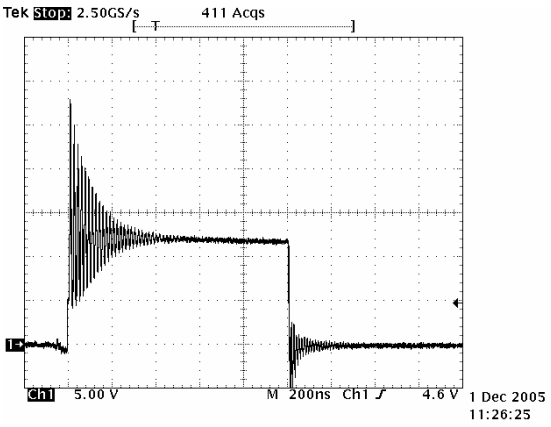


Figure 1: SWN without R-C snubber

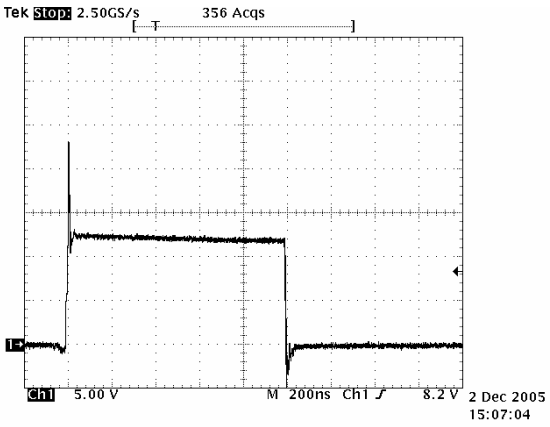


Figure 2: SWN with R-C snubber

Comments:

Oscillations at the switching node (SWN) are a product of parasitic inductance in the PCB's DC-Loop and snappy recovery of Synchronous FET's body diode. The parasitic inductance stores energy when the switching FET conducts. Following the recovery of the synchronous FET's body diode, this energy is transferred back and forth between the parasitic inductance and output capacitance of the synchronous FET (Coss). The oscillations stress the SWN node of the controller plus the synchronous FET and are a potential source of Electro Magnetic Interference.

Procedure for selecting snubber components

Let Cs = 4 x Coss

Where:

Cs is the snubber capacitor
Coss is the output capacitance of the synchronous FET. Determine the value corresponding to V_{IN} of the converter from the Coss graph in the FET datasheet.

As a rule of thumb use a 0.25W Resistor Rs in the 2 to 3Ω range. Place the snubber components as close to the FET as possible.

Design Solution # 48

SP6134 5.0V input to 1.2V output @ 2.5A

Designed by: Brian Kennedy

Part Number: SP6134ER

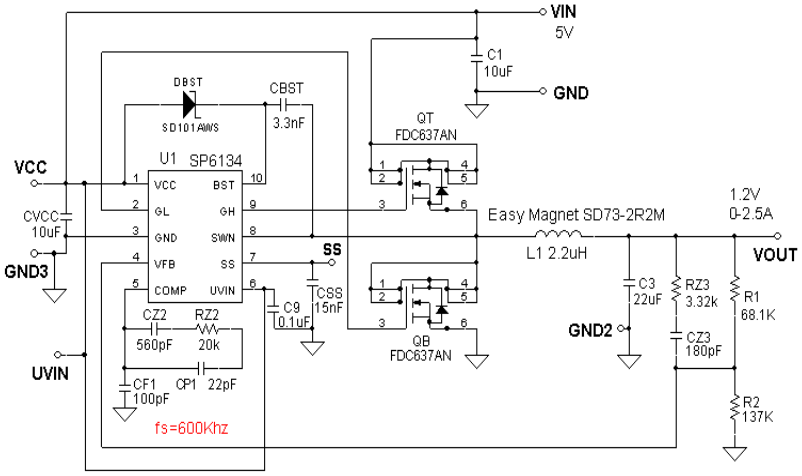
Application Description: 5.0V converted to 1.2V at 2.5A output

Electrical Requirements:

Input Voltage	5.0V
Output Voltage	1.2V
Output Current	2.5A

Circuit Description:

This application has been designed for a 1.2V output that requires 2.5A output current in a small solution size with low output ripple. The SP6134 buck regulator uses PWM control with a 600 kHz switching frequency to provide small solution size with very good 2.5A load efficiency. All the external components have been optimized for an output current of 2.5A which includes a small SOT23-6 pin NMOS switch, a low profile 3.5mm ht 2.2uH inductor, and 0805 size 10uF and 22uF capacitors. The circuit has been designed with a low ESR 22uF ceramic output and type III compensation for fast transient response and low 10mVp output ripple. This report includes figure 7 application schematic complete with component part numbers and figures 1-6 illustrating electrical performance of the design. For further information on implementing Type III loop configuration, see this application note on the Sipex website:
http://www.sipex.com/files/ApplicationNotes/Type%20III%20Loop%20Compensation%20Oct12-06.pdf



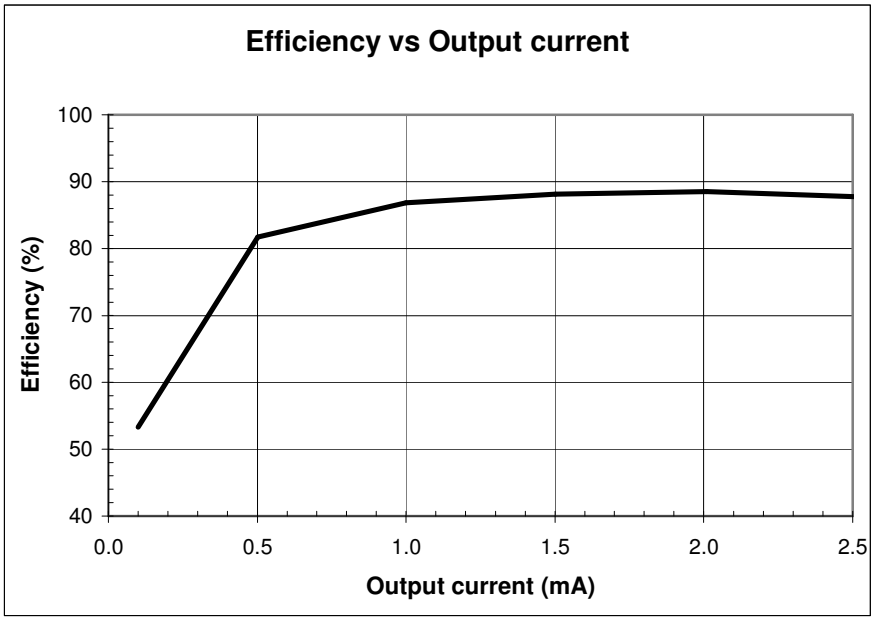
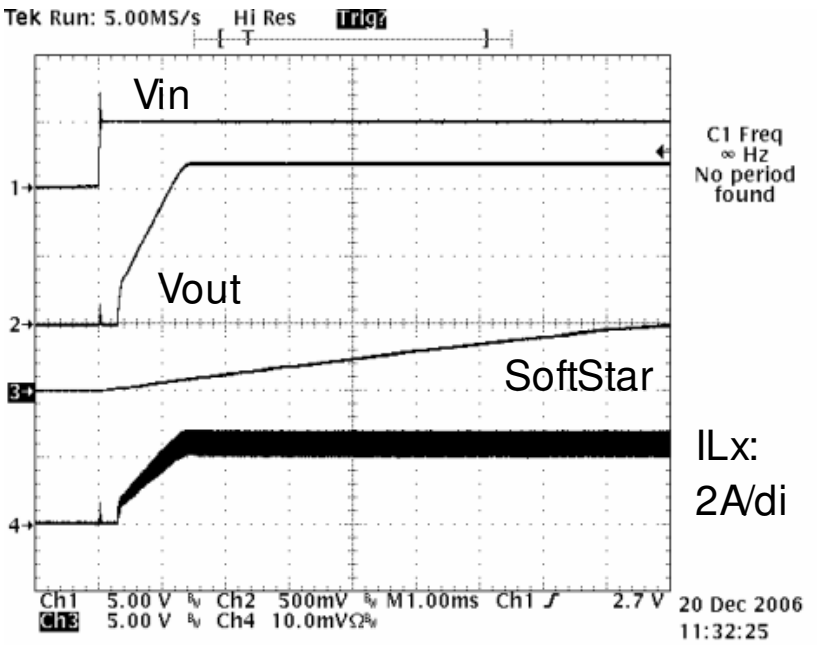
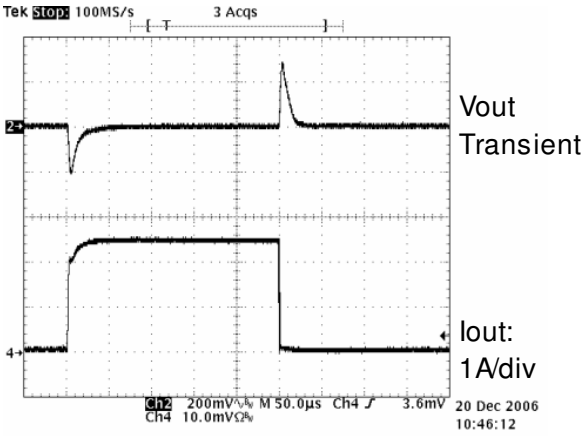


Figure 1. Efficiency Graph



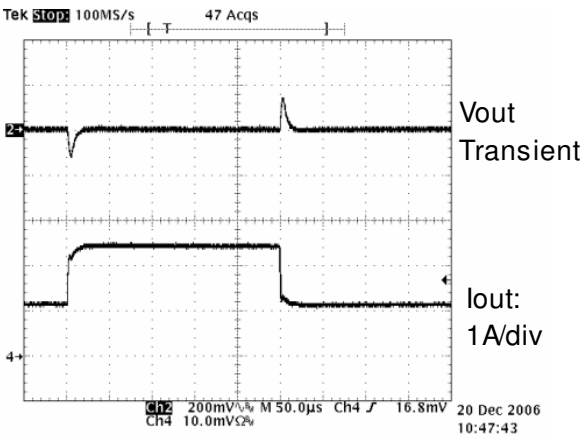
Start up, Iout=2.5A

Figure 2. Start-up 2.5A output current



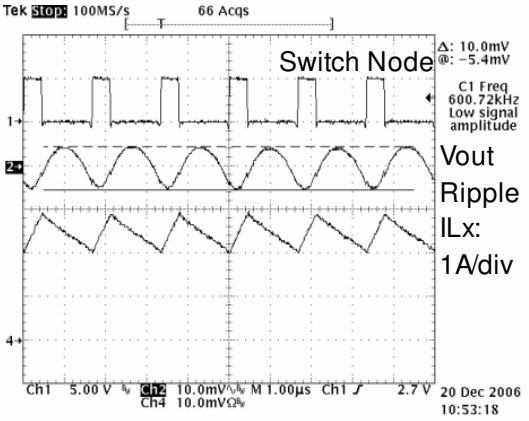
Iout Load Step 0A to 2.5A

Figure 3. Transient Response
0A to 2.5A



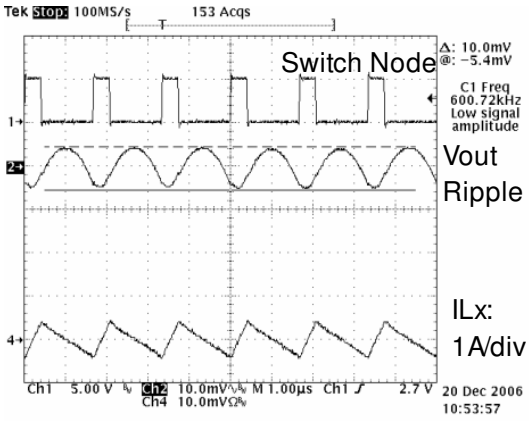
Iout Load Step 1.25A to 2.5A

Figure 4. Transient Response
1.25A to 2.5A



Switching behavior, Iout=2.5A

Figure 5. 2.5A Output Ripple



Switching behavior, No Load

Figure 6. No Load Output Ripple

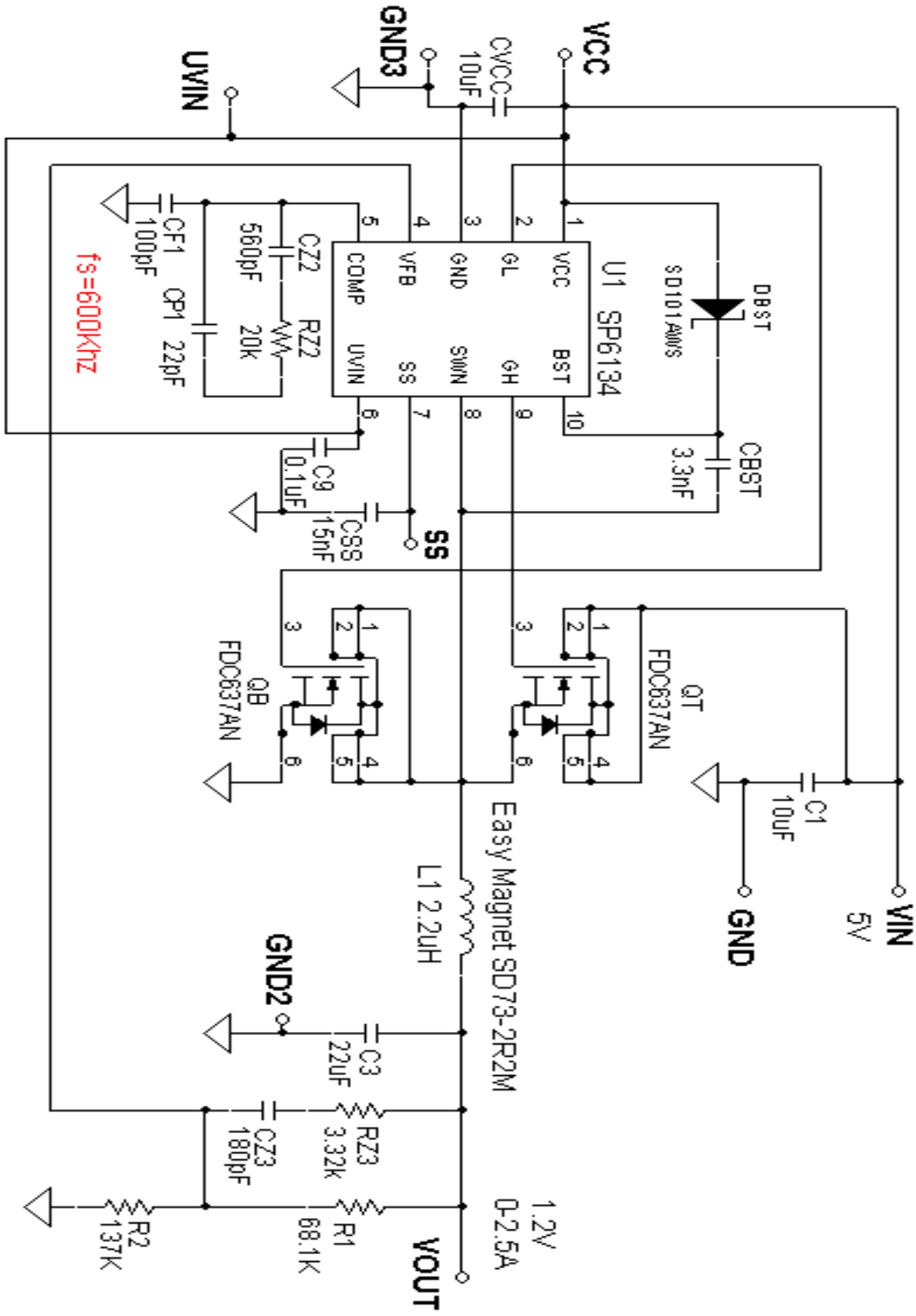


Figure 7. Application Schematic

For further assistance:

Email:	Sipexsupport@sipex.com
WWW Support page:	http://www.sipex.com/content.aspx?p=support
Live Technical Chat:	http://www.geolink-group.com/sipex/
Sipex Application Notes:	http://www.sipex.com/applicationNotes.aspx
Type III loop Compensation Application Note:	http://www.sipex.com/files/ApplicationNotes/Type%20III%20Loop%20Compensation%20Oct12-06.pdf
Type III loop Compensation Calculator:	http://www.sipex.com/files/ApplicationNotes/TypeIIICalculator.xls

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