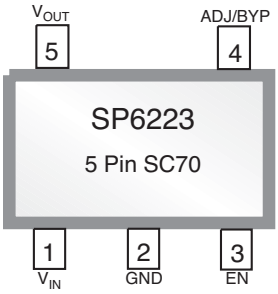
SP6222/SP6223

50mA and 150mA CMOS Linear Regulators

FEATURES

- Very low Dropout Voltage: 200mV typ (150mA load)
- High Output Setpoint Accuracy of 1% (typ)
- Very low Input Voltages Down to 1.6V
- Power-saving Shutdown Mode of 150nA (typ)
- Fast Turn-on (90μs) and Turn-off (90μs)
- Extremely low Quiescent Current of 14μA (typ)
- Very Tight Line regulation, 0.2%/V
- Load Regulation 0.125 mV/mA
- Thermal Shutdown Protection
- Low Noise Output, 100μVRMS With 10nF Bypass
- Fixed or Adjustable Output Versions Available
- Available in RoHS Compliant, Lead Free Packages: SC70 and SOT23



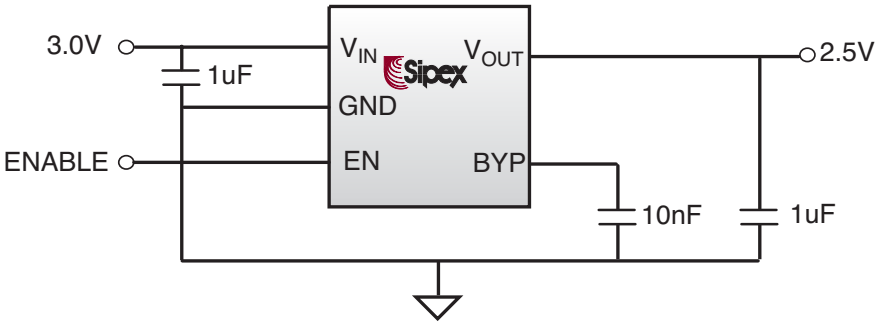
APPLICATIONS

- Cellular Telephones
- Laptop, Notebooks and Palmtop Computers
- Battery-Powered Equipment
- Consumer/ Personal Electronics
- SMPS Post-Regulator
- DC-to-DC Modules
- Medical Devices
- Data Cable
- Pagers

DESCRIPTION

The SP6222 and SP6223 are CMOS LDOs designed to meet a broad range of applications that require accuracy, speed and ease of use. These LDOs offer extremely low quiescent current which only increases slightly under load, thus providing advantages in ground current performance over bipolar LDOs. The LDOs handle an extremely wide load range and guarantee stability with a 1μF ceramic output capacitor. They have excellent low frequency PSRR, not found in other CMOS LDOs and thus offer exceptional Line Regulation. High frequency PSRR is 55dB (typical) at 1kHz. Load Regulation is excellent and temperature stability is comparable to bipolar LDOs. An enable feature is provided on all versions. The SP6222/6223 is available in fixed and adjustable output voltage versions in industry standard SC70 and SOT23 packages.

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Supply Input Voltage (V_{IN}) ..... -2V to 6V
Output Voltage (V_{OUT}) ..... -0.6V to V_{IN}+1V
Enable Input Voltage (V_{EN}) ..... -2V to 7V
Power Dissipation (P_D) ..... Internally Limited, Note 1

Storage Temperature.....-65°C to +150°C
Junction Temperature (T_J).....-40°C to +125°C
Lead Temperature (soldering 5s).....300°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified: V_{IN} = V_{OUT} + 0.3V to 4.5V, C_{OUT} = 1µF ceramic, C_{IN} = 1µF ceramic, I_{OUT} =100µA, T_A = 25°C.
Bold values apply over the full operating temperature range (-40°C to 125°C).

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Operating Input Voltage Range Note 2	**1.6**		**4.5**	V	I_{OUT} = 50mA (SP6222) I_{OUT} = 150mA (SP6223)
Output Voltage Accuracy		1	**3**	%	
Fixed Output Voltage (3.0V version)	**2.91**	3.0	**3.09**	V	
Fixed Output Voltage (2.5V version)	**2.425**	2.500	**2.575**	V	
Reference Voltage	**0.873**	0.9	**0.927**	V	Adjustable version only
Line Regulation		0.05	0.2	%/V	ΔV_{OUT} (V_{IN} below 4.5V)
Load Regulation		0.125	0.225	mV/mA	I_{OUT} = 0.1mA to 50mA (SP6222) I_{OUT} = 0.1mA to 150mA (SP6223)
Thermal Regulation		0.005		%/ºC	I_{OUT} = 50mA (SP6222)
Dropout Voltage (DOV), Note 3		60 200	**100** **300**	mV	I_{OUT} = 50mA (SP6222) I_{OUT} = 150mA (SP6223)
Ground Pin Current		14	25	µA	I_{OUT} = 0.1mA

Note 1. The maximum allowable power dissipation at any T_A (ambient temperature) is $P_{D\,(MAX)} = (T_{J\,(MAX)} - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown. The θ_{JA} of the SP6222/23 (SC-70-5) is 330°C/W mounted on a PC board with minimum copper area (see "Thermal Considerations" section for further details).

Note 2. Minimum V_{IN} must meet 2 conditions: V_{IN} >1.6V and $V_{IN} \geq \{V_{OUT} + DOV\}$

Note 3. Dropout Voltage DOV is defined as the input to output differential at which the output voltage drops 2% below its nominal value measured at 1V differential. The DOV specification is not applicable to output voltages less than 2.7V.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified: V_{IN} = V_{OUT} + 0.3V to 4.5V, C_{OUT} = 1µF ceramic, C_{IN} = 1µF ceramic, I_{OUT} =100µA, T_A = 25°C.
Bold values apply over the full operating temperature range (-40°C to 125°C).

PARAMETER	MIN	TYP	MAX	Units	CONDITIONS
Shutdown Supply Current @ 25ºC		0.150	1	µA	V_{EN} < 0.4V (shutdown), V_{SUPPLY} = 1.6V
Thermal Shutdown Die Temperature	125	150	175	ºC	Regulator turns off
Thermal Shutdown Hysteresis		15		ºC	Regulator turns on again @ 150ºC
Power Supply Rejection Ratio		-55		dB	f ≤ 1kHz
Output Noise Voltage		800		µVRMS	I_{OUT} = 0.1mA, C_{BYP} = 0nF, V_{OUT} =3.0V
		550			I_{OUT} = 50mA, C_{BYP} = 0nF, V_{OUT} =3.0V
		150			I_{OUT} = 0.1mA, C_{BYP} = 10nF, V_{OUT} =3.0V
		100			I_{OUT} = 50mA, C_{BYP} = 10nF, V_{OUT} =3.0V
Wake-up time (T_{ON}) from Shutdown		90	200	µs	V_{IN} ≥ 1.6V, I_{OUT} = 30mA
Turn-off time (T_{OFF}) into Shutdown		90	**140**	µs	I_{OUT} = 0.1mA, V_{IN} ≥ 1.6V
Enable input logic low voltage			**0.4**	V	Regulator shutdown
Enable input logic high voltage	**1.6**			V	Regulator enabled

PIN DESCRIPTION

Pin Name	Pin Number		Description
	5 pin SC-70	5 pin SOT23	
V_{IN}	1	1	Power supply input. Connect a 1uF decoupling capacitor next to this pin.
GND	2	2	Ground Pin.
EN	3	3	Enable/Shutdown (Logic high = enable, logic low = shutdown)
BYP	4 (Fixed)	4 (Fixed)	Reference bypass input for ultra-quite operation. Connecting 10nF capacitor from this pin to ground reduces output noise
ADJ	4 (Adjustable)	4 (Adjustable)	Adjustable regulator feedback input. Connect to a resistive voltage-divider network.
V_{OUT}	5	5	Output voltage of the linear regulator. Connect a 1uF or larger capacitor from this pin to ground.

General Overview

The SP6222 and SP6223 are CMOS LDOs designed to meet a broad range of low voltage applications that require accuracy and ease of use. The SP6222 offers a 50mA output current while the SP6223 offers an output current of 150mA. The SP6222 is available in a 2.5V or 3.0V fixed output along with an adjustable output version. The SP6223 is offered in an adjustable output only. These LDOs have a minimum input voltage of only 1.6V and a maximum input voltage of 4.5V. The output voltage can be programmed to as low as 0.9V and have a maximum dropout voltage rating of 100mV for the SP6222 and 300mV for the SP6223. Both devices are equipped with an enable (EN) input for very low current (10nA typical) shutdown mode.

Enable / Shutdown Operation

The SP6222/6223 is turned on by providing 1.6V or greater to the EN pin. To place the device into shutdown pull the EN pin below 0.4V. If this feature is not required connect EN to input supply to always enable the device whenever power is applied.

Input / Output Capacitor

The SP6222/6223 is designed to operate using very small ceramic capacitors. The minimum input and output capacitor value for stable operation is 1.0μF. The output capacitor value may be increased without limit to improve transient response. Place these capacitors as close as possible to the device.

Bypass (BYP) Capacitor

The fixed output versions offer a BYP pin to decouple the bandgap reference. Connecting an external 10nF capacitor from BYP to GND can reduce output noise. If output noise is not a concern the BYP pin may be left open. When a bypass capacitor is used the turn on time is slower. See the following turn on time plots for various BYP capacitor values. The adjustable output version does not offer this BYP input.

Adjustable Regulator

The output of the device can be programmed to a specific voltage by using two external resistors connected to the ADJ pin (see Typical Application Circuit for Adjustable output). The resistors set

the output voltage based on the following equation:

$V_{OUT} = V_{REF} *(R1/R2 + 1)$

Resistor values are not critical because the ADJ (adjust) pin has a high impedance, but for best performance use resistor values of 470KΩ or less.

Thermal Considerations

The SP6222/6223 is designed to provide 50mA -150mA of continuous current in a tiny package. Maximum power dissipation can be calculated based on the output current and the voltage drop across the part. To determine the maximum power dissipation of the package, use the junction-to-ambient thermal resistance of the device and the following equation:

$P_{D(MAX)} = (T_{J(max)} – T_A) / \theta_{JA}$

$T_{J(max)}$ is the maximum junction temperature of the die and is 125°C. T_A is the ambient temperature. θ_{JA} is the junction-to-ambient thermal resistance of the package. The SOT-23 package has a θ_{JA} of approximately 191°C/W and the SC70 package has a θ_{JA} of approximately 330°C/W.

The actual power dissipation of the regulator circuit can be determined by using the simplified equation:

$P_D = (V_{IN} – V_{OUT}) * I_{OUT}$

To prevent the device from entering thermal shutdown, maximum power dissipation cannot be exceeded.

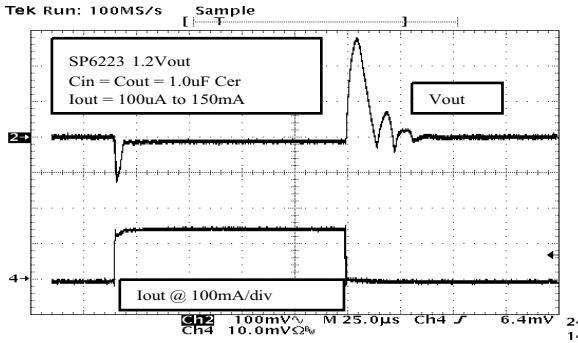
Layout Considerations

The primary path of heat conduction out of the package is via the package leads. Therefore, careful consideration must be taken into account for optimizing layout.

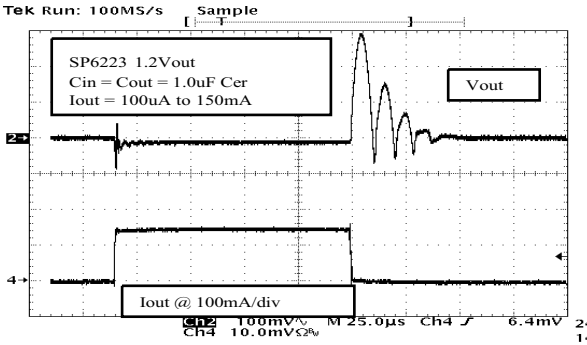
1. Attaching the part to a large copper footprint will enable better heat transfer from the device, especially where there are internal ground and power planes.

2. Place the input and output capacitors close to the device for optimal transient response and device behavior.

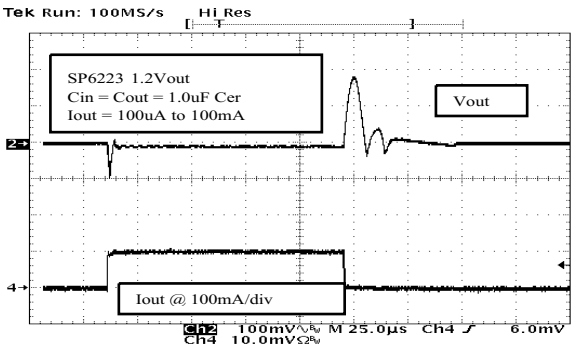
3. Connect all ground connections directly to the ground plane. In case there is no ground plane, connect to a common ground point before connecting to board ground.



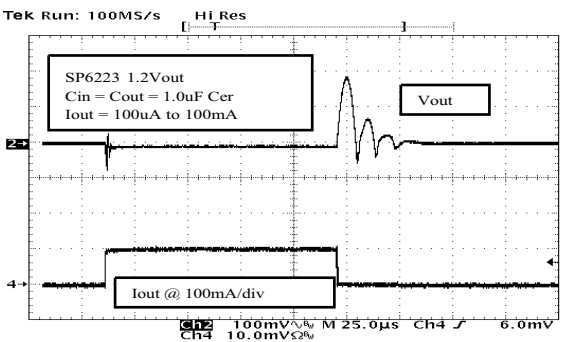
Load Transient Response, 100µA to 150mA, Vin = 1.6V



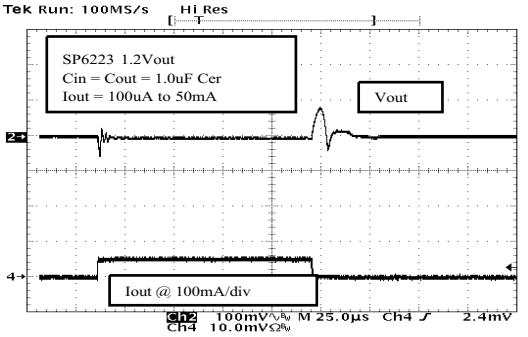
Load Transient Response, 100µA to 150mA, Vin = 3.3V



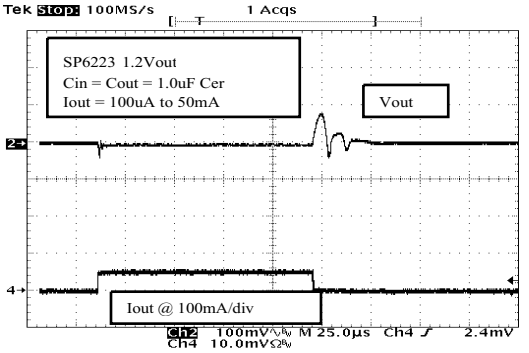
Load Transient Response, 100µA to 100mA, Vin = 1.6V



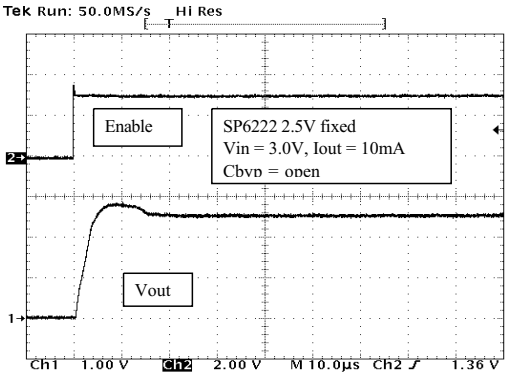
Load Transient Response, 100µA to 100mA, Vin = 3.3V



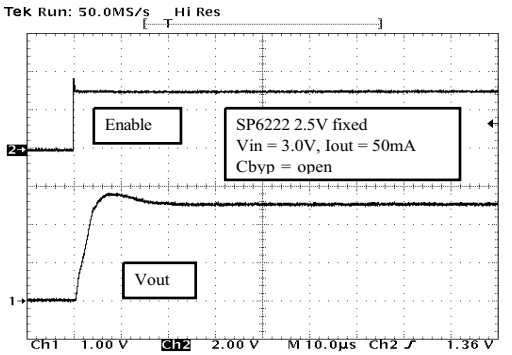
Load Transient Response, 100µA to 50mA, Vin = 1.6V



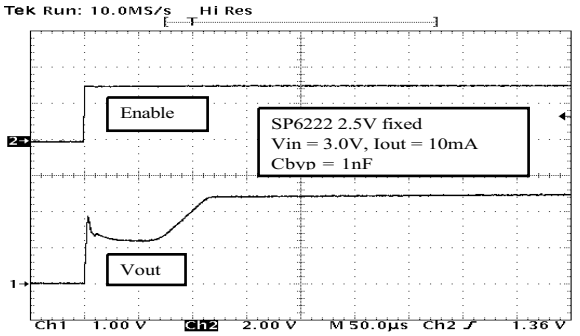
Load Transient Response, 100µA to 50mA, Vin = 3.3V



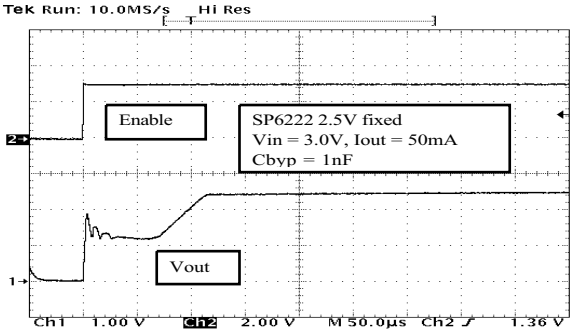
Turn on time, Vin = 3.0V, Iout = 10mA, CBYP = Open



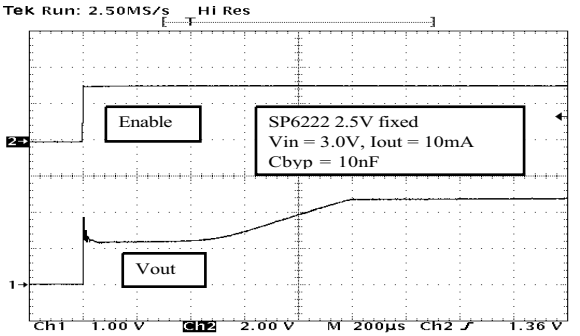
Turn on time, Vin = 3.0V, Iout = 50mA, CBYP = Open



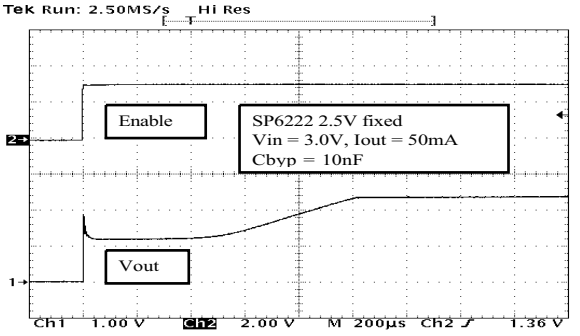
Turn on time, Vin = 3.0V, Iout = 10mA, CBYP = 1nF



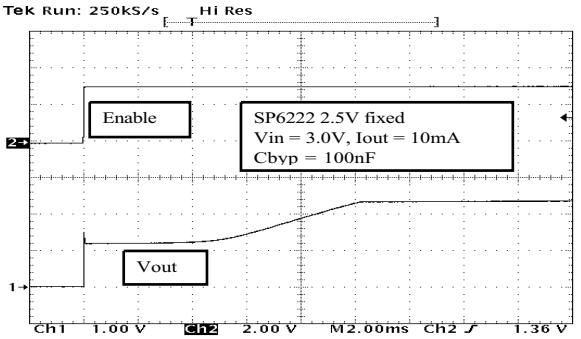
Turn on time, Vin = 3.0V, Iout = 50mA, CBYP = 1nF



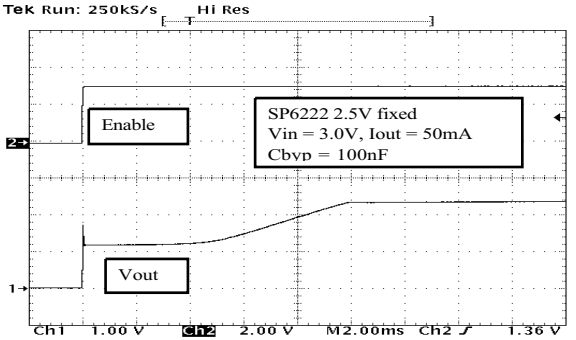
Turn on time, Vin = 3.0V, Iout = 10mA, CBYP = 10nF



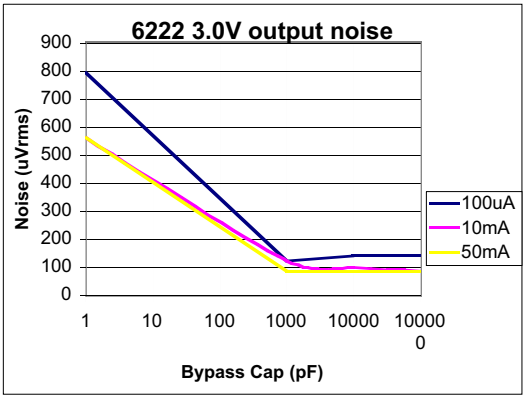
Turn on time, Vin = 3.0V, Iout = 50mA, CBYP = 10nF



Turn on time, Vin = 3.0V, Iout = 10mA, CBYP = 100nF

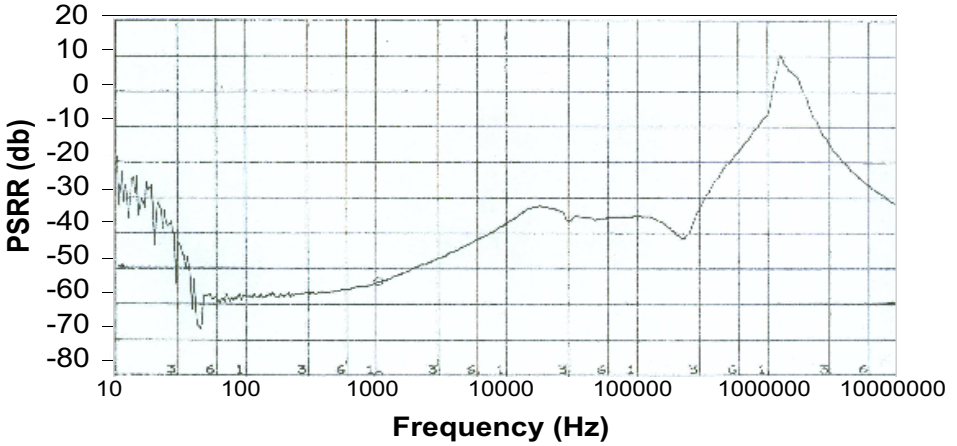


Turn on time, Vin = 3.0V, Iout = 50mA, CBYP = 100nF

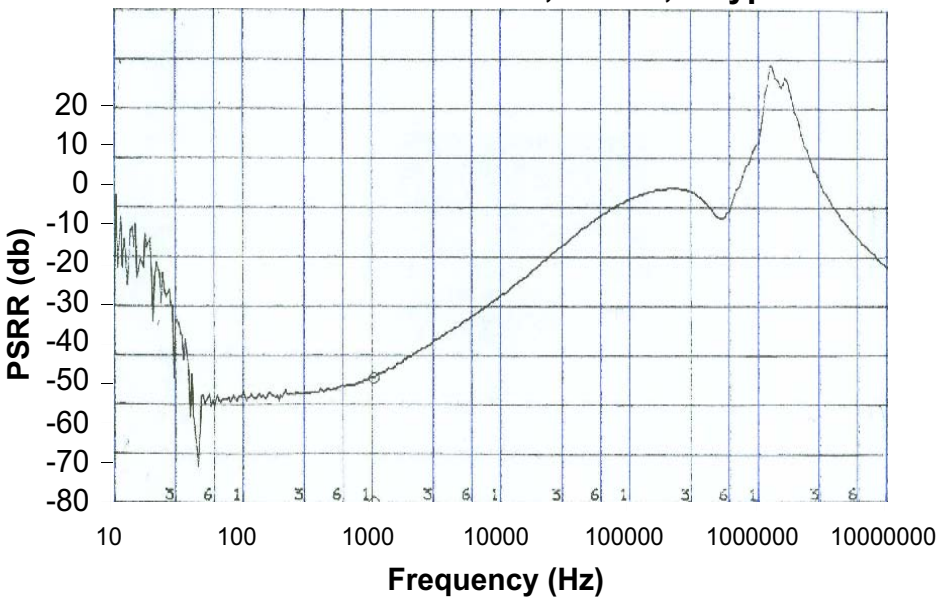


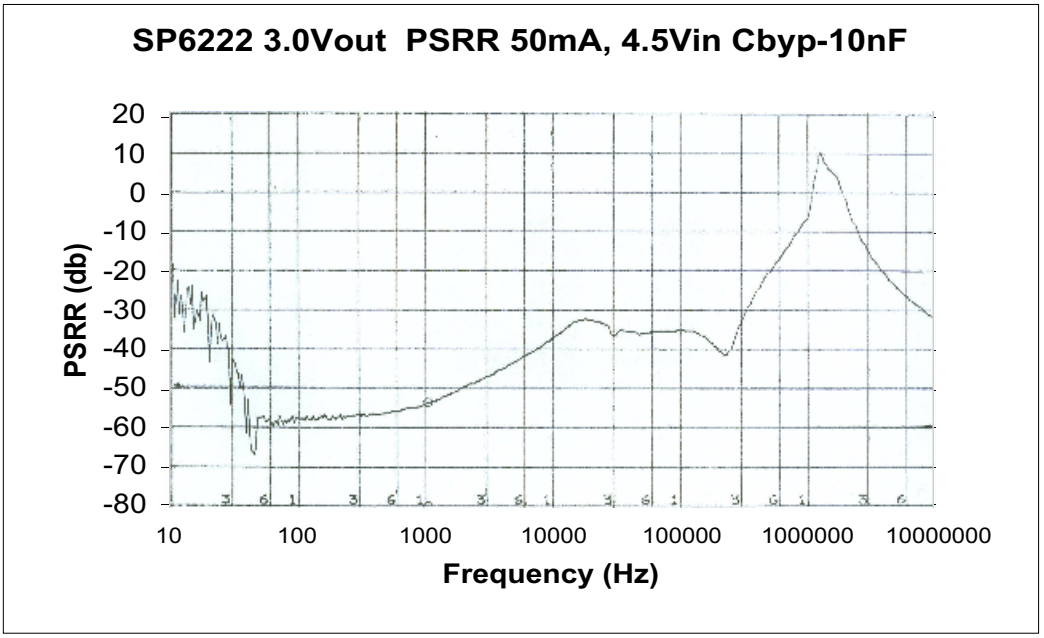
SP6222 3.0V Output Noise vs. CBYP

SP6222 3.0Vout PSRR 100uA, 4.5 Vin Cbyp-10nF

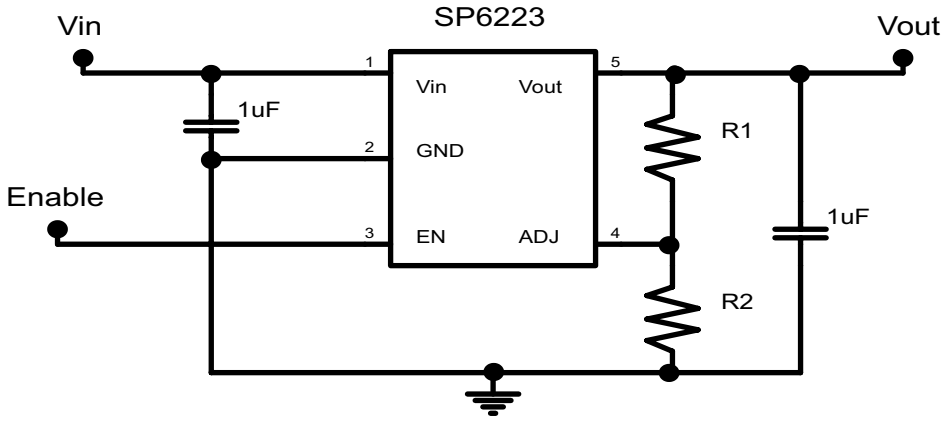


SP6222 3.0Vout PSRR 10mA, 4.5Vin, Cbyp-10nF

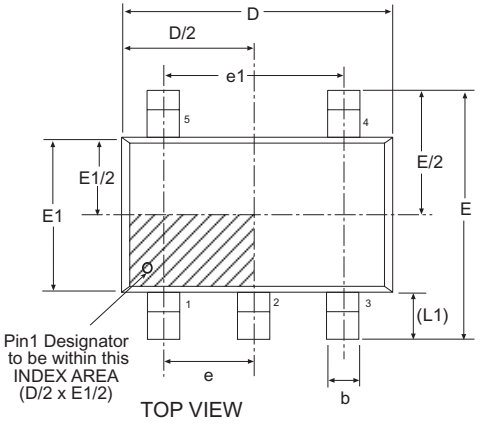


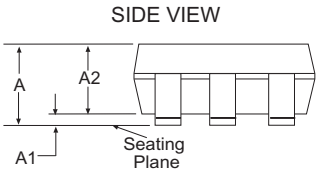


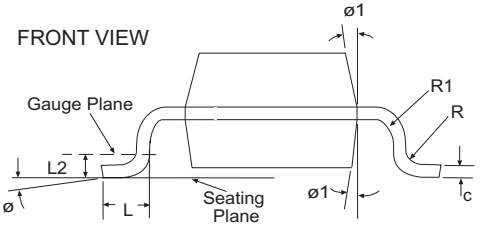
Typical Application Circuit for Adjustable Output



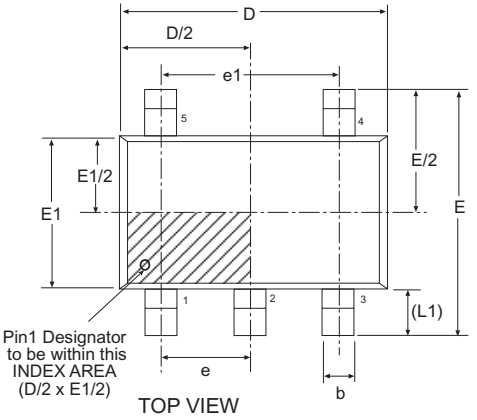
$V_{OUT} = V_{REF} * [1 + (R1/R2)]$

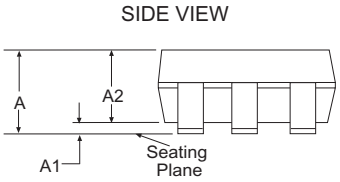


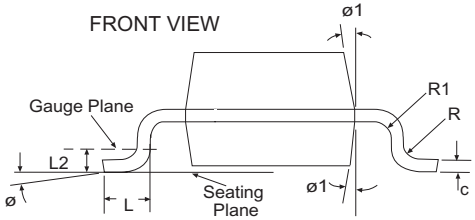




5 Pin SC-70 JEDEC MO-203 Variation AA						
SYMBOL	Dimensions in Millimeters: Controlling Dimension			Dimensions in Inches Conversion Factor: 1 Inch = 25.40 mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.10	-	-	0.043
A1	0.00	-	0.10	0.000	-	0.004
A2	0.70	0.90	1.00	0.028	0.036	0.039
c	0.08	-	0.22	0.004	-	0.009
D	2.00 BSC			0.079 BSC		
E	2.10 BSC			0.083 BSC		
E1	1.25 BSC			0.049 BSC		
L	0.26	0.36	0.46	0.011	0.014	0.018
L1	0.42 REF			0.017 REF		
L2	0.15 BSC			0.006 BSC		
R	0.10	-	-	0.004	-	-
R1	0.10	-	0.25	0.004	-	0.010
Ø	0˚	4º	8º	0˚	4º	8º
Ø1	4˚	-	12º	4˚	-	12º
b	0.15	-	0.30	0.006	-	0.012
e	0.65 BSC			0.026 BSC		
e1	1.30 BSC			0.051 BSC		
SIPEX Pkg Signoff Date/Rev: JL Oct3-05 / Rev A						







5 Pin SOT-23 JEDEC MO-178 Variation AA						
SYMBOL	Dimensions in Millimeters: Controlling Dimension			Dimensions in Inches Conversion Factor: 1 Inch = 25.40 mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.45	-	-	0.057
A1	0.00	-	0.15	0.000	-	0.006
A2	0.90	1.15	1.30	0.036	0.045	0.051
c	0.08	-	0.22	0.004	-	0.009
D	2.90 BSC			0.115 BSC		
E	2.80 BSC			0.111 BSC		
E1	1.60 BSC			0.063 BSC		
L	0.30	0.45	0.60	0.012	0.018	0.024
L1	0.60 REF			0.024 REF		
L2	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
R1	0.10	-	0.25	0.004	-	0.010
Ø	0º	4º	8º	0º	4º	8º
ø1	5º	10º	15º	5º	10º	15º
b	0.30	-	0.50	0.012	-	0.020
e	0.95 BSC			0.038 BSC		
e1	1.90 BSC			0.075 BSC		
SIPEX Pkg Signoff Date/Rev:				JL Oct3-05 / Rev A		

Part Number	Temperature Range	Voltage Option	Package Type
SP6222EC5-2-5-L	-40˚C to +125˚C	2.5V	(Lead Free) 5 Pin SC70
SP6222EC5-2-5-L/TR	-40˚C to +125˚C	2.5V	(Lead Free) 5 Pin SC70
SP6222EC5-3-0-L	-40˚C to +125˚C	3.0V	(Lead Free) 5 Pin SC70
SP6222EC5-3-0-L/TR	-40˚C to +125˚C	3.0V	(Lead Free) 5 Pin SC70
SP6222EC5-L	-40˚C to +125˚C	ADJ	(Lead Free) 5 Pin SC70
SP6222EC5-L/TR	-40˚C to +125˚C	ADJ	(Lead Free) 5 Pin SC70
SP6222EK-2-5-L	-40˚C to +125˚C	2.5V	(Lead Free) 5 Pin SOT-23
SP6222EK-2-5-L/TR	-40˚C to +125˚C	2.5V	(Lead Free) 5 Pin SOT-23
SP6222EK-3-0-L	-40˚C to +125˚C	3.0V	(Lead Free) 5 Pin SOT-23
SP6222EK-3-0-L/TR.	-40˚C to +125˚C	3.0V	(Lead Free) 5 Pin SOT-23
SP6222EK-L	-40˚C to +125˚C	ADJ	(Lead Free) 5 Pin SOT-23
SP6222EK-L/TR	-40˚C to +125˚C	ADJ	(Lead Free) 5 Pin SOT-23
SP6223EC5-L	-40˚C to +125˚C	ADJ	(Lead Free) 5 Pin SC70
SP6223EC5-L/TR	-40˚C to +125˚C	ADJ	(Lead Free) 5 Pin SC70
SP6223EK-L	-40˚C to +125˚C	ADJ	(Lead Free) 5 Pin SOT-23
SP6223EK-L/TR	-40˚C to +125˚C	ADJ	(Lead Free) 5 Pin SOT-23

Available in lead free packaging only.

/TR = Tape and Reel

Pack quantity is 3,000 for SC-70 and 2,500 for SOT-23.

Sipex Corporation

Headquarters and Sales Office
233 South Hillview Drive
Milpitas, CA 95035
TEL: (408) 934-7500
FAX: (408) 935-7600

Appendix and Web Link Information

For further assistance:

Email:	Sipexsupport@sipex.com
WWW Support page:	http://www.sipex.com/content.aspx?p=support
Sipex Application Notes:	http://www.sipex.com/applicationNotes.aspx
Product Change Notices:	http://www.sipex.com/content.aspx?p=pcn

Sipex Corporation
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Sales Office
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Milpitas, CA95035
tel: (408) 934-7500
faX: (408) 935-7600

The following sections contain information which is more changeable in nature and is therefore generated as appendices.

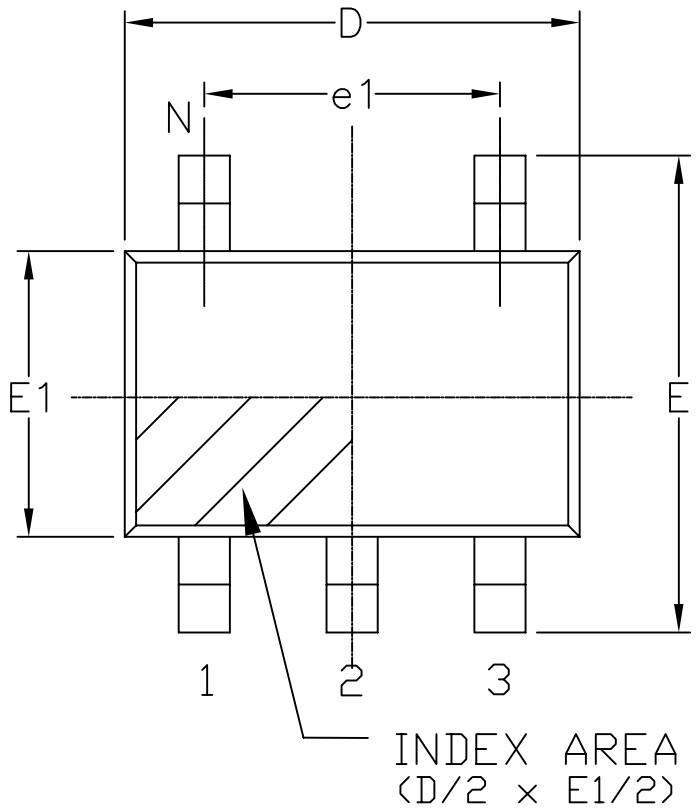
1) **Package Outline Drawings**
2) **Ordering Information**

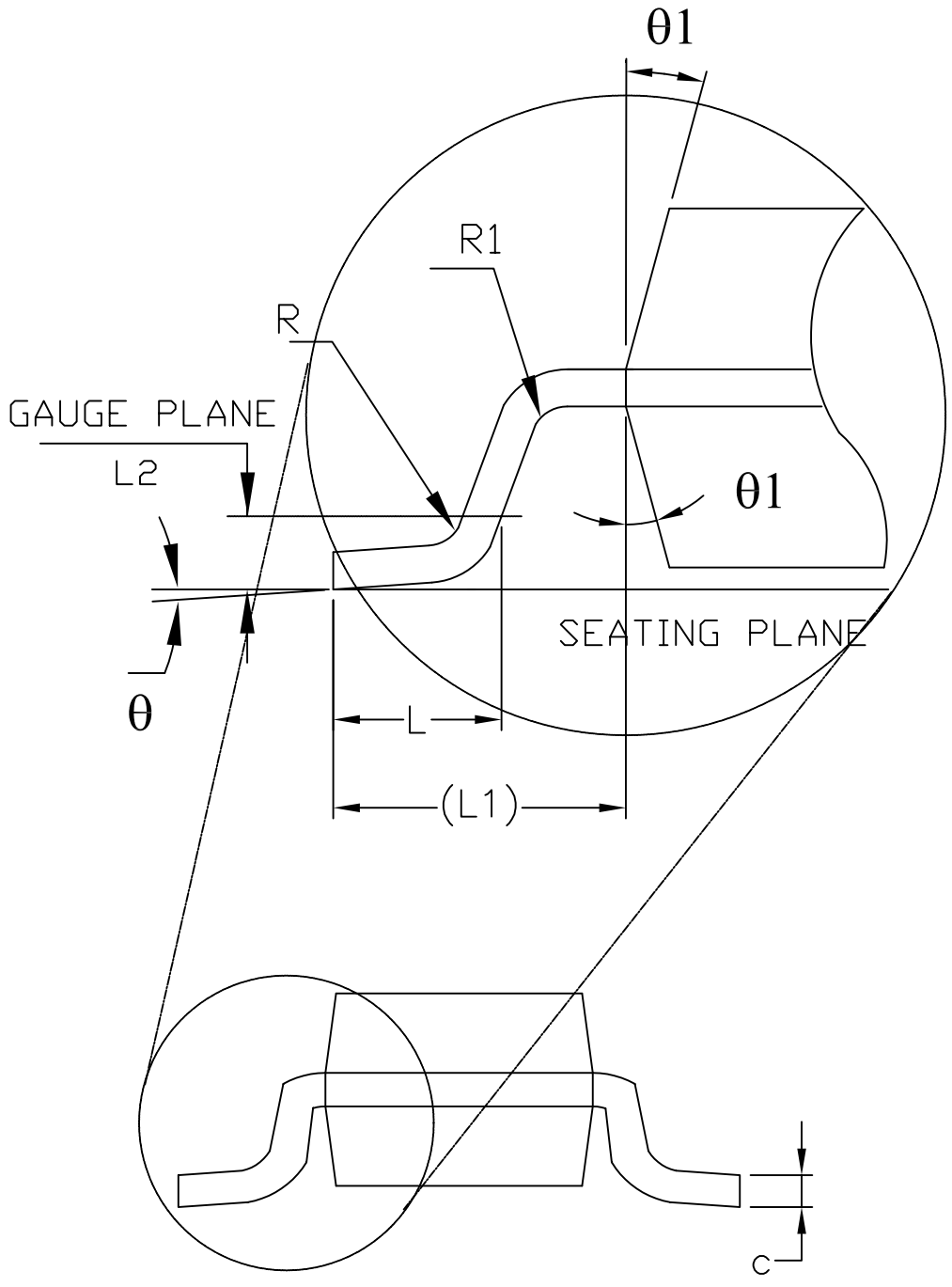
If Available:

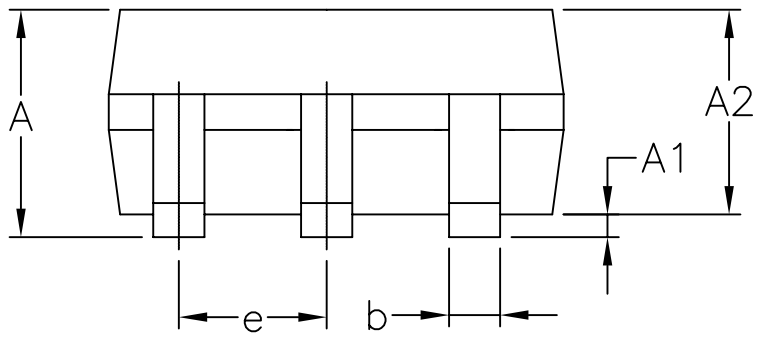
3) **Frequently Asked Questions**
4) **Evaluation Board Manuals**
5) **Reliability Reports**
6) **Product Characterization Reports**
7) **Application Notes for this product**
8) **Design Solutions for this product**

REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	10/03/05	JL
B	DRAWING FORMAT MODIFICATION	07/24/06	JL

Top View







Side View

Front View

5 Pin SC-70 JEDEC MO-203 Variation AA						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.10	—	—	0.043
A1	0.00	—	0.10	0.000	—	0.004
A2	0.70	0.90	1.00	0.028	0.036	0.039
b	0.15	—	0.30	0.006	—	0.012
c	0.08	—	0.22	0.003	—	0.009
D	2.00 BSC			0.079 BSC		
E	2.10 BSC			0.083 BSC		
E1	1.25 BSC			0.049 BSC		
e	0.65 BSC			0.026 BSC		
e1	1.30 BSC			0.051 BSC		
L	0.26	0.36	0.46	0.011	0.014	0.018
L1	0.42 REF			0.017 REF		
L2	0.15 BSC			0.006 BSC		
R	0.10	—	—	0.004	—	—
R1	0.10	—	0.25	0.004	—	0.010
θ	0°	4°	8°	0°	4°	8°
θ1	4°	—	12°	4°	—	12°
N	5			5		

Solved by Sipex™

SIPEX CORPORATION

5 PIN SC-70 PACKAGE OUTLINE

Packaging Approval:

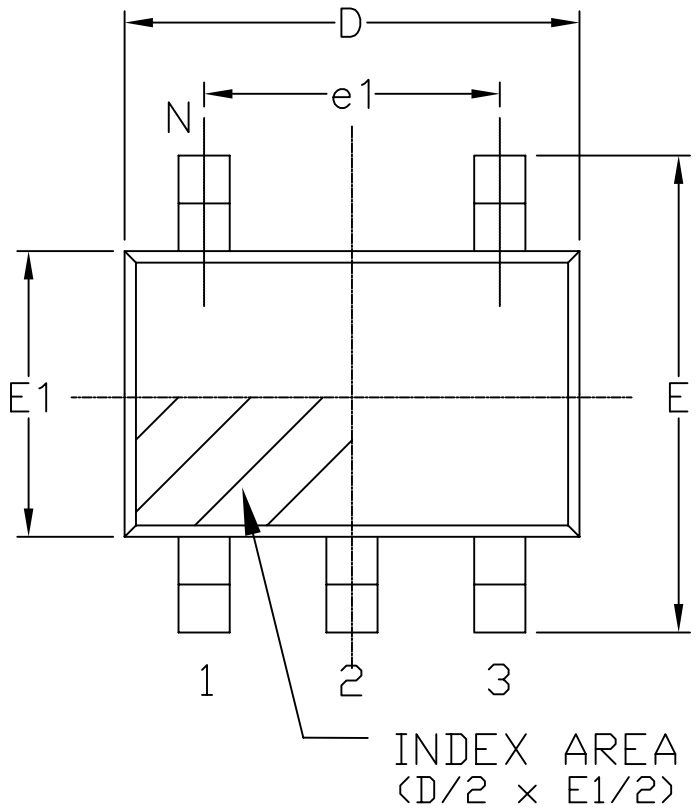
By: JL | Date: 07/24/06

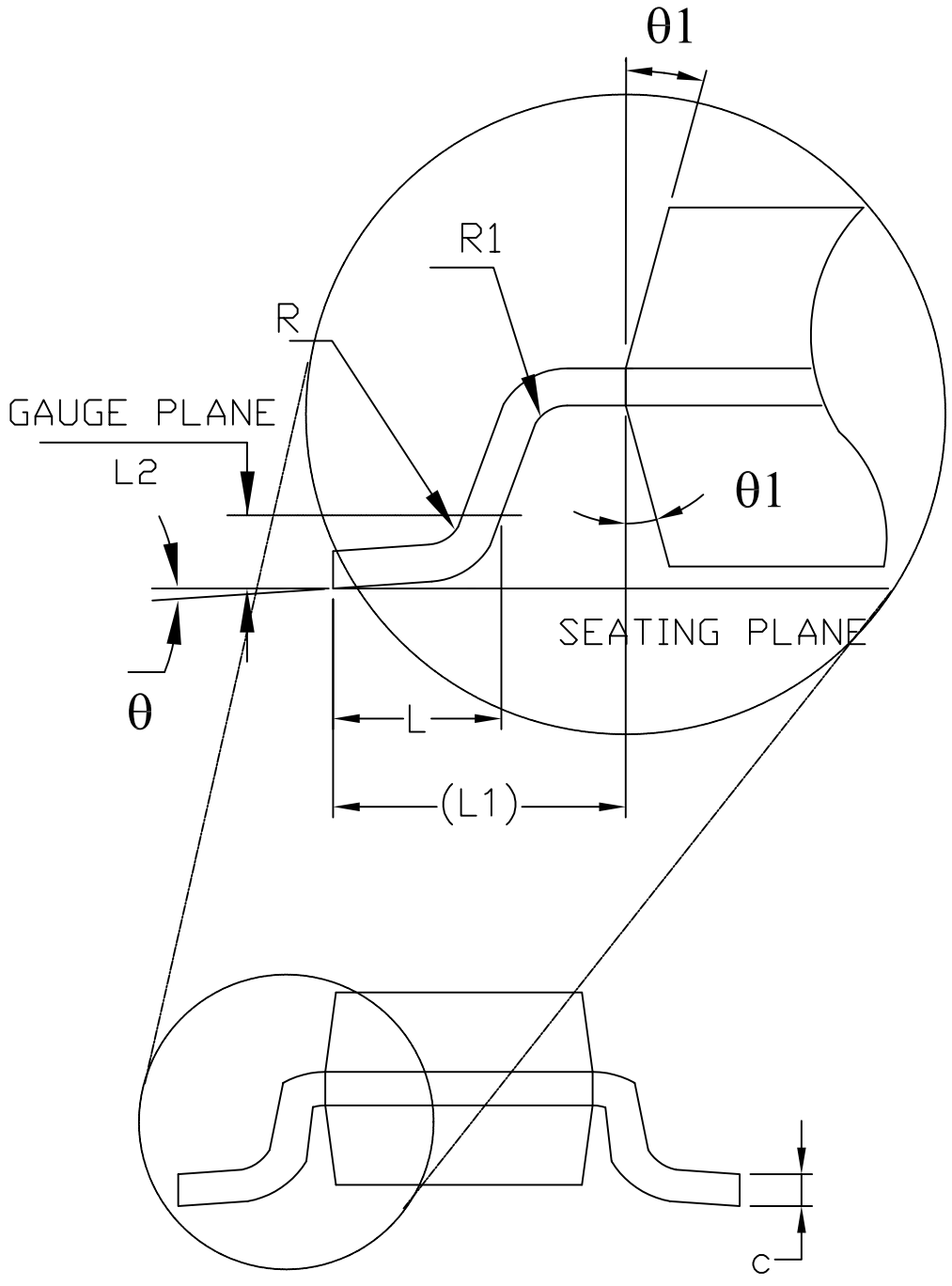
Drawing No: 5-PIN SC-70

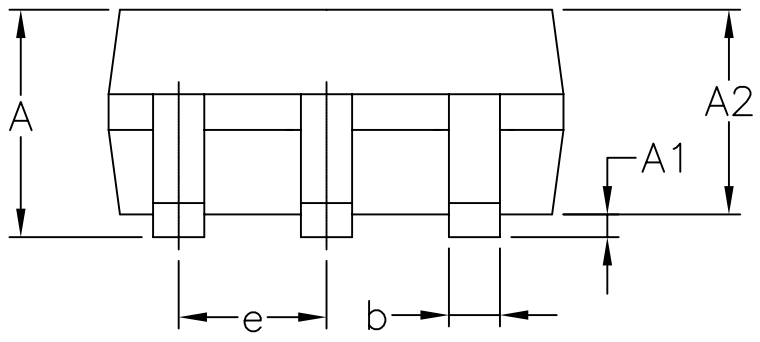
Revision: B | Sheet: 1 OF 1

REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	10/3/05	JL
B	DRAWING FORMAT MODIFICATION	07/25/06	JL

Top View







Side View

Front View

5 Pin SOT-23 JEDEC MO-178 Variation AA						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.45	—	—	0.057
A1	0.00	—	0.15	0.000	—	0.006
A2	0.90	1.15	1.30	0.036	0.045	0.051
b	0.30	—	0.50	0.012	—	0.020
c	0.08	—	0.22	0.003	—	0.009
D	2.90 BSC			0.115 BSC		
E	2.80 BSC			0.111 BSC		
E1	1.60 BSC			0.063 BSC		
e	0.95 BSC			0.038 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.30	0.45	0.60	0.012	0.018	0.024
L1	0.60 REF			0.024 REF		
L2	0.25 BSC			0.010 BSC		
R	0.10	—	—	0.004	—	—
R1	0.10	—	0.25	0.004	—	0.010
θ	0°	4°	8°	0°	4°	8°
θ1	5°	10°	15°	5°	10°	15°
N	5			5		

Solved by Sipex™

SIPEX CORPORATION

5 PIN SOT-23 PACKAGE OUTLINE

Packaging Approval:

By: JL Date: 07/25/06

Drawing No: 5-PIN SOT-23

Revision: B Sheet: 1 OF 1

SP6222/23: FAQ

Part Number: SP6222 and SP6223
Date: June 26, 2006

50mA and 150mA CMOS Linear Regulators

The SP6222 and SP6223 are CMOS LDOs designed to meet a broad range of applications that require accuracy and ease of use. These LDOs offer extremely low quiescent current, providing advantages in performance over comparable bipolar LDOs. The SP6222 and SP6223 LDOs support an extremely wide load range with excellent high and low frequency PSRR (55dB typical), exceptional line regulation and temperature stability over the operating temperature range (-40°C to +125°C). An enable feature on all versions reduces quiescent to 10nA in shutdown mode to conserve battery life.

Value Proposition

- Very Low VIN down to 1.6V
- Low IQ in 14uA typical and 25uA max at room temp
- Excellent PSRR @ 55dB gives excellent line regulation
- Small footprint in 5-pin SC70 and SOT23 package
- Available in ADJ version supports VOUT from as low as 0.9V
- Offered in lead-free RoHS

Competitive Analysis

	Micrel	Mitsumi	Sipex
	MIC5265-2.5 / MIC5265-3.0	MM1572F / MM1573A	SP6222 / SP6223
V_{IN} range	2.7V to 5.5V	V_{OUT}+0.5V to 12V	1.6V to 4.5V
V_{OUT}	2.5V & 3.0V	2.5V & 3.0V	2.5V, 3.0V, & Adj.
V_{OUT} Accuracy	3%	2%	2%
Dropout Voltage	75mV(typ) @ 50mA, 500mV(max) @ 150mA	200mV @ 50mA	100mV(max) @ 50mA, 300mV(max) @150mA
Line Regulation	0.20%	0.20%	0.20%
I_{OUT}	150mA	150mA	SP6222=50mA, SP6223=150mA
Load Regulation	600µV/mA	600µV/mA	225µv/mA
Ground Pin Current	150µA	85µA	25µA
Shutdown Current	2µA	15µA	1µA
V_{OUT} Noise	57µV_{RMS}, w/C_{BYP}=0.1µF	30µV_{RMS}, w/C_{BYP}=0.01µF	100µV_{RMS}, w/C_{BYP}=10nF
Operating Temp. Range	-40°C to +85°C	-35°C to +85°C	-40°C to +125°C

Question:

How do we find out if a Voltage Option will become available soon? What is the process for getting a Voltage Option generated?

Answer:

Please contact Sipex Customer support at CustomerSupport@sipex.com The opportunity will be evaluated by the Marketing Department at Sipex and they will get in touch with you. An alternative path is through your local distributor or sales representative. Our contact page on the Sipex website is http://www.sipex.com/contact.aspx

Low Dropout Family: FAQ

Sipex Family: **Low Dropout Regulators**

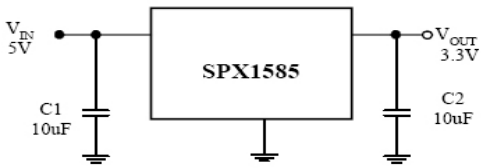
Date: Aug22, 2006

Question:

Are the connection details of a fixed version LDO the same as the adjustable version? I went through the datasheet provided -- it has connection details of only the adjustable version. Do I have to connect resistor R1 AND R2 even in the fixed version?

Answer:

An LDO with fixed output such as the SPX1587 does not require external voltage divider resistors for they are internal. Only the Adjustable versions need a divider for setting output voltage. This info is generally within the Datasheet. The external resistor voltage divider is only used for programming the output voltage of an adjustable part. For the fixed output part, simply connect the ADJ/GND input (pin 1) to GND for typical configuration. Below diagram is from the SPX1585 data sheet showing how a basic fixed regulator is configured. Pin 1 is GND, Pin 2 is Vout and Pin 3 is Vin. Please keep in mind that the package tab is usually connected to Vout and should be isolated if the tab is connected to your GND plane. Some designers will enlarge the Vout plane to allow for the tab connection resulting in no need to isolate tab.



Basic Fixed Regulator

Question:

Is there a simple way to figure out heat loss for an LDO?

Answer:

Yes. Try our Excel-based heat calculation spreadsheet ANP2 available online at http://www.sipex.com/files/ApplicationNotes/ThermalCalculator.xls

For further study, this spreadsheet is mentioned in the following helpful application note: “ANP2: Thermal Considerations for Linear Regulators” http://www.sipex.com/files/ApplicationNotes/LDOThermal.pdf

Reliability and Qualification Report

SP6222, SP6223
CMOS Linear Regulators

Prepared by: G. West
Quality Assurance Manager
Date: 06/26/06

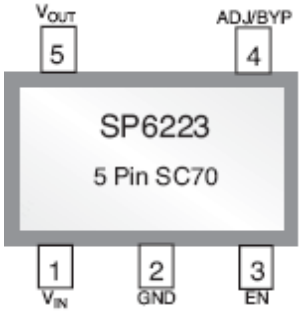
Reviewed by: Fred Claussen
VP Quality & Reliability
Date: 06/26/06

Table Of Contents

Device Description

The SP6222 and SP6223 are CMOS LDOs designed to meet a broad range of applications that require accuracy, speed and ease of use. These LDOs offer extremely low quiescent current which only increases slightly under load, thus providing advantages in ground current performance over bipolar LDOs. The LDOs handle an extremely wide load range and guarantee stability with a 1µF ceramic output capacitor. They have excellent low frequency PSRR, not found in other CMOS LDOs and thus offer exceptional Line Regulation. High frequency PSRR is 55dB (typical) at 1kHz. Load Regulation is excellent and temperature stability is comparable to bipolar LDOs. An enable feature is provided on all versions. The SP6222/6223 is available in fixed and adjustable output voltage versions in industry standard SC70 and SOT23 packages.

Pin Out



Manufacturing Information:

Products:	SP6222, SP6223
Description:	CMOS Linear Regulators
Process:	PBC4 CMOS

SP6222, SP6223 Family Reliability Qualification Test Summary

Device	Lot #	Stress Level	Burn-In Temp	Sample Size	No. Fail
SP6623	3786A001	1000 Hrs	125 °C	77	0
SP6623	4347A001	1000 Hrs	125 °C	77	0
SP6623	2375A001	1000 Hrs	125 °C	58	0

Life Test

Life testing is conducted to determine if there are any fundamental reliability related failure mechanism(s) present in the device.

These failure mechanisms can be divided roughly into four groups:

1. Process or die related failures, such as oxide-related defects, metalization-related defects and diffusion-related defects.
2. Assembly-related defects such as chip mount wire bond or package-related failures.
3. Design related defects.
4. Miscellaneous, undetermined or application-induced failures.

Life Test Results

As part of the Sipex design qualification program, the Engineering group had subjected 211 SP6223 parts for a 1000 hour Reliability life test at 125° C

168 hour Life test

211 parts were subjected to the life test profile and completed 168 hours without any part failures.

500 hour Life test

The 211 parts were re-introduced to the second phase of the test, where the parts successfully completed the 500-hour life test without any failures.

1000 hour Life test

211 parts completed the full1000 hour life/HTOL test successfully, without showing any significant shift in the process parameters.

FIT Rate Calculations

The FIT (failures in time) rate is the predicted number of failures per billion device-hours. This predicted value is based upon the:

1. Life Test conditions (time and temperature, device quantity and number of failures) are summarized under HTOL test table.
2. Activation Energy (E_a) of the potential failure modes.

The weighted Activation Energy, E_a, of observed failure mechanisms of Sipex products has been determined to be 0.8 eV.

Based on the above criteria, the FIT rates at 25°, 55° and 70°C operation at both 60% and 90% confidence levels for the SP331 family products have been calculated and are listed below.

FIT Failure Rates for SP6222, SP6223 Products

Confidence Level	+25°C	+55°C	+70°C
60%	6.3	64.9	180.7
90%	16.6	169.9	473.2

1 FIT = 1 Failure per Billion Device-Hours

MTBF for SP6222, SP6223 Products

Confidence Level	+25°C	+55°C	+70°C
60%	1.58E+08	1.54E+07	5.53E+06
90%	6.03E+07	5.89E+06	2.11E+06

ESD Testing

Human Body Model (HBM) ESD testing was performed per method 3015.7 of MIL-STD-883E using a Keytek Zapmaster 7/4 discharging a 100pF capacitor through a 1.5 Kohm resistor. Three units from lot # 2375A001 were subjected to three discharges of both positive and negative polarity. All units passed after discharges of +/- 4KV.

Lath-up Testing

Latch-up testing was performed on 5 units per EIAJ-ED-17. +/-100mA pulse currents were applied with the unit at 125C ambient temperature. No failures were detected