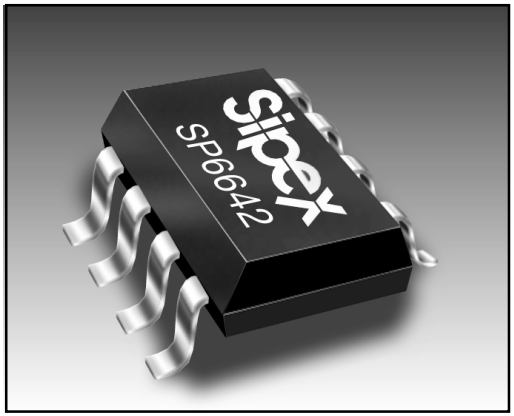
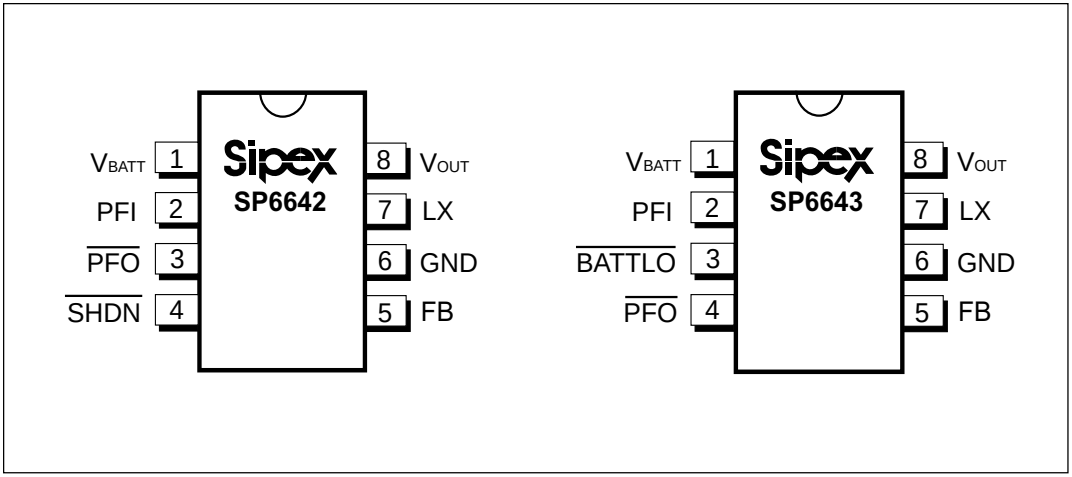
Single Alkaline Cell, High Efficiency Step-Up DC-DC Converter

- 20mA Output Current at 1.2V Input
- +2V to +5.5V Output Range
- 0.85V Guaranteed Start-Up
- 83% High Efficiency
- 1.5µA Quiescent Supply Current at V_{BATT}
- Reverse Battery Protection
- Internal Synchronous Rectifier
- 5nA Logic Controlled Shutdown Current From V_{BATT} For The SP6642
- Low-Battery Detection Active LOW Output For The **SP6643**
- Extremely Small µSOIC Package
- Pin-to-pin Compatible With MAX1642 And MAX1643



DESCRIPTION

The SP6642/6643 devices are high-efficiency, low-power step-up DC-DC converters for +1V inputs ideal for single alkaline cell applications such as pagers, remote controls, and other low-power portable end products. Designers can control the SP6642 device with a 1nA active LOW shutdown input. The SP6643 features an active LOW output for low-battery conditions. Both devices contain a 0.8Ω synchronous rectifier, an oscillator, a 0.6Ω N-channel MOSFET power switch, an internal voltage reference, circuitry for pulse-frequency-modulation, and an under voltage comparator. The output voltage for the SP6642/6643 devices is preset to +3.3V ± 4% or can be adjusted from +2V to +5.5V by manipulating two external resistors.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{BATT} to GND.....-0.3 to 6.0V
V_{OUT} to GND.....-0.3 to 6.0V
LX, $\overline{SHDN}$, FB, $\overline{BATTLO}$, $\overline{PFO}$ to GND....-0.3 to 6.0V
PFI to GND.....-0.3 to 6.0V
Reverse battery Current, T_{AMB}=+25°C.....220mA (NOTE 1)
V_{BATT} forward current.....0.5A
V_{OUT}, LX current.....1A
Storage Temperature Range.....-65˚C to +165˚C
Lead Temperature (soldering 10s).....+300˚C
Operating Temperature.....-40˚C to +85˚C

Power Dissipation Per Package
8-pin µSOIC (derate 4.85mW/°C above +70°C).....390mW

CAUTION:
ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

SPECIFICATIONS

V_{BATT} = $V_{\overline{SHDN}}$ = 1.3V, I_{LOAD} = 0mA, FB = GND, T_{AMB} = -40°C to +85°C, and typical values are at T_{AMB} = +25°C unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Minimum Operating Input Voltage, $V_{BATT(MIN)}$		0.2		V	R_L=3kΩ
Maximum Operating Input Voltage, $V_{BATT(MAX)}$			1.65	V	
Start-Up Input Voltage (V_{BATT}), NOTE 2	0.85	0.75		V	R_L=3kΩ,T_{AMB}=+25°C
Start-Up Input Voltage (V_{BATT}), Temperature Coefficient		-2		mV/°C	
$\overline{SHDN}$ Input Voltage V_{IL} V_{IH}	 80		20	%	 % of V_{BATT} for the **SP6642** % of V_{BATT} for the **SP6642**
$\overline{SHDN}$ Input Current			10	nA	**SP6642**
FB Input Current			10	nA	V_{FB}=1.3V
FB Set Voltage, V_{FB}	1.215	1.262	1.309	V	external feedback
PFI Input Current			10	nA	V_{PFI}=650mV
PFI Trip Voltage	590	614	632	mV	falling PFI,hysteresis=1%
$\overline{BATTLO}$ Trip Voltage	0.96	1.00	1.04	V	V_{OUT} = 3.3V, hysteresis = 2%, **SP6643**
Output Voltage, V_{OUT}	3.16	3.30	3.44	V	V_{FB}<0.1V
Output Voltage Range	2.0		5.5	V	external feedback
N-Channel On-Resistance		0.6	1.5	Ω	V_{OUT}=3.3V
P-Channel On-Resistance		0.8	2.2	Ω	V_{OUT}=3.3V
P-Channel Catch-Diode Voltage		0.8		V	I_{DIODE}=100mA,P-Channel switch off

SPECIFICATIONS (continued)

V_{BATT} = $V_{\overline{SHDN}}$ = 1.3V, I_{LOAD} = 0mA, FB = GND, T_{AMB} = -40°C to +85°C, and typical values are at T_{AMB} = +25°C unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Quiescent Current into V_{OUT}, I_{QOUT}		13	20	µA	V_{OUT}=3.5V
Quiescent Current into V_{BATT}, I_{QBATT}		1.5	2.5	µA	V_{BATT}=1.0V
Shutdown Current into V_{OUT}, $I_{SHDNOUT}$		0.001	0.5	µA	V_{OUT}=3.5V for the **SP6642**
Shutdown Current into V_{BATT}, $I_{SHDNBATT}$		0.005	0.1	µA	V_{BATT}=1.0V for the **SP6642**
Low Output Voltage for $\overline{PFO}$ and $\overline{BATTLO}$, V_{OL}			0.4	V	V_{PFI}=0V,V_{OUT}=+3.3V,I_{SINK}=1mA
Leakage Current for $\overline{PFO}$ and $\overline{BATTLO}$			1	µA	V_{PFI}=650mV,$V_{\overline{PFO}}$=6V
BATTLO Trip Voltage	0.96	1.0	1.04	V	V_{OUT}=+3.3V,hysteresis=2% for the **SP6643**
On-Time Constant, K	17	25	35	V-µs	0.9V<V_{BATT}<1.5V (t_{ON}=K/V_{BATT})
Off-Time Tracking Ratio (NOTE 3)	1		1.5		0.9V<V_{BATT}<1.5V,V_{OUT}=+3.3V
Efficiency		83		%	I_{LOAD}=20mA

NOTE 1: The reverse battery current is measured from the Typical Operating Circuit's input terminal to GND when the battery is connected backward. A reverse current of 220mA will not exceed package dissipation limits but, if left for an extended time (more than 10 minutes), may degrade performance.

NOTE 2: Start-up guaranteed by correlation to measurements of device parameters (i.e. switch on-resistance, on-times, and output voltage trip points.

NOTE 3: tOFF = Ratio x $\left[\frac{t_{ON} \times V_{BATT}}{V_{OUT} - V_{BATT}}\right]$. This guarantees discontinous condition.

NOTE 4: Specifications to -40ºC are guaranteed by design, not production tested.

PERFORMANCE CHARACTERISTICS

Refer to the circuit in *Figure 25* with V_{BATT} = 1.2V, R1 + R2 = 1MΩ, and T_{AMB} = +25°C unless otherwise noted.

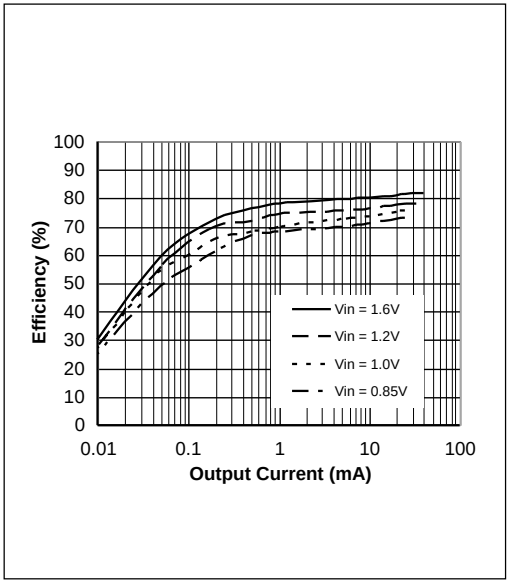


Figure 1. Efficiency vs. Output Current (V_{OUT}=2.4V) where L1=100μH, Sumida CD54-101

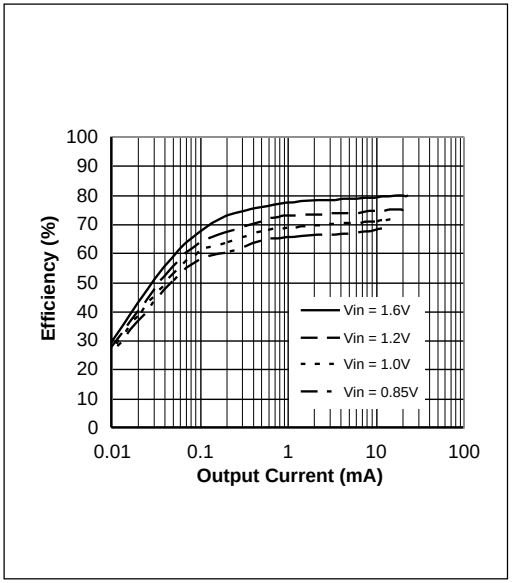


Figure 2. Efficiency vs. Output Current (V_{OUT}=2.4V) where L1=150μH, TDK NLC565050T-151K

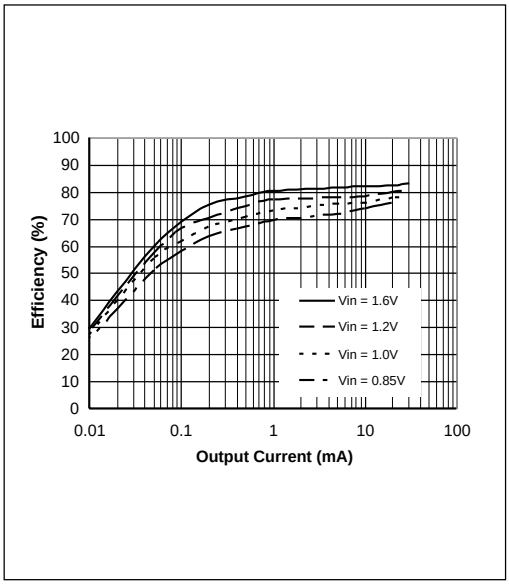


Figure 3. Efficiency vs. Output Current (V_{OUT}=3.3V) where L1=100μH, Sumida CD54-101

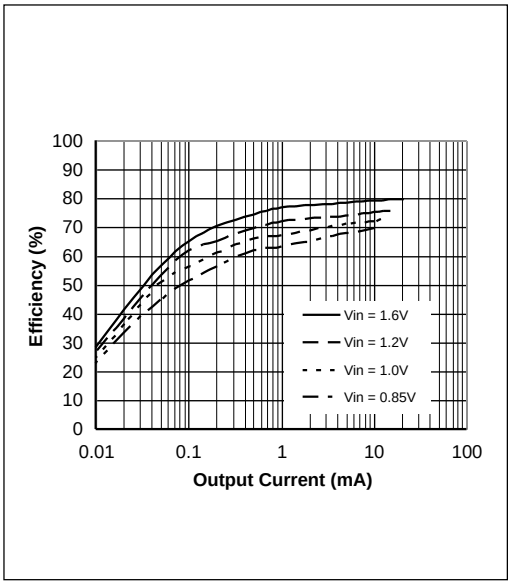


Figure 4. Efficiency vs. Output Current (V_{OUT}=3.3V) where L1=150μH, TDK NLC565050T-151K

PERFORMANCE CHARACTERISTICS (continued)

Refer to the circuit in *Figure 25* with V_{BATT} = 1.2V, R1 + R2 = 1MΩ, and T_{AMB} = +25°C unless otherwise noted.

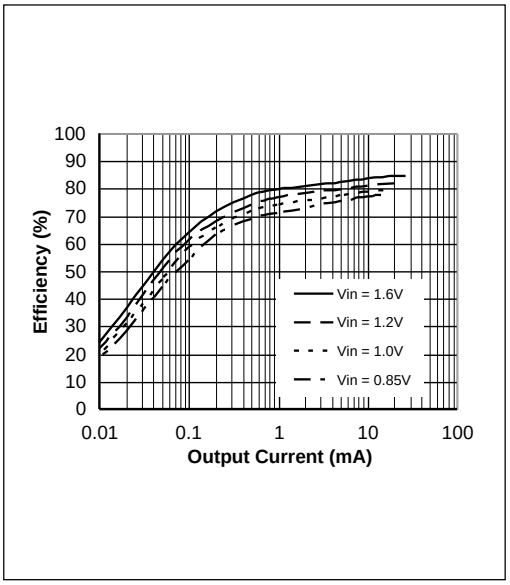


Figure 5. Efficiency vs. Output Current (V_{OUT}=5.0V) where L1=100μH, Sumida CD54-101

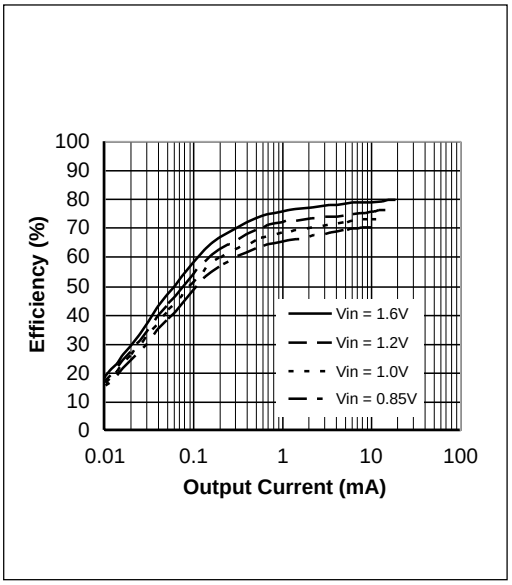


Figure 6. Efficiency vs. Output Current (V_{OUT}=5.0V) where L1=150μH, TDK NLC565050T-151K

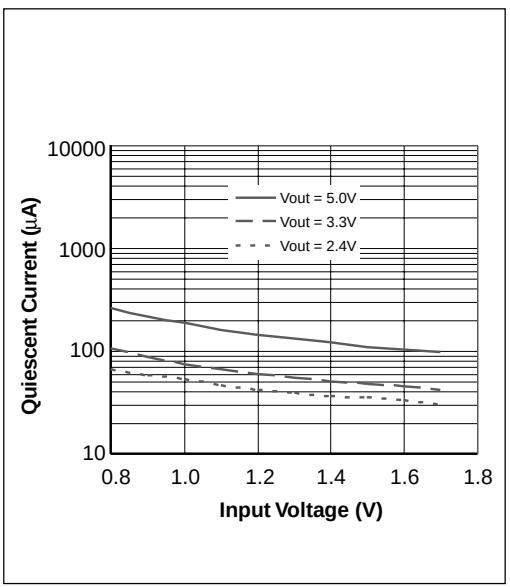


Figure 7. No-Load Battery Current vs. Input voltage

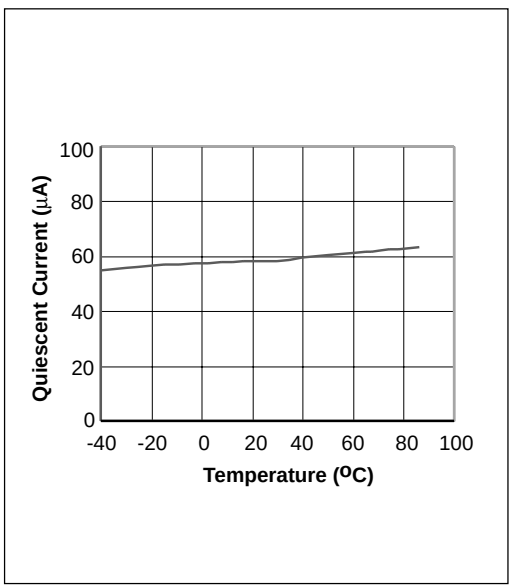


Figure 8. No-Load Battery Current vs. Temperature Where V_{BATT} = 1.2V, V_{OUT} = 3.3V

PERFORMANCE CHARACTERISTICS (continued)

Refer to the circuit in *Figure 25* with V_{BATT} = 1.2V, R1 + R2 = 1MΩ, and T_{AMB} = +25°C unless otherwise noted.

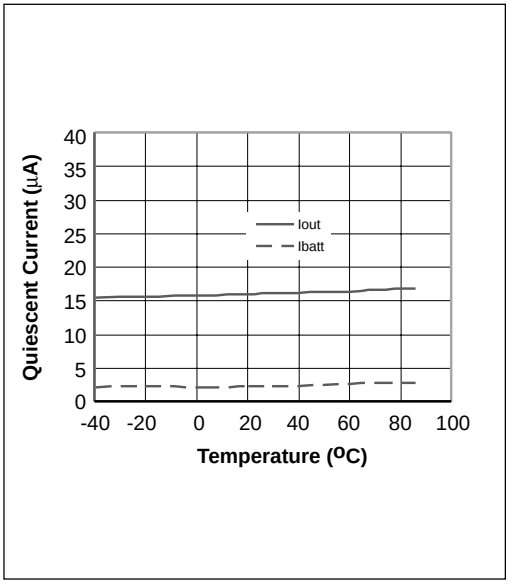


Figure 9. V_{BATT} and V_{OUT} Pin Quiescent Currents vs. Temperature where V_{BATT} = 1.2V, V_{OUT} = 3.6V

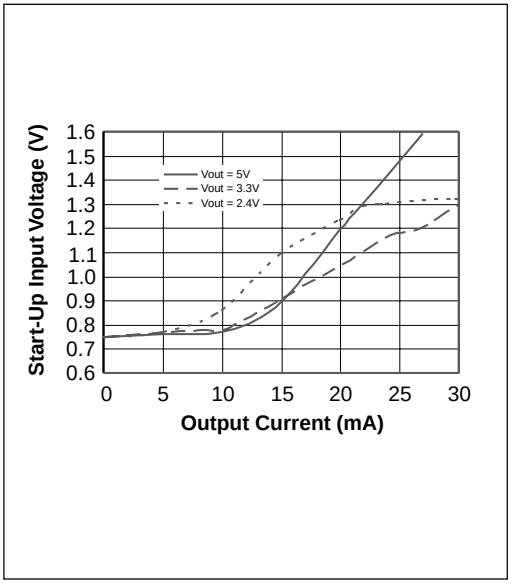


Figure 10. Minimum Start-Up Input Voltage vs. Output Current where L1=100µH, Sumida CD54-101

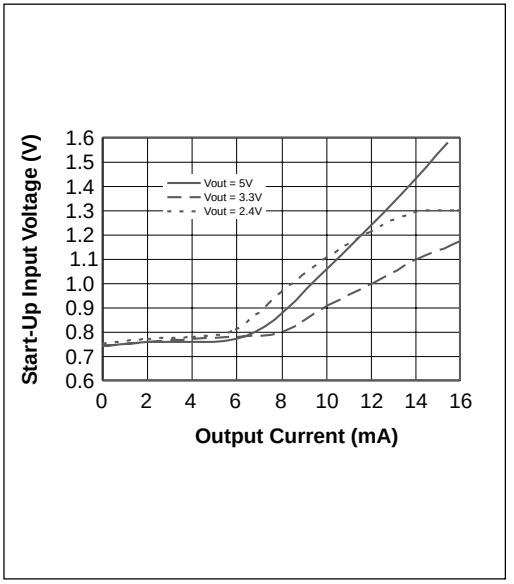


Figure 11. Minimum Start-Up Input Voltage vs. Output Current where L1=150µH, TDK NLC565050T-151K

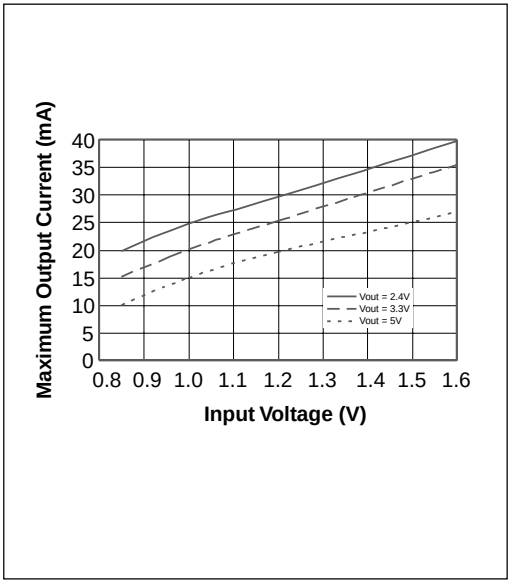


Figure 12. Maximum Output Current vs. Input Voltage where L1=100µH, Sumida CD54-101

PERFORMANCE CHARACTERISTICS (continued)

Refer to the circuit in *Figure 25* with V_{BATT} = 1.2V, R1 + R2 = 1MΩ, and T_{AMB} = +25°C unless otherwise noted.

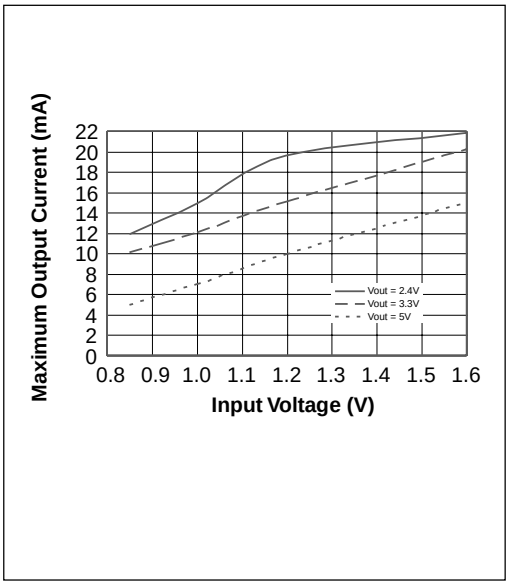


Figure 13. Maximum Output Current vs. Input Voltage where L1=150µH, TDK NLC565050T-151K

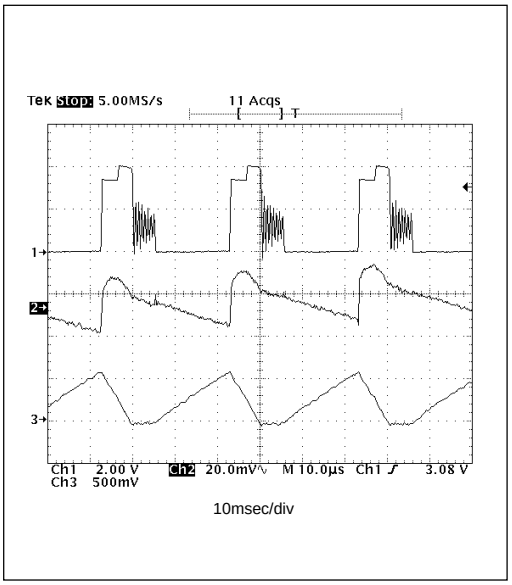


Figure 14. Switching Waveforms:
V_{OUT}=3.3V, V_{IN}=1.2V, I_{OUT}=12mA where
1: LX, 2V/div, L1=TDK NKLC565050T-151K
2: V_{OUT}, 20mV/div, 3.3V DC offset
3: Inductor Current, 100mA/div

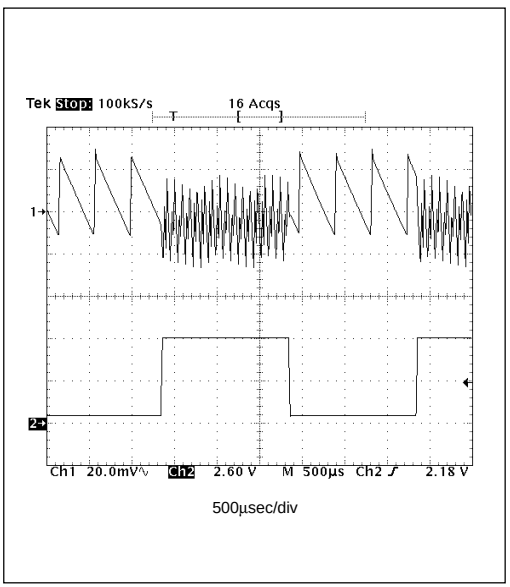


Figure 15. Load-Transient Response:
V_{OUT}=3.3V, V_{BATT}=1.2V where
1: V_{OUT}, 20mV/div, 3.3V DC offset
2: LOAD, 2mA to 20mA, 10mA/div

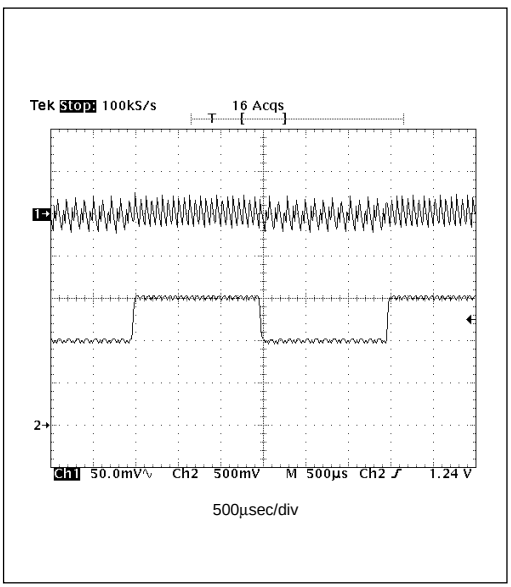


Figure 16. Line-Transient Response:
V_{OUT}=3.3V, LOAD=15mA where
1: V_{OUT}, 50mV/div, 3.3V DC offset
2: V_{BATT}, 1V to 5V, 500mV/div

PERFORMANCE CHARACTERISTICS (continued)

Refer to the circuit in *Figure 25* with V_{BATT} = 1.2V, R1 + R2 = 1MΩ, and T_{AMB} = +25°C unless otherwise noted.

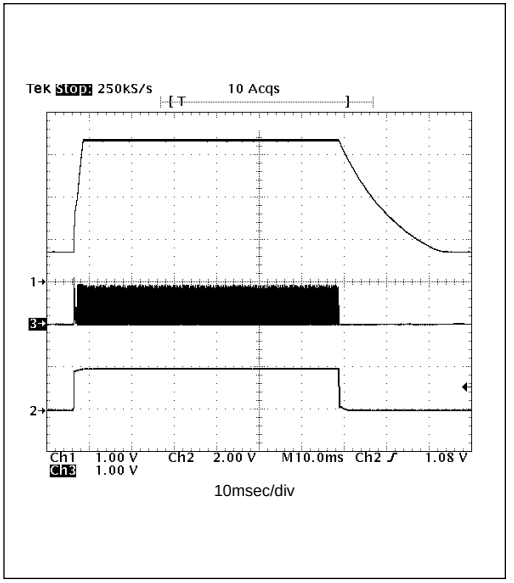


Figure 17. Shutdown Response and Inductor Current: V_{OUT}=3.3V, V_{BATT}=1.2V, I_{OUT}=5mA where
1: V_{OUT}, 1V/div
2: $\overline{SHDN}$, 2v/div
3: Inductor Current, 200mA/div

NAME	FUNCTION	PIN NUMBER	
		SP6642	SP6643
V_{BATT}	Battery Supply. For the **SP6643**, this pin ties to the sensor input of the $\overline{BATTLO}$ comparator.	1	1
PFI	Power-Fail Input. When the voltage on PFI drops below 614mV, $\overline{PFO}$ sinks current.	2	2
$\overline{BATTLO}$	Open-Drain Battery-LOW Output. When the voltage at V_{BATT} drops below 1V, $\overline{BATTLO}$ sinks current.	-	3
$\overline{PFO}$	Open-Drain Power-Fail Output. Sinks current when PFI drops below 614mV.	3	4
$\overline{SHDN}$	Active-LOW Shutdown Input. Connect to V_{BATT} for normal operation.	4	-
FB	Feedback Input. Input for adjustable-output operation. Connect this input pin to an external resistor voltage divider between V_{OUT} and GND. Connect to GND for fixed-output operation.	5	5
GND	Connect to the lowest circuit potential, typically ground.	6	6
LX	Coil. An inductor is connected from V_{BATT} to the N-Channel MOSFET switch drain and the P-Channel synchronous-rectifier drain through this pin.	7	7
V_{OUT}	Power Output. Feedback input for fixed 3.3V operation and IC power input. Connect filter capacitor close to V_{OUT}.	8	8

Table 1. SP6642/6643 Pin Descriptions

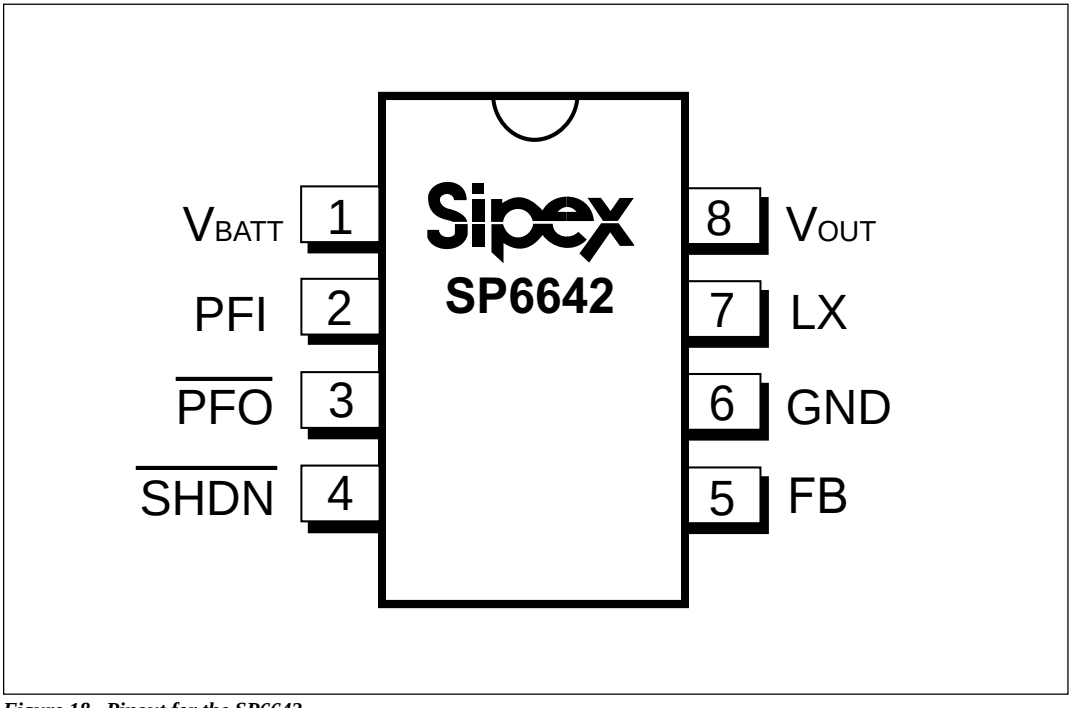


Figure 18. Pinout for the SP6642

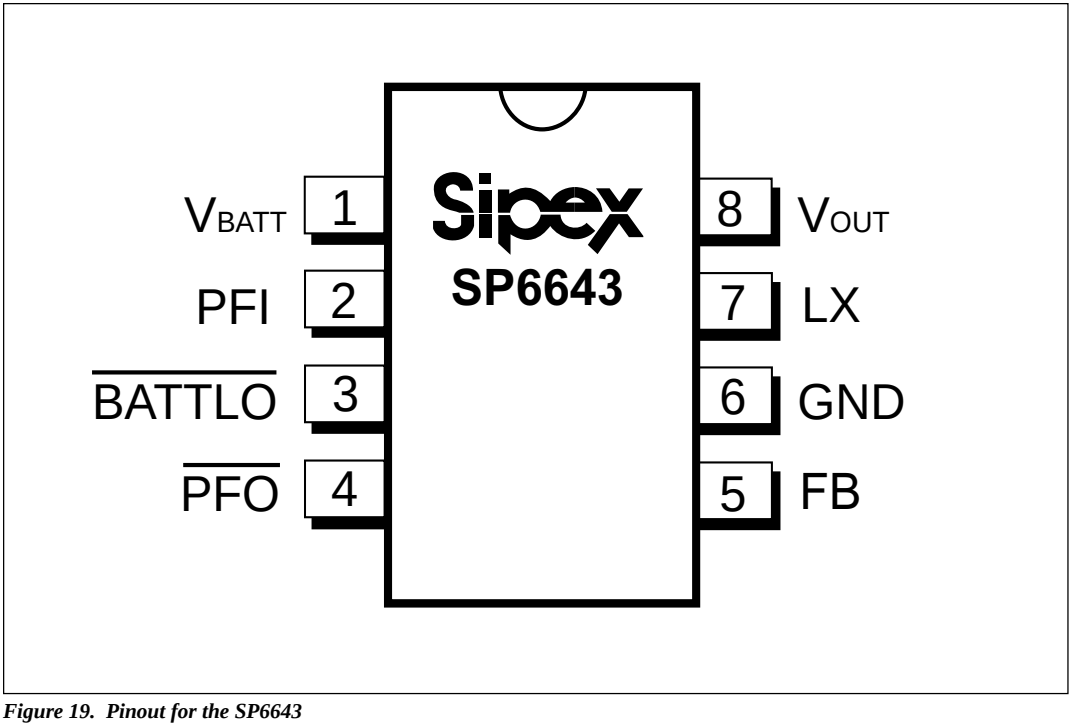


Figure 19. Pinout for the SP6643

DESCRIPTION

The SP6642/6643 devices are high-efficiency, low-power step-up DC-DC converters ideal for single alkaline cell applications such as pagers, remote controls, and other low-power portable end products.

The SP6642 features a 5nA logic-controlled shutdown mode. The SP6643 features dedicated low-battery detector circuitry. Both devices contain a 0.8Ω synchronous rectifier, an oscillator, a 0.6Ω N-channel MOSFET power switch, an internal voltage reference, circuitry for pulse-frequency-modulation, and an under voltage comparator. The output voltage for the SP6642/6643 devices can be adjusted from +2V to +5.5V by manipulating two external resistors. The output voltage is preset to +3.3V.

THEORY OF OPERATION

The SP6642/6643 devices are ideal for end products that function with a single alkaline cell, such as remote controls, pagers, and other portable consumer products. Designers can implement the SP6642/6643 devices into applications with the following power management operating states: 1. where the primary battery is good and the load is active, and 2. where the primary battery is good and the load is sleeping.

In the first operating state where the primary supply is good and the load is active, the SP6642/6643 devices typically offer 80% efficiency, drawing tens of milliamps.

Applications will predominantly operate in the second state where the primary supply is good and the load is sleeping. The SP6642/6643 devices draw a very low quiescent current while the load in its disabled state will draw typically hundreds of microamps.

The pulse-frequency-modulation (PFM) circuitry provides higher efficiencies at low to moderate output loads than traditional PWM converters are capable of delivering.

The on-time and minimum off-times are varied as a function of the input and output voltages:

$$t_{ON} = \frac{K}{V_{BATT}}$$

$$t_{OFF(MIN)} = \frac{1.2 \times K}{V_{OUT} - V_{BATT}}$$

where t_{ON} is the on-time, K is the on-time constant typically 25V-µs, V_{BATT} is the supply voltage, $t_{OFF(MIN)}$ is the minimum off-time, and V_{OUT} is the output voltage. This allows the SP6642/6643 devices to maintain a high efficiency over a wide range of loads and input/output voltages. The DC-DC converter is powered from V_{OUT}.

In a state where the error comparator detects that the output voltage at V_{OUT} is too low, the internal N-channel MOSFET switch is turned on until the on-time is satisfied. Refer to *Figures 20, 21*, 22 and *23*. During the on-time, current ramps up in the inductor, storing energy in a magnetic field. When the MOSFET turns off, during the second half of each cycle the magnetic field collapses. This causes the inductor voltage to force current through the synchronous rectifier transferring the stored energy from the inductor to the output filter capacitor and the load. The output filter capacitor stores charge while current from the inductor is high and holds the output voltage high until the second half of the next switching cycle, smoothing power flow to the load.

Internal Bootstrap Circuitry

The internal bootstrap circuitry contains a low-voltage start-up oscillator that pumps up the output voltage to approximately 1.9V so the main DC-DC converter can function. At lower battery supply voltages, the circuitry can start up with low-load conditions. Designers can reduce the load as needed to allow start-up with input voltages below 1V. Refer to *Figures 10* to *13*. Once started, the output voltage can maintain the load as the battery voltage decreases below the initial start-up voltage. The start-up oscillator is powered by V_{BATT} driving a charge pump and NMOS switch. During start-up, the P-channel synchronous rectifier remains off and either its body diode or an external diode is used as an output rectifier.

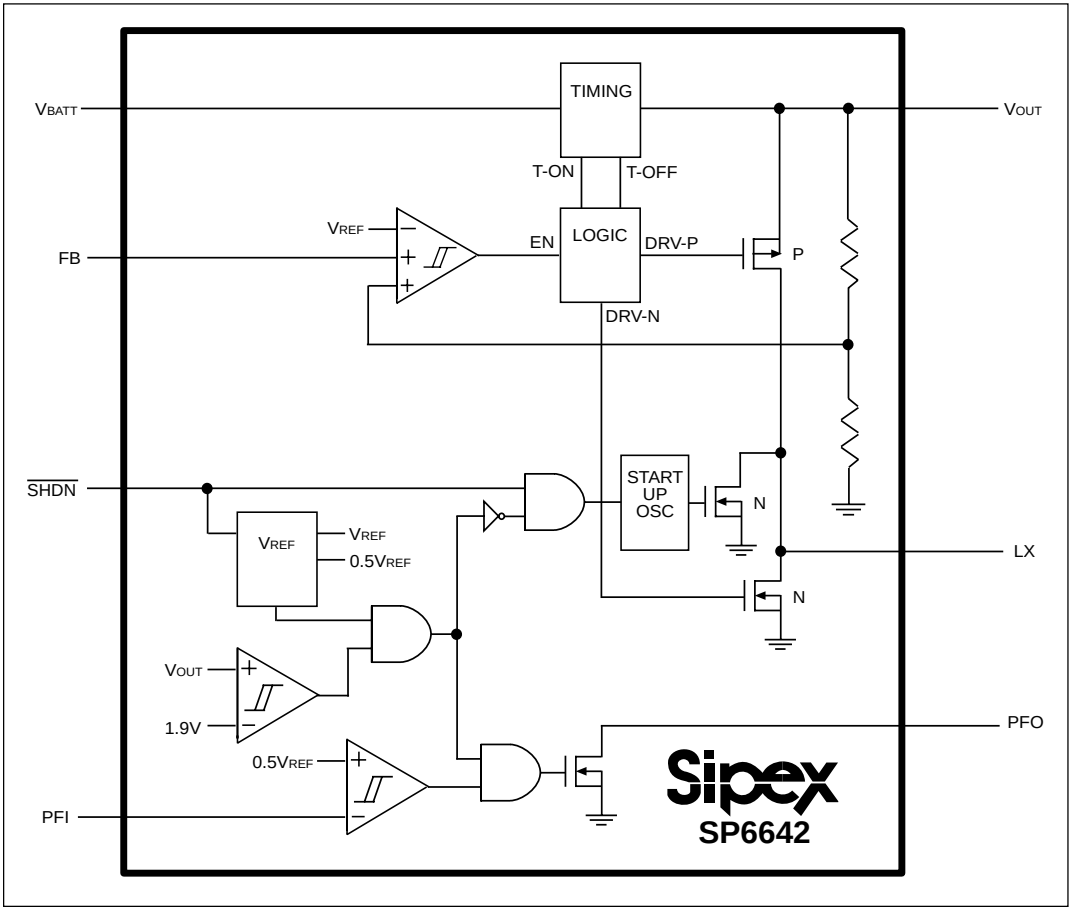


Figure 20. Internal Block Diagram of the SP6642

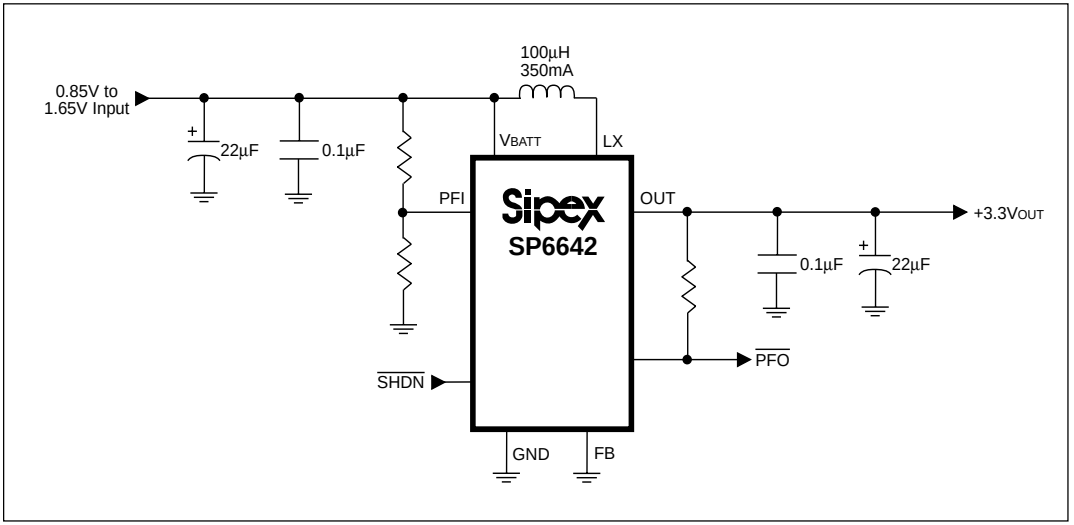


Figure 21. SP6642 +3.3V Typical Application Circuit

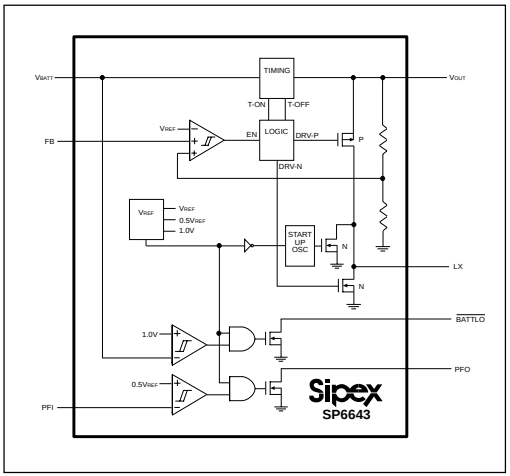


Figure 22. Internal block diagram of the SP6643

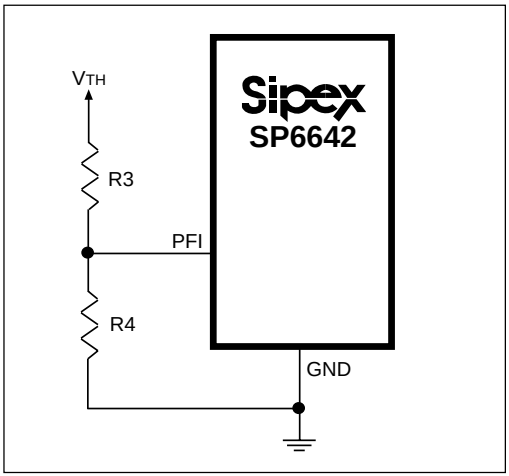


Figure 24. Power-Fail Detection Circuitry

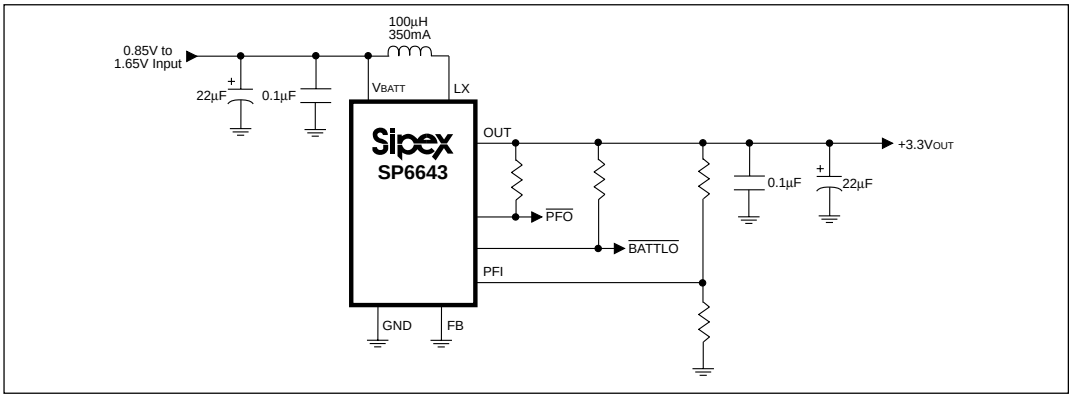


Figure 23. SP6643 +3.3V Typical Application Circuit

Power-Fail Detection Circuitry

The SP6642/6643 devices have an internal comparator for power-fail detection. This comparator can detect a loss of power at the input or output. If the voltage at PFI falls below 614mV, the $\overline{PFO}$ output sinks current to ground. Hysteresis at the power-fail input is 1%. The power-fail monitor's threshold voltage is determined by two resistors, R3 and R4. Refer to *Figure 24*. The power-fail monitor threshold voltage can be set using the following equation:

$$R3 = R4 \times \left[\frac{V_{TH}}{V_{PFI}} - 1 \right]$$

where R3 and R4 are the resistors in *Figure 24*, V_{TH} is the desired threshold voltage of the power-fail detector, and V_{PFI} is the 614mV reference of the power-fail comparator. Since PFI leakage is 10nA max, select feedback resistor R4 in the 100kΩ to 1MΩ.

$\overline{BATTLO}$ for the SP6643

The SP6643 device has an internal comparator for low-battery detection. If V_{BATT} drops below 1V, $\overline{BATTLO}$ will sink current. $\overline{BATTLO}$ is an open-drain output. $\overline{BATTLO}$ used in conjunction with the power-fail detection circuitry (PFI/$\overline{PFO}$) will monitor both the input and output voltages.

Shutdown for the SP6642

A logic LOW at $\overline{SHDN}$ will drive the SP6642 into a shutdown mode where $\overline{PFO}$ goes into a high-impedance state, the internal switching MOSFET turns off, and the synchronous rectifier turns off to prevent reverse current from flowing from the output back to the input. Designers should note that in shutdown, the output can drift to one diode drop below V_{BATT} because there is still a forward current path through the

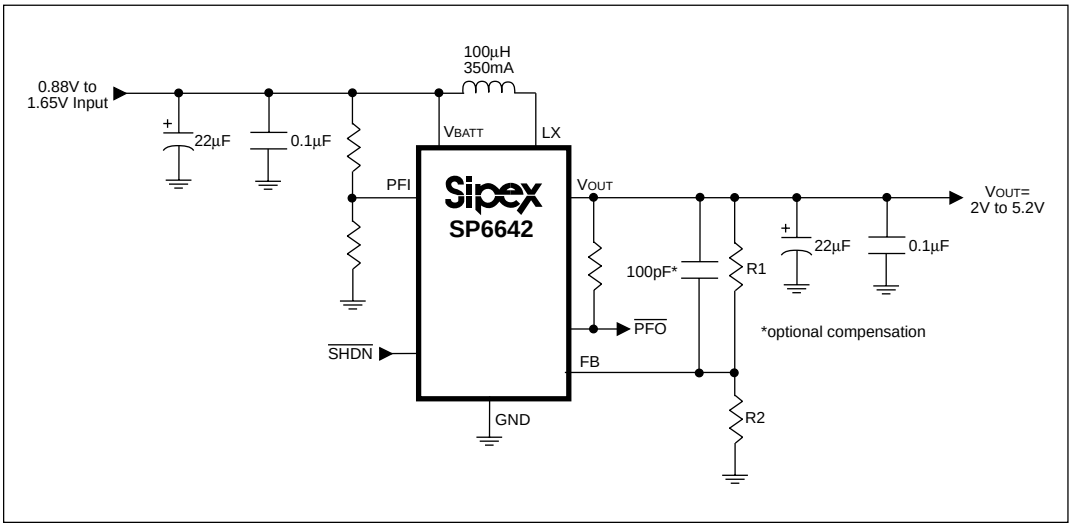


Figure 25. Adjustable Output Voltage Circuitry

synchronous-rectifier body diode from the input to the output. To disable the shutdown feature, designers can connect $\overline{SHDN}$ to V_{BATT}.

Adjustable Output Voltage

Driving FB to ground (logic LOW) will drive the output voltage to the fixed-voltage operation of +3.3V ± 4%. Connecting FB to a voltage divider between V_{OUT} and ground will select an adjustable output voltage between +2V and +5.5V. Refer to *Figure 25*. FB regulates to +1.23V.

Since the FB leakage current is 10nA maximum, designers should select the feedback resistor R2 in the 100kΩ to 1MΩ range. R1 can be determined with the following equation:

$$R1 = R2 \times \left[\frac{V_{OUT}}{V_{REF}} - 1 \right]$$

where R3 and R4 are the feedback resistors in *Figure 25*, V_{OUT} is the output voltage, and V_{REF} is 1.23V.

Battery Reversal Protection

The SP6642/6643 devices will tolerate single-cell battery reversal up to the package power-dissipation limits noted in the **ABSOLUTE MAXIMUM RATINGS** section. An internal diode in series with an internal 5Ω resistor limits any reverse current to less than 220mA preventing damage to the devices. Prolonged operation above 220mA reverse-battery current can degrade performance of the devices.

The Inductor

It is recommended that designers implement a 100µH inductor for typical application of the SP6642/6643 devices. Lower inductor values down to 68µH will increase the maximum output current. Higher inductor values up to 220µH will reduce peak inductor current and any consequent ripple and noise. The saturation-current rating of the inductor selected must exceed the peak current limit synthesized by the SP6642/6643 devices' timing algorithms. This can be calculated with the following equation:

$$I_{PEAK} = \frac{K_{MAX}}{L_{MIN}}$$

where I_{PEAK} is the peak current, K_{MAX} is 35V-µs, and L_{MIN} is the minimum inductance selected. The maximum recommended I_{PEAK} is 350mA. To optimize efficiency, select an inductor with a series resistance less than 1Ω.

Table 1 lists surface mount inductor information for the user, including series resistance and saturation current rating.

It is suggested designers select the largest inductor value possible that will satisfy the load requirement and minimize peak switching current and any resultant noise and voltage ripple. A closed-core inductor, such as a toroid or shielded bobbin, will minimize any fringe magnetic fields or EMI.

APPLICATION NOTES

Printed circuit board layout is a critical part of design. Poor designs can result in excessive EMI on the voltage gradients and feedback paths on the ground planes with applications involving high switching frequencies and large peak currents. Excessive EMI can result in instability or regulation errors.

All power components should be placed on the PC board as closely as possible with the traces kept short, direct, and wide (≥50mils or 1.25mm). Extra copper on the PC board should be integrated into ground as a pseudo-ground plane. On a multilayer PC board, route the star ground using component-side copper fill, then connect it to the internal ground plane using vias.

For the SP6642/6643 devices, the inductor and input and output filter capacitors should be soldered with their ground pins as close together as possible in a star-ground configuration. The V_{OUT} pin must be bypassed directly to ground as close to the SP6642/6643 devices as possible (within 0.2in or 5mm). The DC-DC converter and any digital circuitry should be placed on the opposite corner of the PC board as far away from sensitive RF and analog input stages. The external voltage-feedback network should be placed very close to the FB pin (within 0.2in or 5mm). Any noisy traces, such as from the LX pin, should be kept away from the voltage-feedback network and separated from it using grounded copper to minimize EMI.

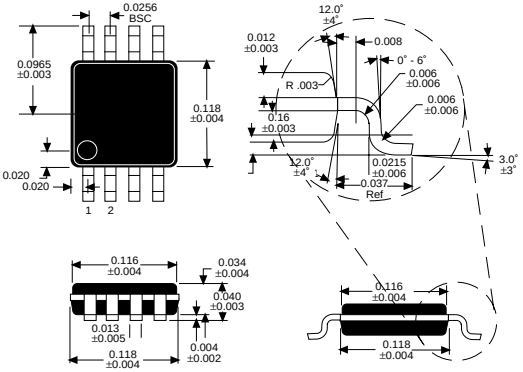
Capacitor equivalent series resistance is a major contributor to output ripple, usually greater than 60%. Low ESR capacitors are recommended. Ceramic capacitors have the lowest ESR. Low-ESR tantalum capacitors may be a more acceptable solution having both a low ESR and lower cost than ceramic capacitors. Designers should select input and output capacitors with a rating exceeding the peak inductor current. Do not allow tantalum capacitors to exceed their ripple-current ratings. A 22µF, 6V, low-ESR, surface-mount tantalum output filter capacitor typically provides 60mV output ripple when stepping up from 1.3V to 3.3V at 20mA. An input filter capacitor can reduce peak currents drawn from the battery and improve efficiency. Low-ESR aluminum electrolytic capacitors are acceptable in some applications but standard aluminum electrolytic capacitors are not recommended.

Designers should add LC pi filters, linear post-regulators, or shielding in applications necessary to address excessive noise, voltage ripple, or EMI concerns. The LC pi filter's cutoff frequency should be at least a decade or two below the DC-DC converters's switching frequency for the specified load and input voltage.

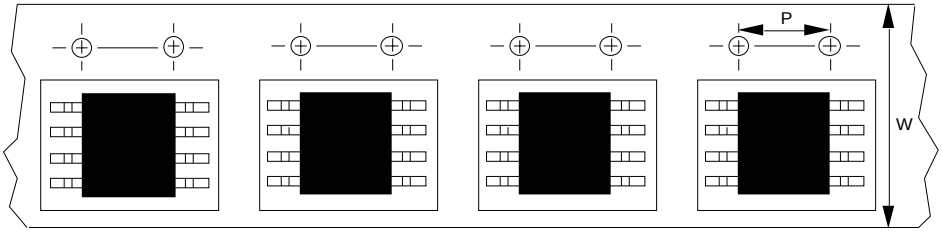
Table 1. Surface-Mount Inductor Information

INDUCTANCE (µH)	VENDOR/PART	INDUCTOR SPECIFICATION	
		RESISTANCE (Ω)	I_{SAT} (mA)
68	Coilcraft DO1608-683	0.75	400
	Sumida CD54-680	0.46	610
100	Coilcraft DO1608-104	1.1	310
	Sumida CD54-101	0.7	520
	TDK NLC565050T-101K	1.6	250
150	Coilcraft DO1608-154	1.7	270
	Sumida CD54-151	1.1	400
	TDK NLC565050T-151K	2.2	210
220	Coilcraft DO1608-224	2.3	220
	Sumida CD54-221	1.57	350

All package dimensions in inches



50 µSOIC devices per tube



8-pin µSOIC 13" reels: P = 8mm, W = 12mm			
pkg	min qty per reel	std qty per reel	max qty per reel
EU	500	2500	3000

ORDERING INFORMATION

Model	Temperature Range	Package Type
SP6642EU	-40°C to +85°C	8-Pin μSOIC
SP6643EU	-40°C to +85°C	8-Pin μSOIC

Please consult the factory for pricing and availability on a Tape-On-Reel option.

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